TEXAS INSTRUMENTS

Linear Circuits

Power+™, Peripheral Drivers/Actuators, Display Drivers

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Volume 4

Power+™, Peripheral Drivers/Actuators, Display Drivers

TEXAS INSTRUMENTS

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INTRODUCTION

Texas Instruments offers an extensive line of industry-standard integrated circuits designed to provide highly reliable circuits for switching inductive loads such as lamps, solenoids, motors and relays.

TI power devices represent technologies from classic bipolar, through BIDFET†, to the Texas Instruments PRISM™ process, which offer improvements in power consumption and temperature stability.

This data book (volume 4 of 4) provides information on the following types of products:

- Peripheral drivers/actuator circuits
- Display driver circuits
- Intelligent Power+™ circuits with protection and diagnostic features
- Power+ Logic™ circuits, which integrate logic control with multiple power FETs
- Power+ Array™ devices, which integrate multiple discrete-like power FETs into one package

TI continues to enhance quality and reliability of integrated circuits by improving materials, processes, test methods, and test equipment. Quality and performance are monitored throughout all phases of manufacturing; quality specifications and programs are continuously enhanced.

The alphanumeric listing in this data book includes all devices in Volumes 1, 2, 3, and 4. Products in this data book are shown in **bold** type. The alphanumeric index provides a method of quickly locating the correct device type. The selection guide includes a functional description of each device providing key parameter information and packaging types. Ordering information and mechanical data are in the last section of the data book.

While this volume offers design and specification data for TI power integrated circuits, complete technical data for any TI semiconductor product is available from your nearest TI field sales office, local authorized TI distributor, or by writing directly to:

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We believe the new 1993 Linear Circuits Data Book, Volume 4, is a significant addition to your library of technical literature from Texas Instruments.

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.
PRISM, Intelligent Power+, Power+ Arrays, and Power+ Logic are trademarks of Texas Instruments Incorporated.

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† New devices added to this volume

‡ MIL-STD-883 versions of these devices are available.

†New devices added to this volume

Power+ Arrays™

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60	7.5	2	0.09	200	Totally independent	200	TPIC5201	KV	2–99

Power+ Logic™

OFF-STATE VOLTAGE MAX (V)	OUTPUT CURRENT (mA)	DRIVERS PER PACKAGE	$R_{DS(on)}$ (Ω)	INPUT COMP.	FUNCTION	DELAY TIME TYP (ns)	TYPE	PKG	PAGE
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45	250	8	1.3	CMOS	8-bit D-type latch	625	TPIC6273	DW, N	2–117
45	250	8	1.3	CMOS	8-bit shift register	625	TPIC6595	DW, N	2–125
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DESC.	PRODUCT FEATURES	DRIVERS PER PKG	INPUT COMP.	POWER SUPPLY	TYPE	PKG	PAGE
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					SN75512B		4–37
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					SN75518		4–49
	Serial-in parallel-out architecture, 60-V totem-pole outputs, 40-mA current source output, Improved direct replacement for UCN4810A and TL4810A	10	CMOS	V_{CC1}(logic) = 5 V to 15 V, V_{CC2}(display) = 0 to 60 V	TL4810B	DW, N	4–117
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DESC.	PRODUCT FEATURES	DRIVERS PER PKG	INPUT COMP.	POWER SUPPLY	TYPE	PKG	PAGE
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DESC.	PRODUCT FEATURES	DRIVERS PER PKG	INPUT COMP.	POWER SUPPLY	TYPE	PKG	PAGE
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SWITCHING VOLTAGE MAX (V)	OFF-STATE VOLTAGE MAX (V)	OUTPUT CURRENT (mA)	DRIVERS PER PKG	OUTPUT CLAMP DIODES	INPUT COMP.	FUNCTION	DELAY TIME TYP (ns)	TYPE	PKG	PAGE
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UDN-5722	SN75477	3–115
ULN-2001	ULN2001A	3–127
ULN-2002	ULN2002A	3–127
ULN-2003	ULN2003A	3–127
ULN-2004	ULN2004A	3–127
ULN-2021	SN75466	3–101
ULN-2022	SN75467	3–101
ULN-2023	SN75468	3–101
ULN-2024	SN75469	3–101
ULN-2074	ULN2074	3–135
ULN-2075	ULN2075	3–135

UNITRODE	SUGGESTED TI REPLACEMENT	PAGE NO.
L293	L293	3–7
L293	SN754411†	3–121
L293D	L293D	3–11
L293D	SN754410†	3–121
L298	L298	3–15

† Consult product data sheet for possible slight product differences.

GOULD/AMI	SUGGESTED TI REPLACEMENT	PAGE NO.
S4535	SN75518	4–49

SILICONIX	SUGGESTED TI REPLACEMENT	PAGE NO.
SI9552	SN75552	4–57
SI9553	SN75553	4–65
SI9554	SN75554	4–65

SPRAGUE	SUGGESTED TI REPLACEMENT	PAGE NO.
UCN5810A	TL4810B	4–117
UCN5812A	TL5812	4–123
UCN5818A	SN75518	4–49
UCN5852A	SN75552	4–57
UCN5853A	SN75553	4–65
UCN5854A	SN75554	4–65

SUPERTEX	SUGGESTED TI REPLACEMENT	PAGE NO.
HV52	SN75552	4–57
HV53	SN75553	4–65
HV54	SN75554	4–65

C_{gd} **Gate-Drain Capacitance**
Capacitance measured between the gate and drain with V_{GS} = 0 V ($C_{gd} = C_{rss}$)

C_{ds} **Drain-Source Capacitance**
Capacitance measured between the drain and source with V_{GS} = 0 V ($C_{ds} = C_{iss} - C_{rss}$)

C_{gs} **Gate-Source Capacitance**
Capacitance measured between the gate and source with V_{GS} = 0 V ($C_{ds} = C_{oss} - C_{rss}$)

C_{iss} **Short-Circuit Input Capacitance**
Input capacitance with drain and source shorted ($C_{iss} = C_{gd} + C_{gs}$, C_{ds} shorted)

C_{oss} **Short-Circuit Output Capacitance**
Total capacitance between drain and source with gate and source shorted ($C_{oss} = C_{ds} + C_{gd}$, C_{gs} shorted)

C_{rss} **Short-Circuit Reverse Transfer Capacitance**
Gate-to-drain capacitance with V_{GS} = 0 ($C_{rss} = C_{gd}$)

E_{AS} **Single-Pulse Avalanche Energy**
Maximum energy dissipation allowed during avalanche breakdown for a single pulse of avalanche current

g_{fs} **Common-Source Large-Signal Transconductance**
Ratio of change in drain current due to a change in gate-to-source voltage

I_{AS} **Peak Avalanche Current**
Maximum allowable current during avalanche breakdown

I_{CC} **Power Supply Current**
Total current from the V_{CC} supply

I_D **DC Drain Current**
Measured dc current into the drain

I_{DM} **Peak-Drain Current, Single Output**
Maximum allowable value of drain current

I_{DSS} **Zero-Gate-Voltage Drain Current**
Current into drain when gate-to-source voltage is zero

I_{DSX} **Off-State Drain Current**
See Zero-Gate-Voltage Drain Current (I_{DSS})

I_{GSSF} **Forward Gate Current, Drain-to-Source Short Circuited**
DC current into gate with forward gate-to-source voltage and drain shorted to source

I_{GSSR} **Reverse Gate Current, Drain-to-Source Short Circuited**
DC current into gate with reverse gate-to-source voltage and drain shorted to source

I_I **Input Current**
DC current to the gate

I_{IH} **Input Current High**
Current the device uses to switch state from low to high

I_{IL} **Input Current Low**
Current the device uses to switch state from high to low

I_O **Continuous Output Current**
DC output current across the drain-to-source junction

$I_{O(chp)}$ **Output Chopping Current**
Value at which output current changes from continuous current to low duty cycle pulsed current

I_{OM} **Peak Output Current**
Maximum output current in the on state

I_R **Reverse Leakage Current**
Current flow across reverse-biased junction at specified applied voltage

I_{SD} **Source-Drain Diode Current**
Maximum continuous forward diode current

P_D **Maximum Device Power Dissipation**
Amount of power consumed by die such that maximum junction temperature is not exceeded at held case temperature

Q_g **Total Gate Charge**
Maximum charge drawn by gate at a specified V_{GS}

Q_{gd} **Gate-Drain Charge**
Charge between the gate and drain of device

Q_{gs} **Gate-Source Charge**
Charge between the gate and source of device

$r_{DS(on)}$ **Static Drain-Source On-State Resistance**
Resistance between the drain and source during on state

r_I **Input Resistance**
Resistance between gate and source

$R_{\theta JA}$ **Junction-to-Ambient Thermal Resistance**
Thermal resistance (steady state) from the device case to the ambient (air)

$R_{\theta JC}$ **Junction-to-Case Thermal Resistance**
Thermal resistance (steady state) from the device junction to case

r_o **Output Resistance**
Resistance between drain and source

t_a **Reverse-Recovery-Current Rise Time**
Elapsed time for diode current to reach maximum value during reverse recovery

T_A **Ambient Operating Temperature (Free Air)**
Air temperature measured below a device in an environment cooled only by natural air convection

t_c **Cycle Time**
Time interval between the start and end of a cycle

T_C **Case Operating Temperature**
Temperature measured at a specific location on the case of a device

$t_{d(off)}$ **Turn-Off Delay Time**
Time interval during which an input pulse falls from 90% of its peak value to drain waveform falling to 10% of its off-state amplitude

$t_{d(on)}$ **Turn-On Delay Time**
Time interval during which an input pulse rises from 10% of its peak value to drain waveform falling to 90% of its off-state amplitude

t_f **Fall Time**
Time interval for signal to change from 90% to 10% of its peak value

t_h **Hold Time**
Time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

T_J **Virtual Junction Temperature**
Calculated value of the silicon junction(s) temperature based on the thermal and electrical behavior of the device

t_{off} **Turn-Off Time**
Time interval between gate turn off and drain-to-source shutdown

t_{on} **Turn-On Time**
Time interval between gate turn on and drain-to-source turn on

t_{PHL} **Propagation Delay Time, High-to-Low Level Output**
Time interval for drain-to-source signal to fall from 90% to 10% of its peak value

t_{PLH} **Propagation Delay Time, Low-to-High Level Output**
Time interval for drain-to-source signal to rise from 10% to 90% of its peak value

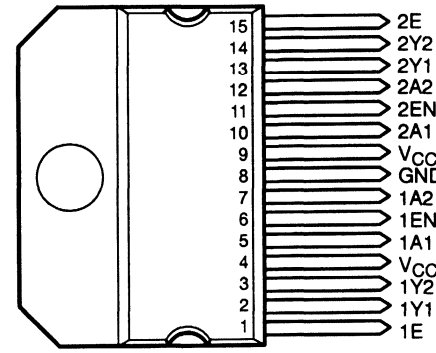
t_r **Rise Time**
Time interval for signal to rise from 10% to 90% of its peak value

t_{rr}	**Reverse-Recovery Time** Time required to remove excess carriers from a diode after reverse of carrier flow
t_{su}	**Setup Time** Time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal
t_v	**Valid Time** Delay time from 50% rising edge of serial clock input to 10% change in serial output
t_w	**Pulse Duration** Active pulse time measured at 50% of steady-state amplitude from leading edge to trailing edge of the same pulse
V_{BR}	**Breakdown Voltage** Drain-to-source voltage at which device avalanche multiplication occurs
V_{DS}	**Drain-Source Voltage** Voltage measured across the drain to source
V_F	**Clamp Diode Forward Current** Measurement of current through the clamp diode
V_{GS}	**Gate-Source Voltage** Measurement of the input voltage in reference to the source
V_I	**Input Voltage** Voltage measured from gate to source
V_{IH}	**Input Voltage High** Voltage on gate that initiates drain-to-source turn on
V_{IL}	**Input Voltage Low** Voltage on gate that initiates drain-to-source turn off
V_{OH}	**High-Level Output Voltage** Voltage measured on the source-to-drain in high state
V_{OK}	**Output Clamp Voltage** Voltage measured on the source to clamp input
V_{OL}	**Low-Level Output Voltage** Voltage measured on the drain-to-source in low state
V_{SD}	**Forward On-Voltage** Voltage measured on the source-to-drain in the forward direction
$V_{SD(ov)}$	**Overvoltage Shutdown Voltage** Specified temperature at which overvoltage shutdown circuit is activated
V_{TGS}	**Gate-Source Threshold voltage** Gate voltage required to produce a specified amount of drain current

SLIS006 – D2942, JUNE 1987 – REVISED JANUARY 1990

- **Formerly TLP298**
- **2-A Output Current Capability Per Full-H Driver**
- **Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers**
- **Wide Range of Output Supply Voltage 5 V to 46 V**
- **Separate Input-Logic Supply Voltage Thermal Shutdown**
- **Internal Electrostatic Discharge Protection**
- **High Noise Immunity**
- **3-State Outputs**
- **Minimized Power Dissipation**
- **Sink/Source Interlock Circuitry Prevents Simultaneous Conduction**
- **Improved Functional Replacement for the SGS L298**

KV PACKAGE
(TOP VIEW)



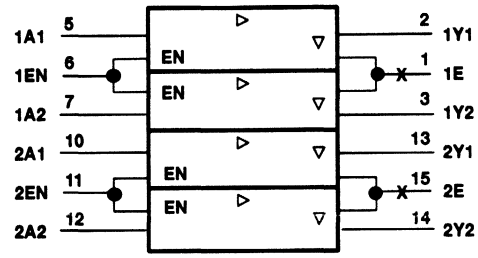
The tab is electrically connected to GND.

description

The TPIC0298 is a dual high-current full-H driver designed to provide bidirectional drive currents of up to 2 A at voltages from 5 V to 46 V. It is designed to drive inductive loads such as relays, solenoids, dc motors, stepping motors, and other high-current or high-voltage loads in positive-supply applications. All inputs are TTL compatible. Each output (Y) is a complete totem-pole drive with a Darlington transistor sink and a pseudo-Darlington source. Each full-H driver is enabled separately. Outputs 1Y1 and 1Y2 are enabled by 1EN and outputs 2Y1 and 2Y2 are enabled by 2EN. When an EN input is high, the associated channels are active. When an EN input is low, the associated channels are off (i.e., in the high-impedance state).

Each half of the device forms a full-H reversible driver suitable for solenoid or motor applications. The current in each full-H driver can be monitored by connecting a resistor between the sense output terminal 1E and GND and another resistor between sense output terminal 2E and GND.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

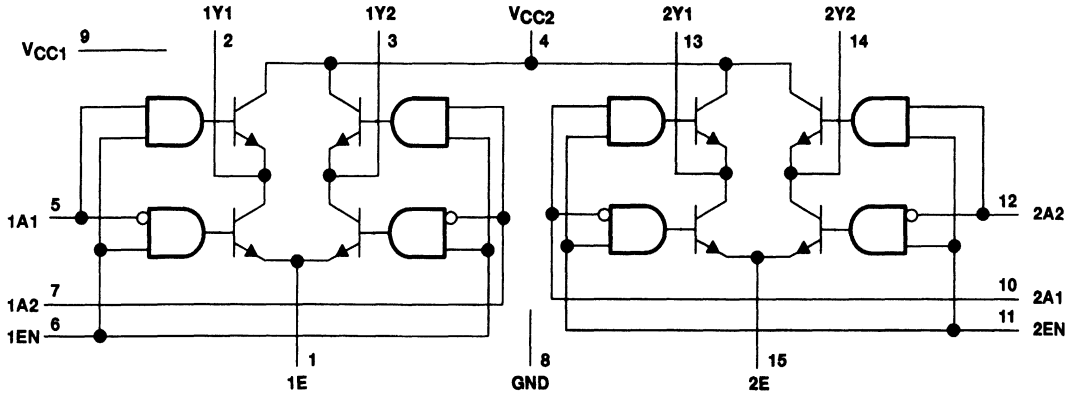
INPUTS		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level, L = low-level
X = irrelevant
Z = high-impedance (off)

External high-speed output-clamp diodes should be used for inductive transient suppression. To minimize device power dissipation, a V_{CC1} supply voltage, separate from V_{CC2}, is provided for the logic inputs.

The TPIC0298 is designed for operation from 0°C to 70°C.

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)

Logic supply voltage range, V_{CC1} (see Note 1) ..... −0.3 V to 7 V
Output supply voltage range, V_{CC2} ..... −0.3 V to 50 V
Input voltage range at A or EN, V_I (see Note 2) ..... −1.6 V to 7 V
Output voltage range, V_O ..... −2 V to V_{CC2} + 2 V
Emitter terminal (1E and 2E) voltage range, V_E ..... −0.5 V to 2.3 V
Emitter terminal (1E and 2E) voltage (nonrepetitive, $t_w \leq 50$ µs) ..... −1 V
Input current at A or EN, I_I ..... −15 mA
Peak output current, I_{OM}: (nonrepetitive, $t_w \leq 0.1$ ms) ..... ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) ..... ±2.5 A
Continuous output current, I_O ..... ±2 A
Peak combined output current for each full-H driver (see Note 3):
(nonrepetitive, $t_w \leq 0.1$ ms) ..... ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) ..... ±2.5 A
Continuous combined output current for each full-H driver (see Note 3) ..... ±2 A
Continuous dissipation at (or below) 25°C free-air temperature (see Note 4) ..... 3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 4) ..... 25 W
Operating free-air, case, or virtual junction temperature range ..... −40°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to the network GND, unless otherwise noted.
2. The maximum current limitation at this terminal generally occurs at a voltage of lower magnitude than the voltage limit. Neither the maximum current nor the maximum voltage for this terminal should be exceeded.
3. Combined output current applies to each of the two full-H drivers individually. This current is the sum of the currents at outputs 1Y1 and 1Y2 for full-H driver 1 and the sum of the currents at outputs 2Y1 and 2Y2 for full-H driver 2. The full-H drivers can carry the rated combined current simultaneously.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		5	46	V
Emitter terminal (1E or 2E) voltage, V_E (see Note 5)		−0.5†	2	V
			$V_{CC1}-3.5$	
			$V_{CC2}-4$	
High-level input voltage, V_{IH} (see Note 5)	A	2.3	V_{CC1}	V
			$V_{CC2}-2.5$	
	EN	2.3	7	
			V_{CC1}	
Low-level input voltage at A or EN, V_{IL}		−0.3†	1.5	V
Output current, I_O			±2	A
Communication frequency			40	kHz
Operating free-air temperature, T_A		0	70	°C

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for emitter terminal voltage and logic voltage levels.

NOTE 5: For optimum device performance, the maximum recommended voltage at any A input is 2.5 V lower than V_{CC2}, the maximum recommended voltage at any EN input is V_{CC1}, and the maximum recommended voltage at any emitter terminal is 3.5 V lower than V_{CC1} and 4 V lower than V_{CC2}.

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and V_E, T_J = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -12$ mA				−0.9	−1.5	V
V_{OH}	High-level output voltage		$I_{OH} = -1$ A			$V_{CC2}-1.8$	$V_{CC2}-1.2$		V
			$I_{OH} = -2$ A			$V_{CC2}-2.8$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage		$I_{OL} = 1$ A				$V_E+1.2$	$V_E+1.8$	V
			$I_{OL} = 2$ A				$V_E+1.7$	$V_E+2.6$	
V_{drop}	Total source pulse sink output voltage drop		$I_{OH} = -1$ A, $I_{OL} = 1$ A		See Note 6		2.4	3.4	V
			$I_{OH} = -2$ A, $I_{OL} = 2$ A				3.5	5.2	
I_{OZH}	Off-state (high-impedance state) output current, high-level voltage applied		$V_O = V_{CC2}$					500	µA
I_{OZL}	Off-state (high-impedance state) output current, low-level voltage applied		$V_O = 0$ V, $V_E = 0$ V					−500	µA
I_{IH}	High-level input current	A	$V_I = V_{IH}$	EN = H			20	100	µA
				EN = L				10	
		EN	$V_I = V_{IH} \le V_{CC1} - 0.6$ V				6	100	
I_{IL}	Low-level input current		$V_I = 0$ V to 1.5 V					−10	µA
I_{CC1}	Logic supply current		$I_O = 0$	All outputs at high level			7	12	mA
				All outputs at low level			20	32	
				All outputs at high impedance			4	6	
I_{CC2}	Output supply current		$I_O = 0$	All outputs at high level			25	50	mA
				All outputs at low level			6	20	
				All outputs at high impedance				2	

† All typical values are at V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0 V, T_J = 25°C (unless otherwise noted).

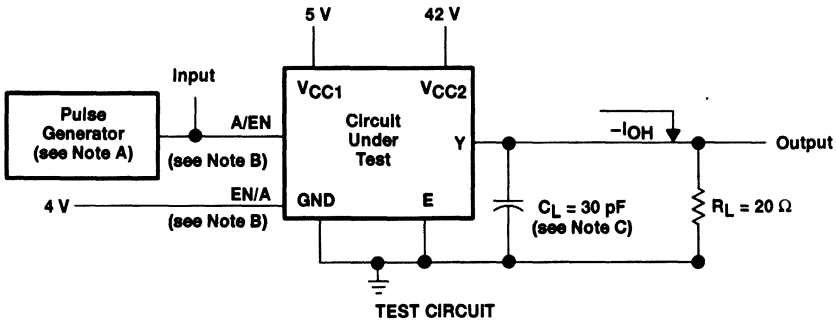
NOTE 6: The V_{drop} specification applies for I_{OH} and I_{OL} applied simultaneously to different output channels:

$$V_{drop} = V_{CC2} - V_{OH} + V_{OL} - V_E$$

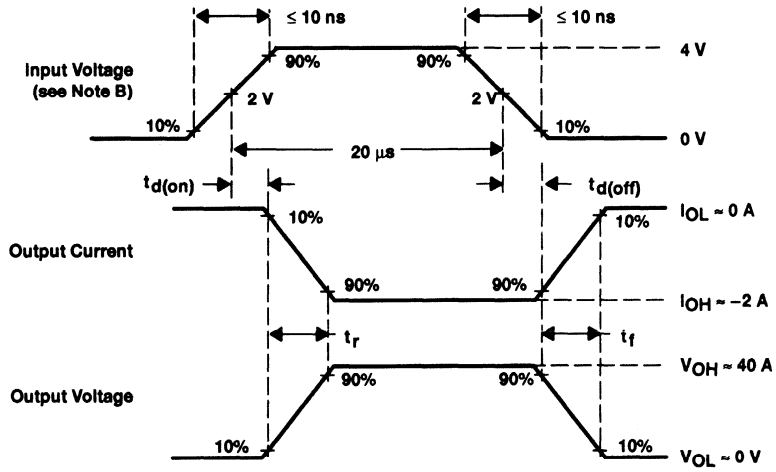
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time, source current from A input	C_L = 30 pF, See Figure 1		0.6		µs
$t_{d(off)}$	Turn-off delay time, source current from A input			0.8		µs
t_r	Rise time, source current (turning on)			0.8		µs
t_f	Fall time, source current (turning off)			0.2		µs
$t_{d(on)}$	Turn-on delay time, source current from EN input			0.5		µs
$t_{d(off)}$	Turn-off delay time, source current from EN input			2.5		µs
$t_{d(on)}$	Turn-on delay time, sink current from A input	C_L = 30 pF, See Figure 2		1.3		µs
$t_{d(off)}$	Turn-off delay time sink current from A input			0.5		µs
t_r	Rise time, sink current (turning on)			0.2		µs
t_f	Fall time, sink current (turning off)			0.2		µs
$t_{d(on)}$	Turn-on delay time, sink current from EN input			0.3		µs
$t_{d(off)}$	Turn-off delay time, sink current from EN input			1		µs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

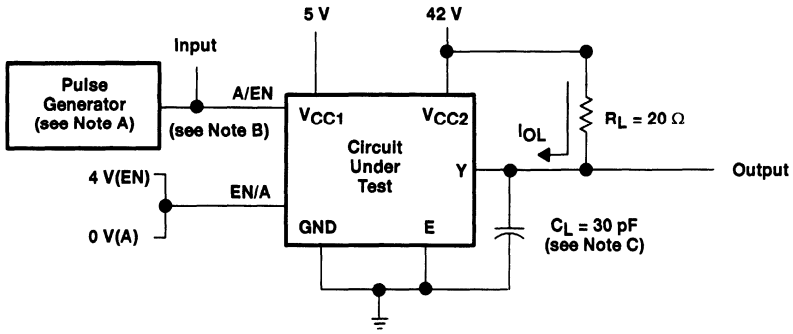


VOLTAGE AND CURRENT WAVEFORMS

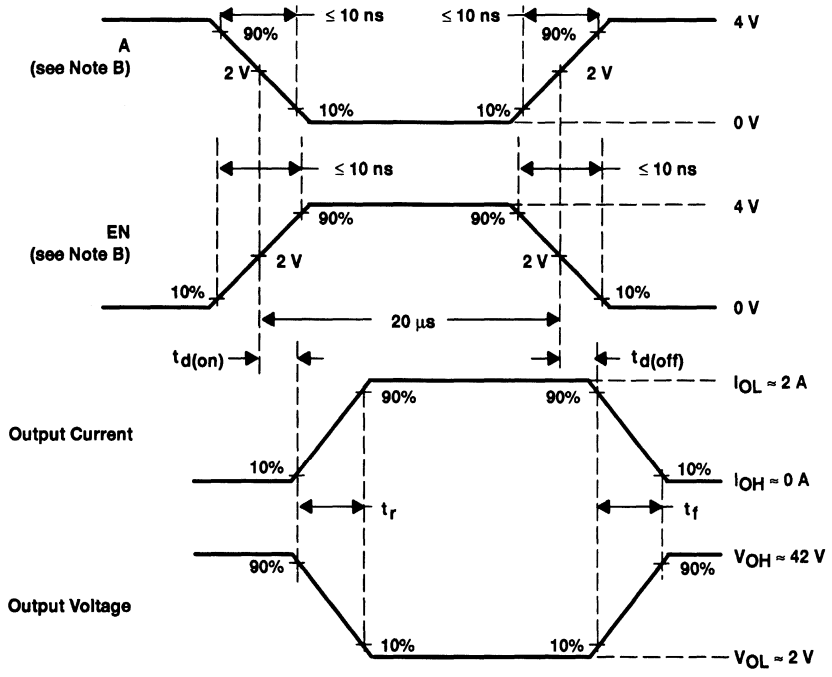
NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 4 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

Figure 1. Source Current Test Circuit and Waveforms From Data and Enable Inputs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 0 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

Figure 2. Sink Current Test Circuit and Voltage Waveforms From Data and Enable Inputs

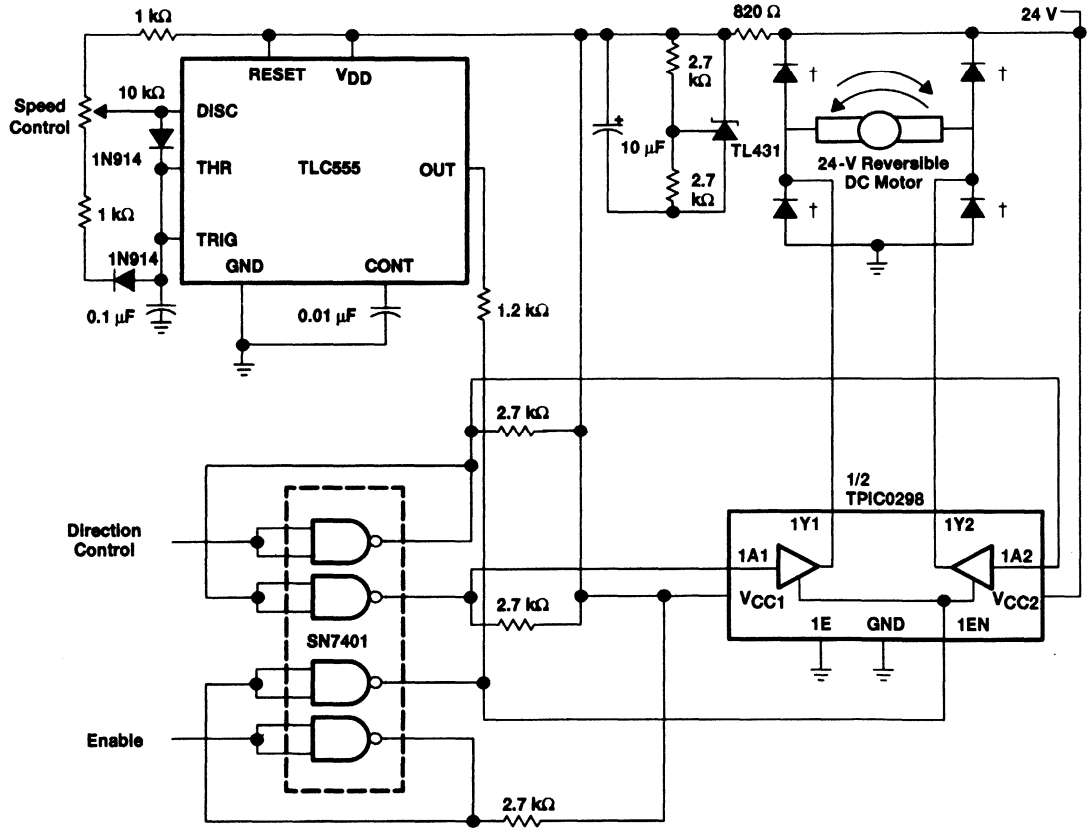
APPLICATION INFORMATION

This circuit shows one half of a TPIC0298 used to provide full-H bridge drive for a 24-V, 2-A dc motor. Speed control is achieved with a TLC555 timer. This provides variable duty-cycle pulses to the EN input of the TPIC0298. In this configuration, the operating frequency is approximately 1.2 kHz. The duty cycle is adjustable from 10% to 90% to provide a wide range of motor speeds. The motor direction is determined by the logic level at the direction control input. The circuit can be enabled or disabled by the logic level at the EN input. A 5-V supply for the logic and timer circuit is provided by a TL431 shunt regulator. For circuit operation, refer to the function table.

FUNCTION TABLE

ENABLE	DIRECTION CONTROL	1Y1	1Y2
H	H	Source	Sink
H	L	Sink	Source
L	X	Disabled	Disabled

X = don't care H = high level L = low level

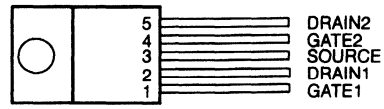


† Diodes are 1N4934 or equivalent.

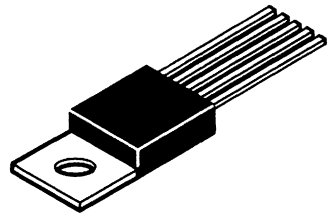
Figure 3. TPIC0298 as Bidirectional-DC Motor Drive

- **Two 7.5-A Independent Output Channels, Continuous Current Per Channel**
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 15 A Per Channel**
- **Avalanche Energy . . . 120 mJ**

KC PACKAGE
(TOP VIEW)



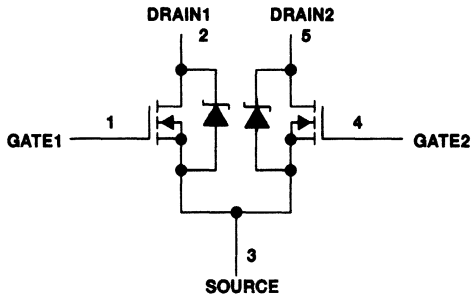
The tab is electrically connected to SOURCE.



description

The TPIC2202 is a monolithic power DMOS array that consists of two independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Gate-source voltage, V_{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I_D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T_A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T_C = 75°C, all outputs on (see Note 2)	31 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.42 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 μA, V_{GS} = 0		60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 7.5 A, V_{GS} = 15 V, See Notes 3 and 4			0.68	0.94	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.07	1	μA
			T_C = 125°C		1.3	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = −20 V, V_{DS} = 0			10	100	nA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{GS} = 15 V, I_D = 7.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C		0.09	0.125	Ω
			T_C = 125°C		0.15	0.21	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 5 A, See Notes 3 and 4		2.5	4.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz			490		pF
C_{oss}	Short-circuit output capacitance, common source				285		
C_{rss}	Short-circuit reverse transfer capacitance, common source				90		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 7.5 A, V_{GS} = 0, di/dt = 100 A/μs, V_{DS} = 48 V, See Figure 1		0.8	1.3	V
t_{rr}	Reverse recovery time			200		ns
Q_{RR}	Total source-drain diode charge			1.5		μC

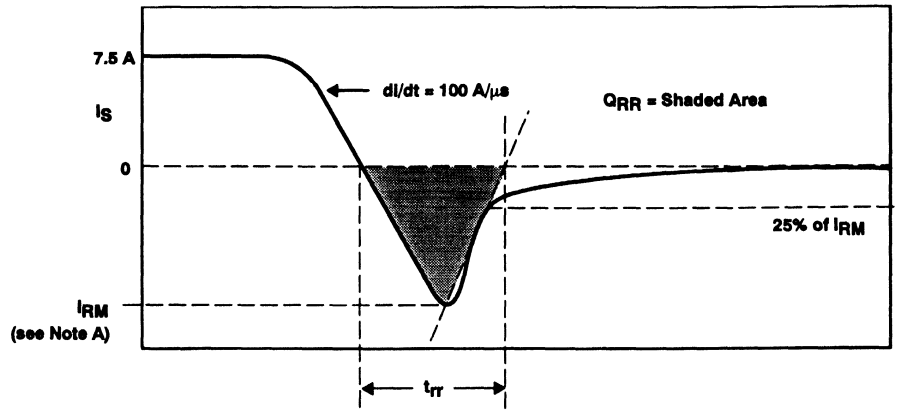
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 6.7 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		12		ns
$t_{d(off)}$	Turn-off delay time			100		
t_r	Rise time			43		
t_f	Fall time			5		
Q_g	Total gate charge	V_{DD} = 48 V, I_D = 2.5 A, V_{GS} = 10 V, See Figure 3		13.6	18	nC
Q_{gs}	Gate-source charge			8.3	11	
Q_{gd}	Gate-drain charge			5.3	7	
L_D	Internal drain inductance			7		nH
L_S	Internal source inductance			7		

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			2.4	°C/W
		One output dissipating power			3.3	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

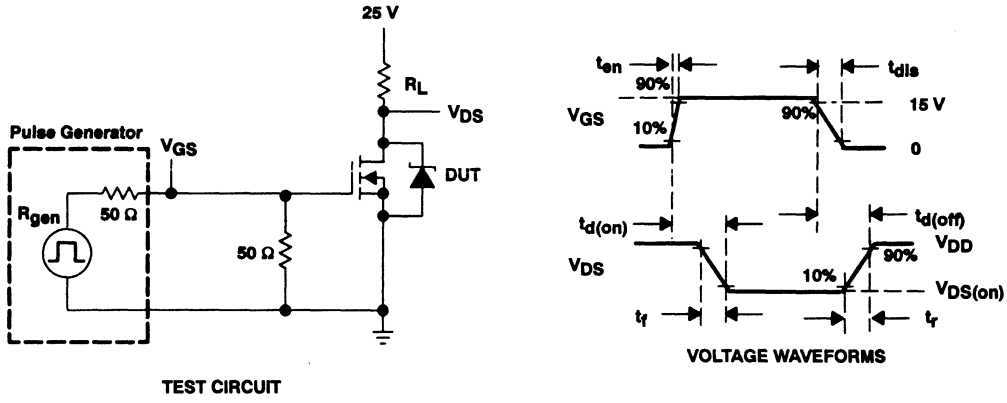


Figure 2. Test Circuit and Voltage Waveforms, Resistive Switching

PARAMETER MEASUREMENT INFORMATION

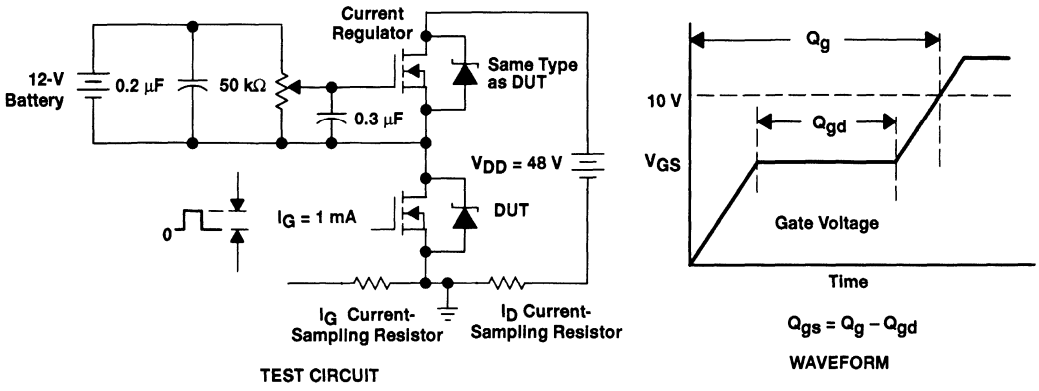
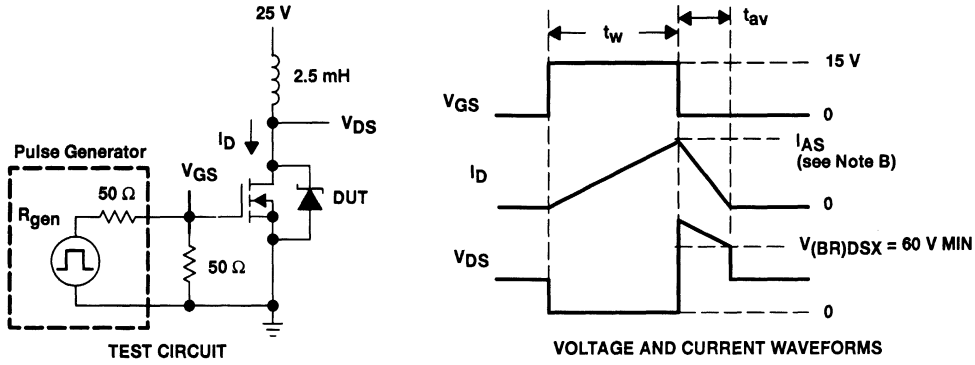


Figure 3. Gate Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 7.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
CASE TEMPERATURE

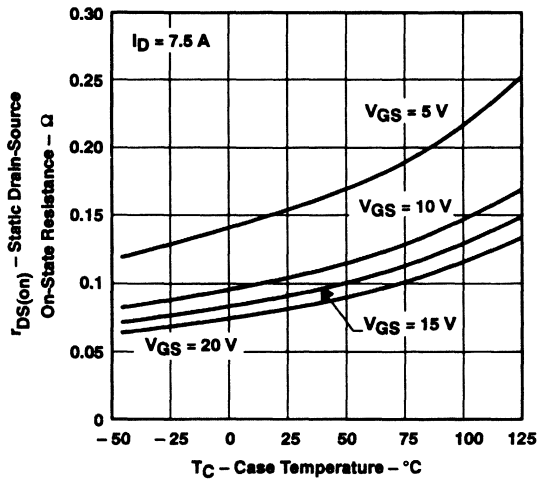


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

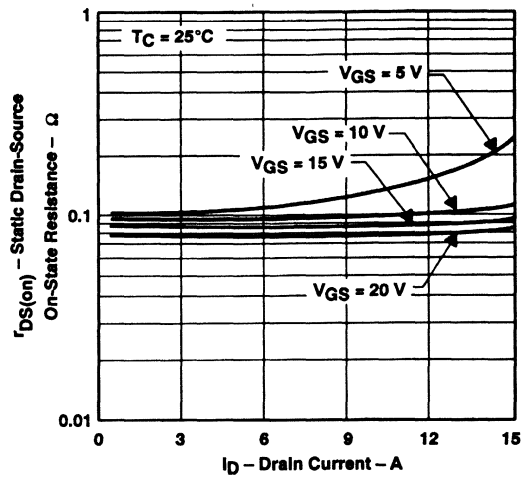


Figure 6

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

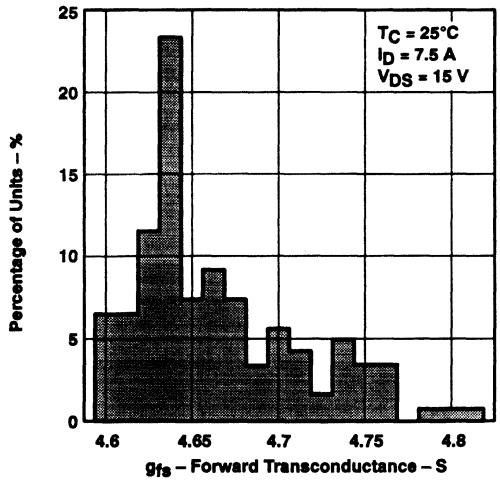


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

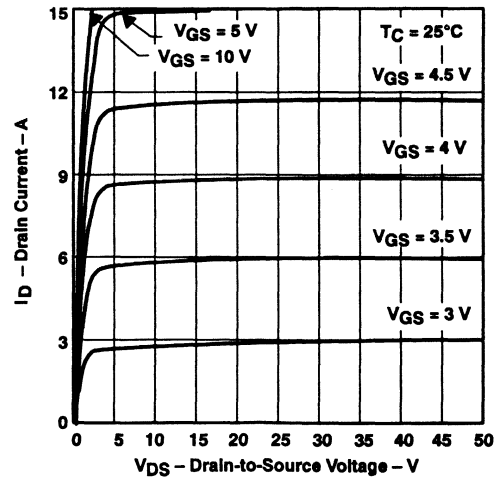


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE
vs
CASE TEMPERATURE

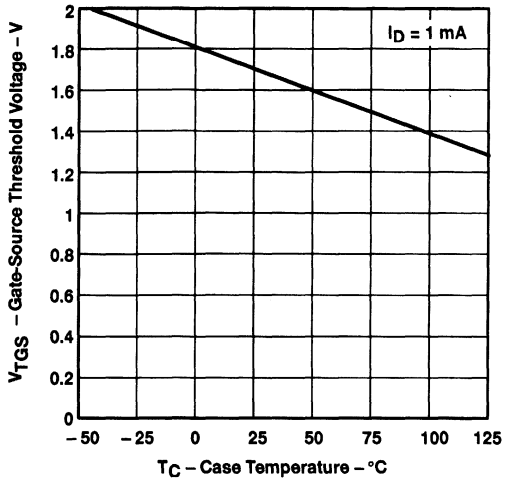


Figure 9

SOURCE-DRAIN DIODE CURRENT
vs
SOURCE-DRAIN VOLTAGE

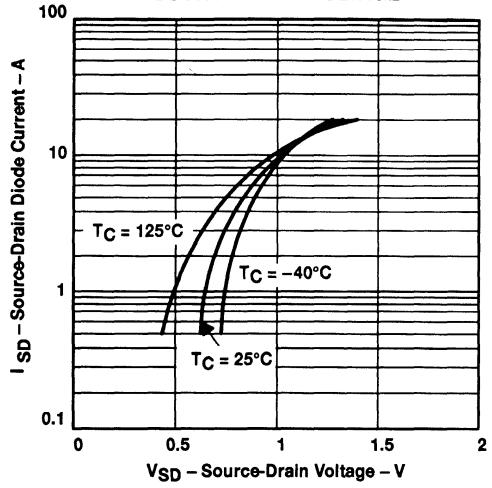


Figure 10

GATE-SOURCE VOLTAGE
vs
GATE CHARGE

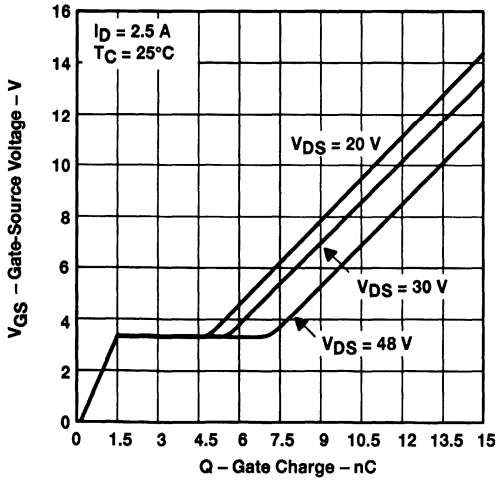


Figure 11

REVERSE RECOVERY TIME
vs
REVERSE di/dt

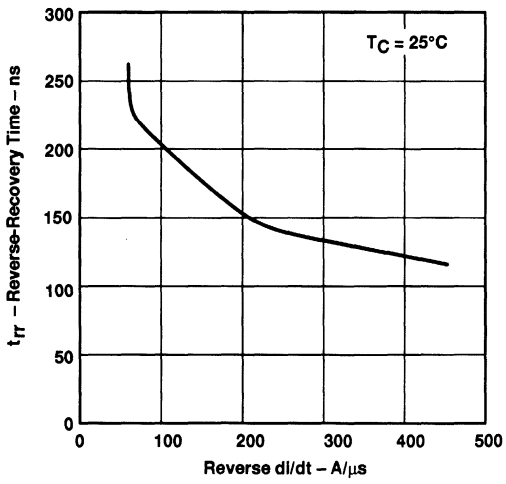


Figure 12

TYPICAL CHARACTERISTICS

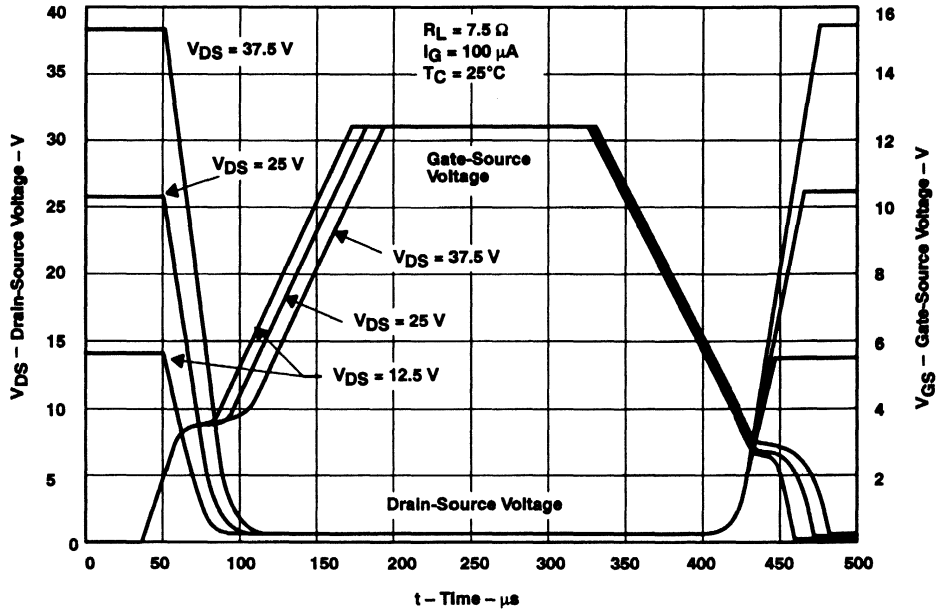


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-SOURCE VOLTAGE

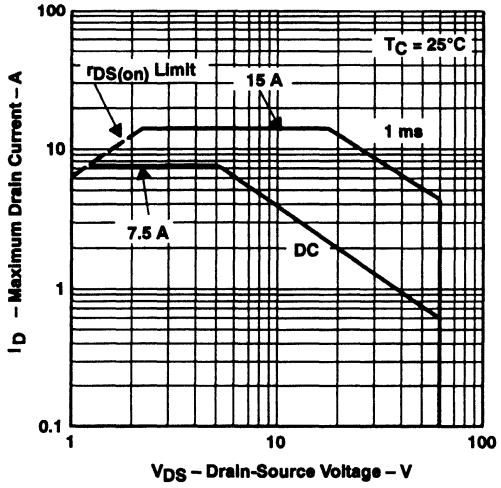


Figure 14

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

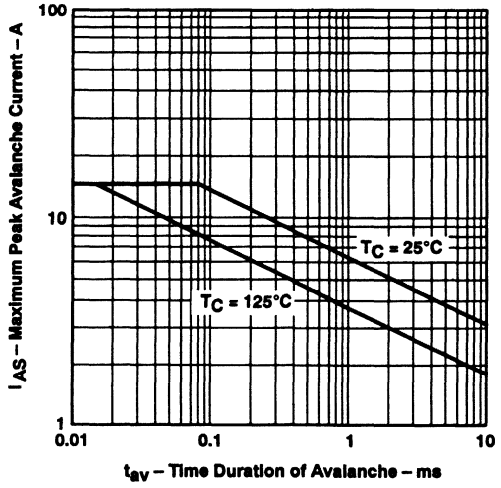
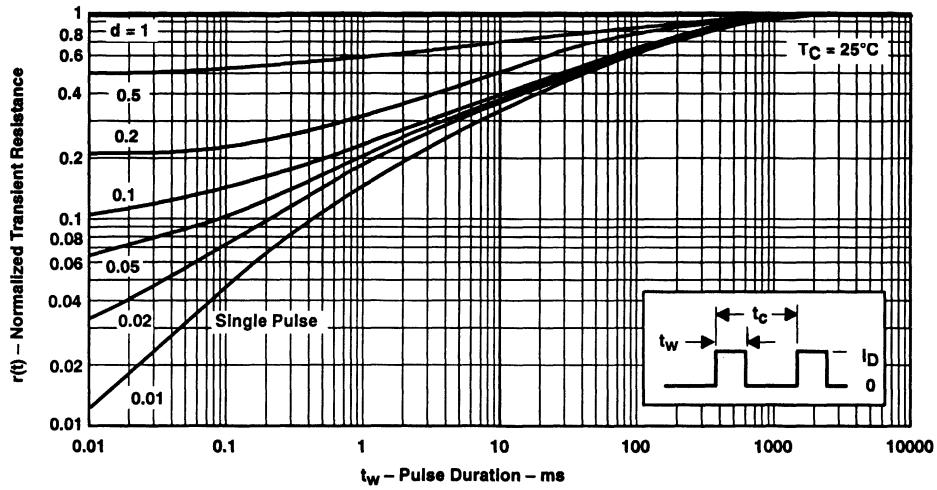


Figure 15

THERMAL INFORMATION

NORMALIZED TRANSIENT THERMAL IMPEDANCE vs SQUARE-WAVE PULSE DURATION



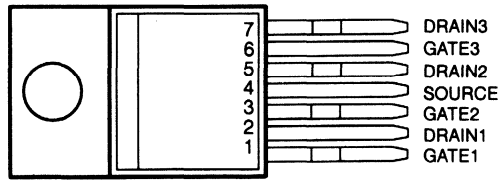
NOTES: $Z_{\theta JC}(t) = r(t) R_{\theta JC}$
t_w = pulse duration
t_c = period
d = duty cycle = t_w/t_c

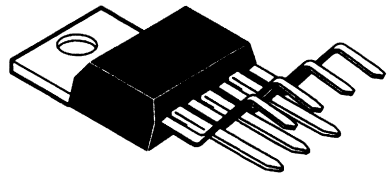
Figure 16

SLDS049 – D4043, SEPTEMBER 1992

- **Three 7.5-A Independent Output Channels, Continuous Current Per Channel**
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 15 A Per Channel**
- **Avalanche Energy . . . 120 mJ**

KV PACKAGE
(TOP VIEW)



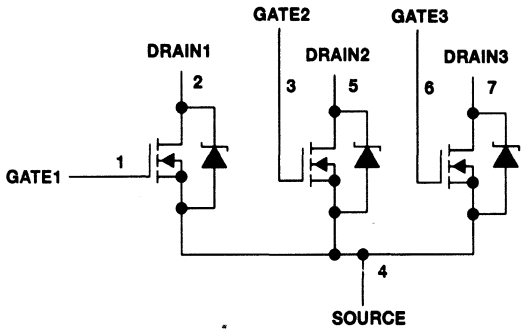


The tab is electrically connected to SOURCE.

description

The TPIC2301 is a monolithic power DMOS array that consists of three independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Gate-source voltage, V_{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I_D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T_A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T_C = 75°C, all outputs on (see Note 2)	50 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.66 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 µA, V_{GS} = 0			60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}			1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 7.5 A, V_{GS} = 15 V, See Notes 3 and 4				0.68	0.94	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C			0.07	1	µA
			T_C = 125°C			1.3	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0				10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = −20 V, V_{DS} = 0				10	100	nA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{GS} = 15 V, I_D = 7.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C			0.09	0.125	Ω
			T_C = 125°C			0.15	0.21	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 5 A, See Notes 3 and 4			3.3	4.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz				490		pF
C_{oss}	Short-circuit output capacitance, common source					285		
C_{rss}	Short-circuit reverse transfer capacitance, common source					90		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 7.5 A, V_{DS} = 48 V,	V_{GS} = 0, See Figure 1	di/dt = 100 A/µs,		0.8	1.3	V
t_{rr}	Reverse recovery time					200		ns
Q_{RR}	Total source-drain diode charge					1.5		µC

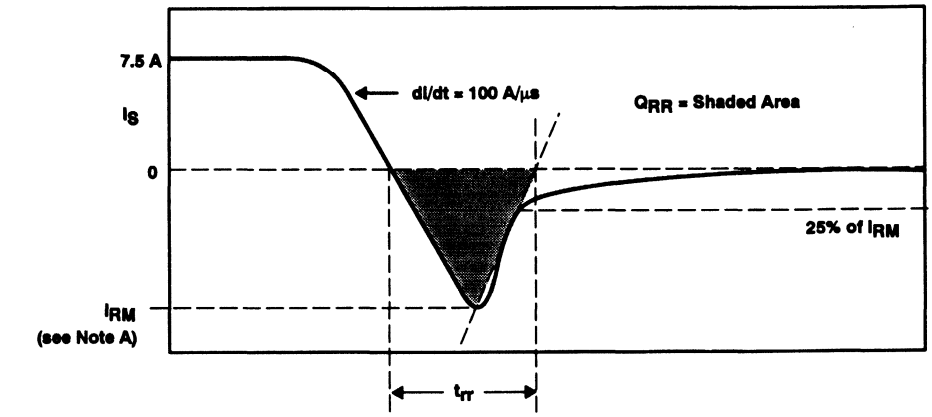
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, t_{dis} = 10 ns,	R_L = 6.7 Ω, See Figure 2	t_{en} = 10 ns,		12		ns
$t_{d(off)}$	Turn-off delay time					100		
t_r	Rise time					43		
t_f	Fall time					5		
Q_g	Total gate charge	V_{DS} = 48 V, See Figure 3	I_D = 2.5 A,	V_{GS} = 10 V,		13.6	18	nC
Q_{gs}	Gate-source charge					8.3	11	
Q_{gd}	Gate-drain charge					5.3	7	
L_D	Internal drain inductance					7		nH
L_S	Internal source inductance					7		

thermal resistance

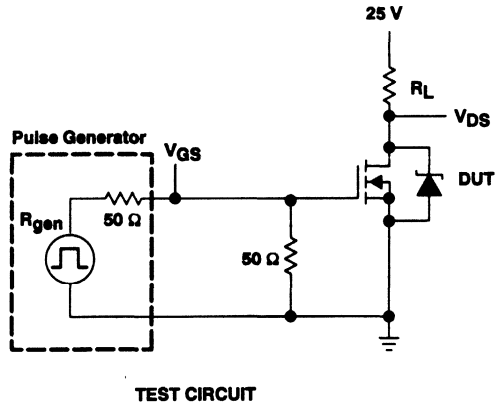
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			1.5	°C/W
		One output dissipating power			3.3	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode



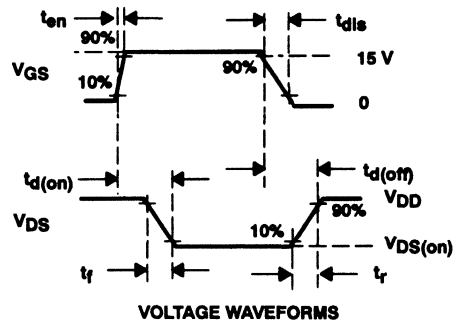


Figure 2. Resistive Switching

PARAMETER MEASUREMENT INFORMATION

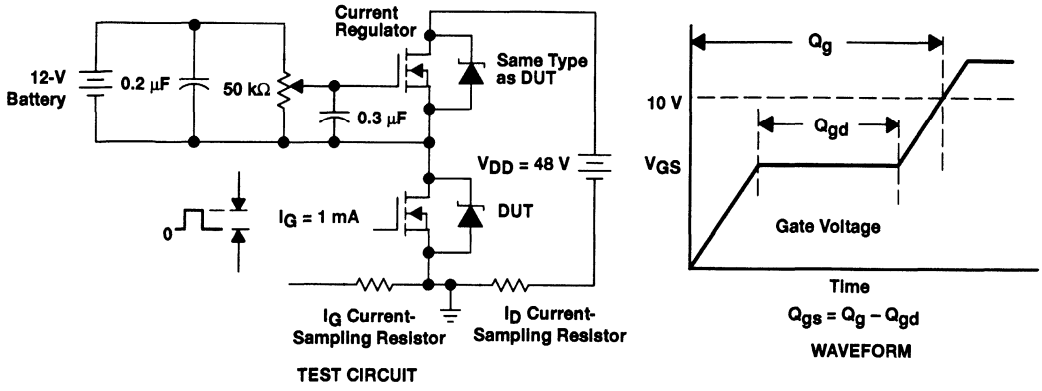
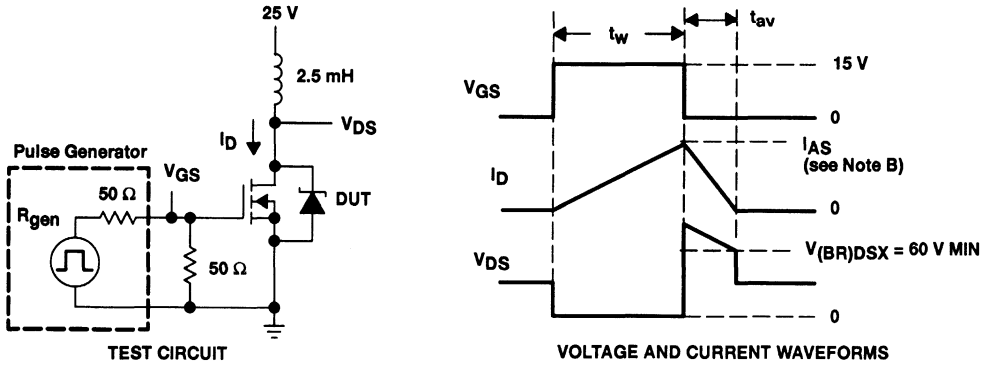


Figure 3. Gate-Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 7.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
CASE TEMPERATURE

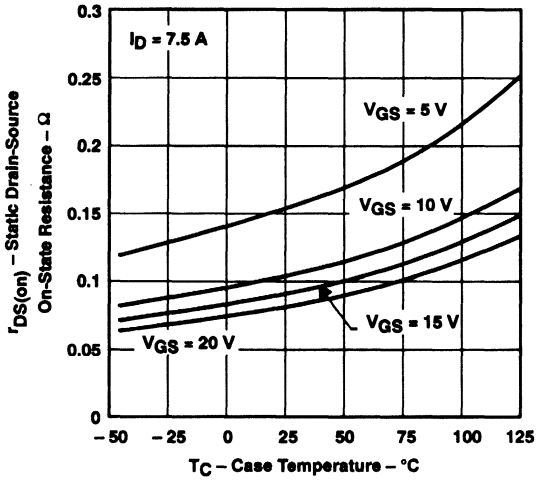


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

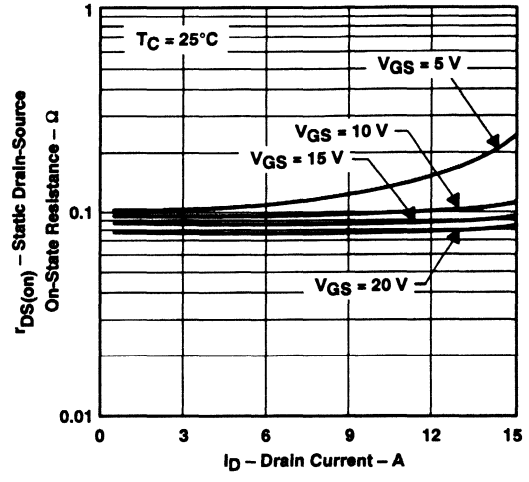


Figure 6

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

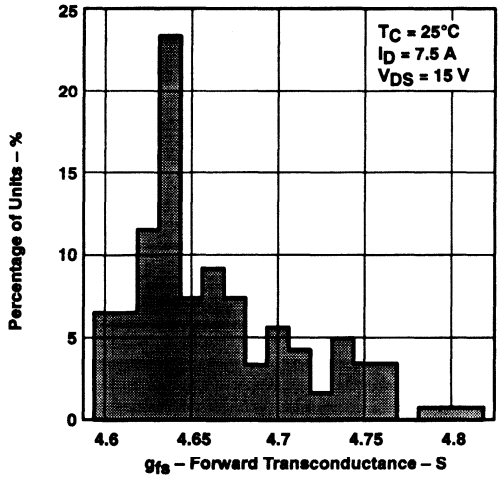


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

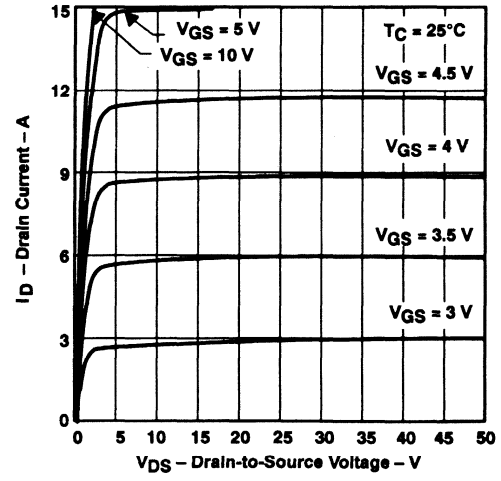


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE vs CASE TEMPERATURE

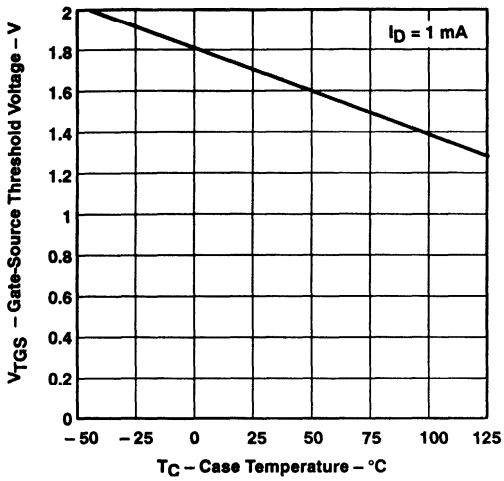


Figure 9

SOURCE-DRAIN DIODE CURRENT vs SOURCE-DRAIN VOLTAGE

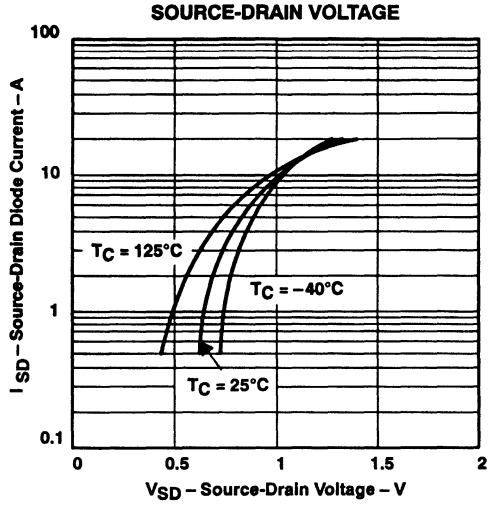


Figure 10

GATE-SOURCE VOLTAGE vs GATE CHARGE

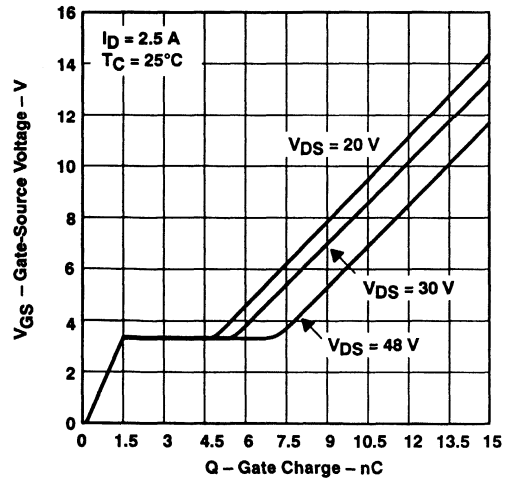


Figure 11

REVERSE RECOVERY TIME vs REVERSE dI/dt

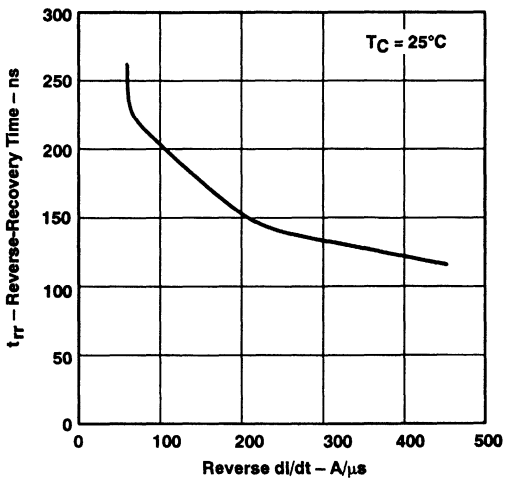


Figure 12

TYPICAL CHARACTERISTICS

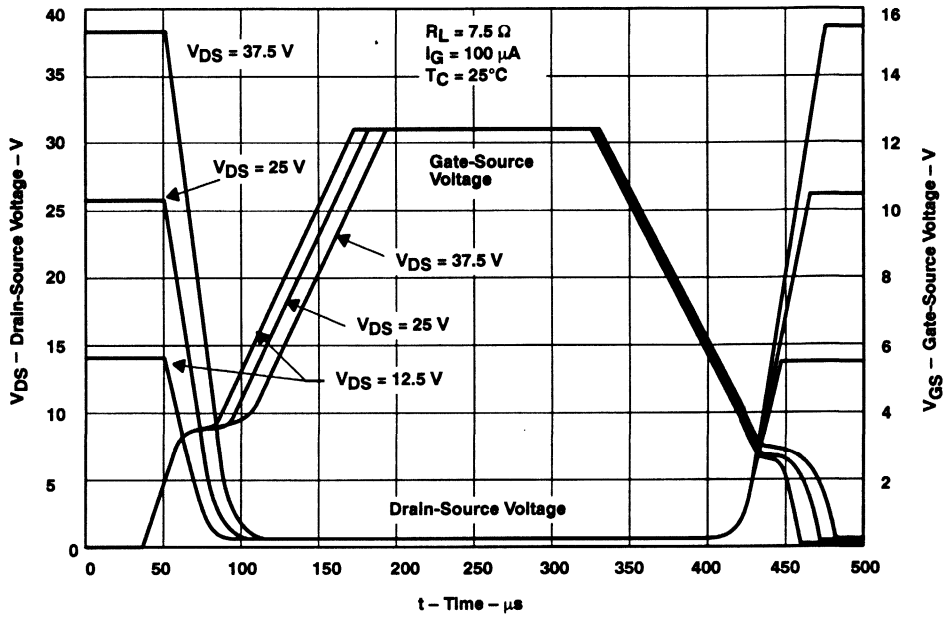


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-SOURCE VOLTAGE

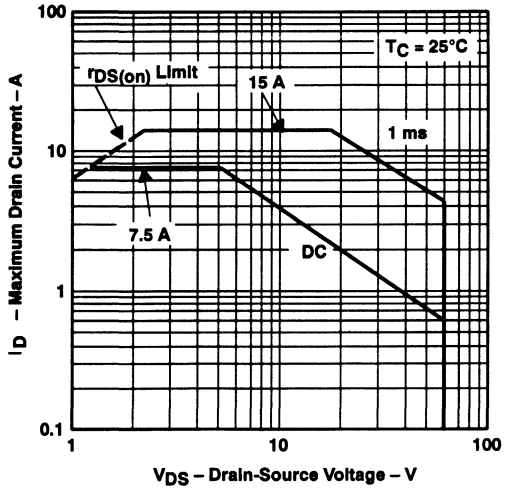


Figure 14

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

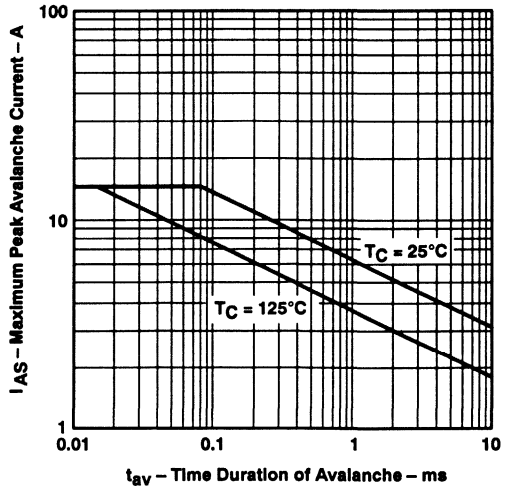
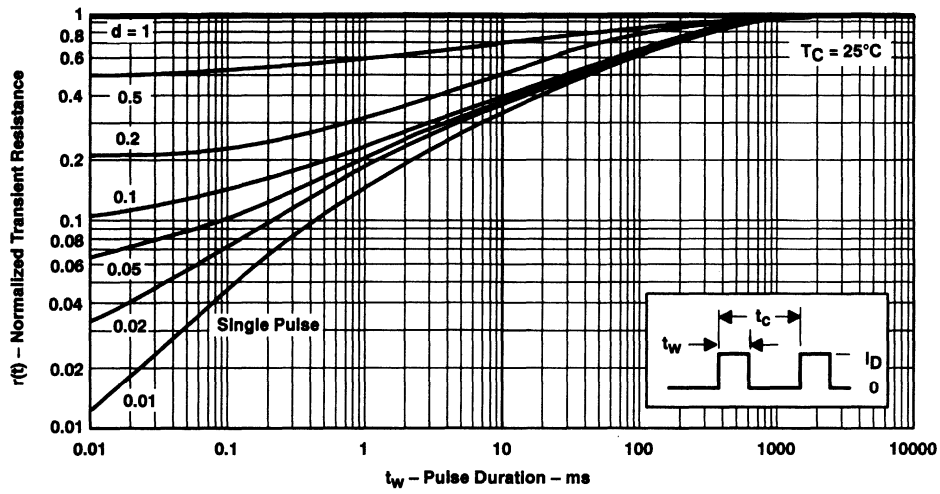


Figure 15

THERMAL INFORMATION

NORMALIZED TRANSIENT THERMAL IMPEDANCE
vs
SQUARE-WAVE PULSE DURATION



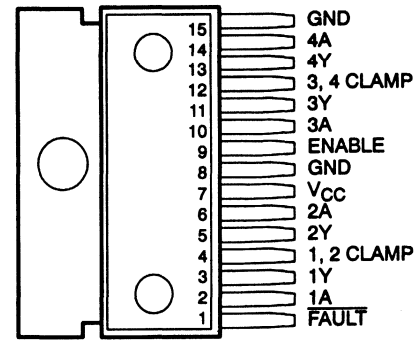
NOTES: $Z_{\theta JC}(t) = r(t)\ R_{\theta JC}$
t_w = pulse duration
t_c = period
d = duty cycle = t_w/t_c

Figure 16

SLIS007A – D3299, AUGUST 1989 – REVISED MAY 1993

- **1-A Current Capability Per Channel**
- **45-V Inductive Switching Voltage Capability**
- **Current Sink Inputs Compatible With TTL or CMOS Devices**
- **Output Clamp Diodes for Inductive Transient Protection**
- **Independent Thermal Shutdown Protection**
- **Overvoltage Shutdown Protection**
- **Independent Channel Current Limit**
- **Error Sensing**
- **Extended Temperature Range of –40°C to 125°C**

KN PACKAGE
(TOP VIEW)



The tab is electrically connected to the GND pins.

description

The TPIC2404 is a monolithic high-voltage high-current quadruple low-side switch especially designed for driving from low-level logic to peripheral loads such as relays, solenoids, motors, lamps, and other high-voltage high-current loads. The high-efficiency power switch is optimized for applications where a very rugged power switch is required. The device tolerates power supply transients and reverse battery conditions up to 13 V.

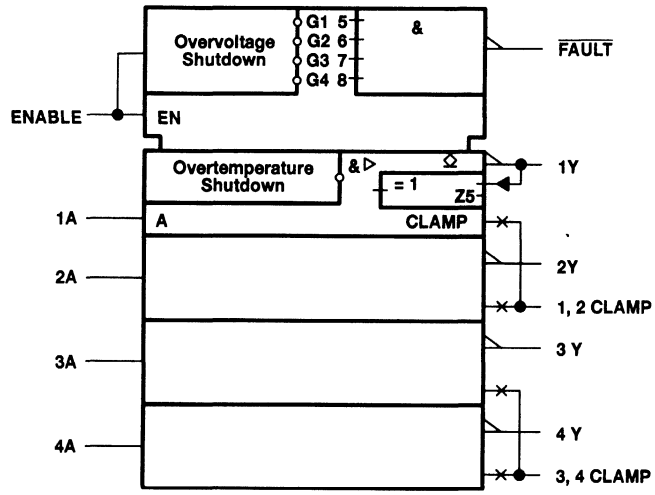
The TPIC2404 features four inverting open-collector outputs controlled by a common-enable input. When ENABLE is low, the outputs are disabled. An error-sensing circuit monitors load and device faults. When an error is sensed, the $\overline{\text{FAULT}}$ output goes to a low state. In addition, the device features on-board V_{CC} overvoltage and thermal overload protection circuits, and the outputs are current limit protected.

FUNCTION TABLE

	INPUTS		OUTPUTS	
	ENABLE	A	Y	$\overline{\text{FAULT}}$
Normal operation	H	H	L	H
	H	L	H	H
	L	X	H	H
Open load	H	L	L	L
	H	H	L	H
Short to GND	H	L	L	L
	H	H	L	H
Overvoltage shutdown	H	H	H	L
	H	L	H	H
Thermal shutdown	H	H	H	L
	H	L	H	H
Short to V_{CC}	H	H	H	L
	H	L	H	H

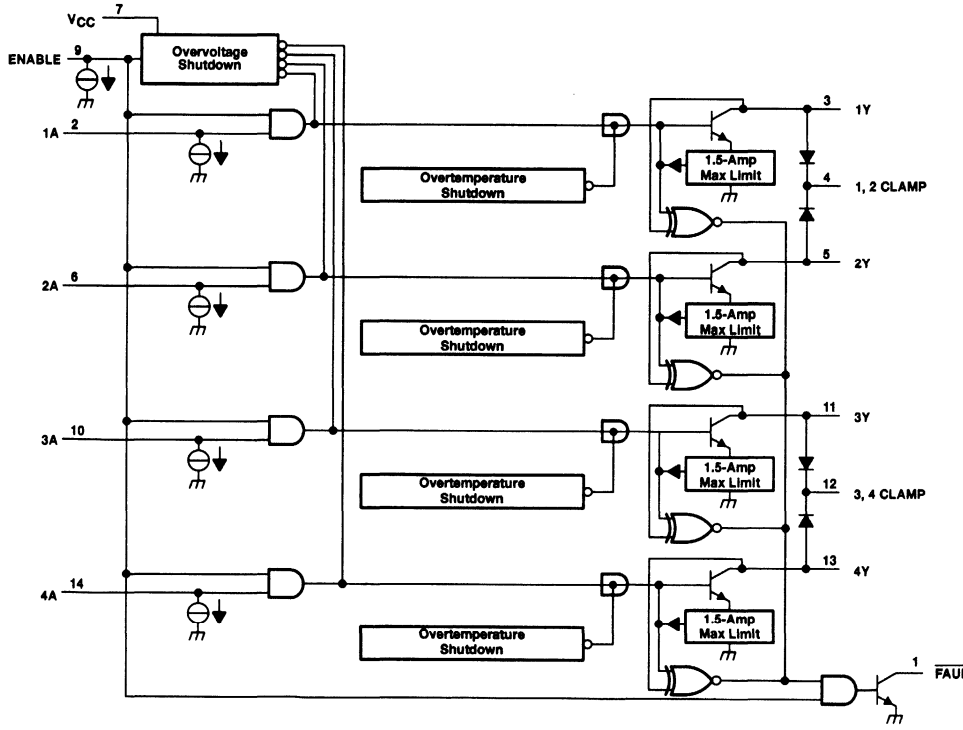
H = high level, L = low level, X = irrelevant

logic symbol†

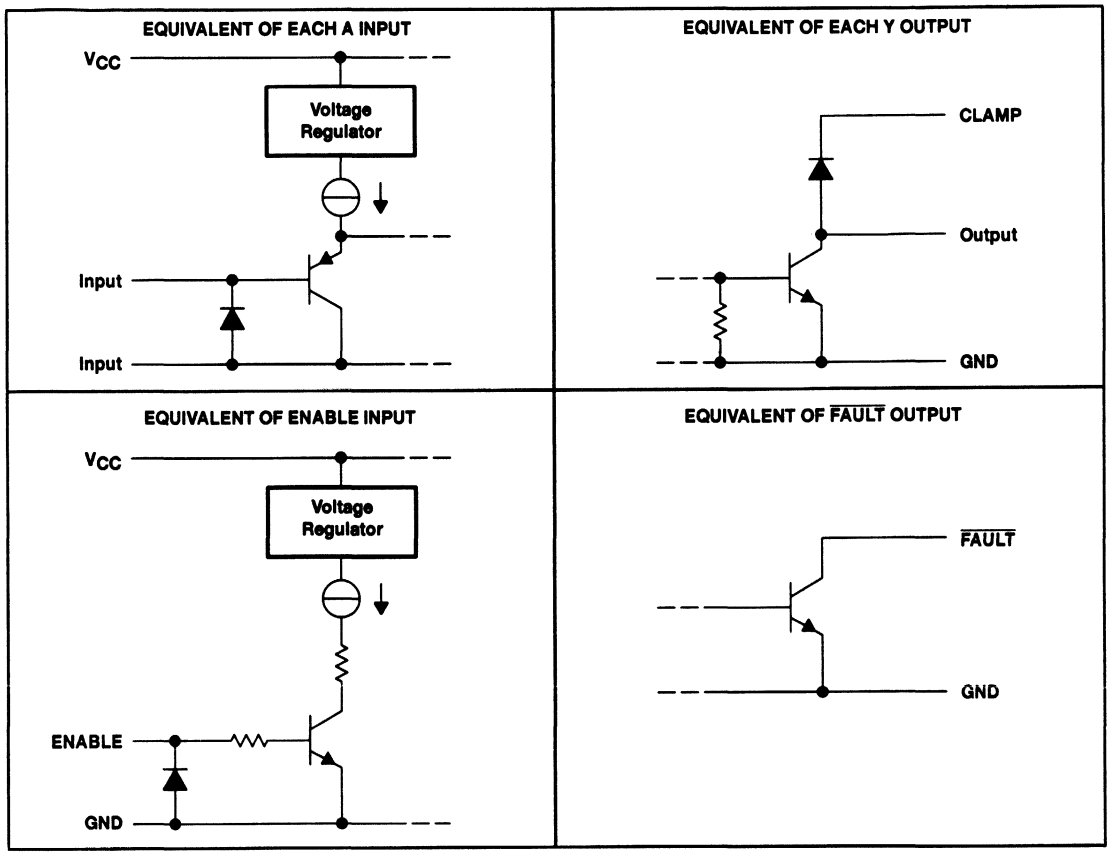


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −13 V to 24 V
Input voltage range, V_I ..... −0.6 V to 7 V
Output voltage range, V_O (see Note 2) ..... −0.6 V to 45 V
Output sustaining voltage, $V_{O(sust)}$ ..... 45 V
Continuous output sink current (repetitive, $t_w < 8$ ms), I_{OL} (see Note 3) ..... 1.5 A
Output clamp-diode voltage, V_{OK} ..... 45 V
Continuous total dissipation at (or below) 25°C case temperature (see Note 4) ..... 50 W
Operating case or virtual junction temperature range ..... −55°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network GND.
2. For a fault condition to be valid, the output voltage needs to be a minimum of 7 V.
3. Output sink current is limited by the overcurrent limit.
4. For operation above 25°C free-air or case temperature, refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below rated dissipation.

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

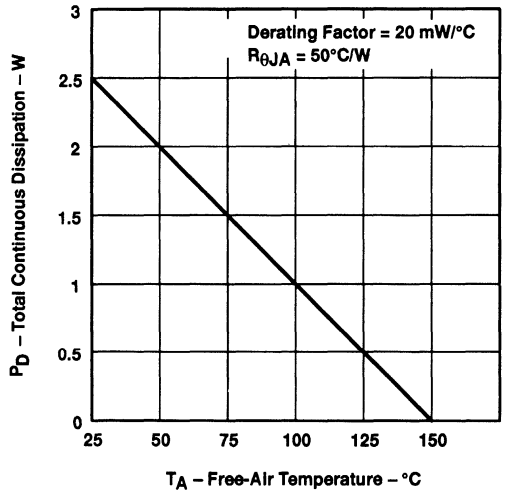


Figure 1

CASE TEMPERATURE DISSIPATION DERATING CURVE

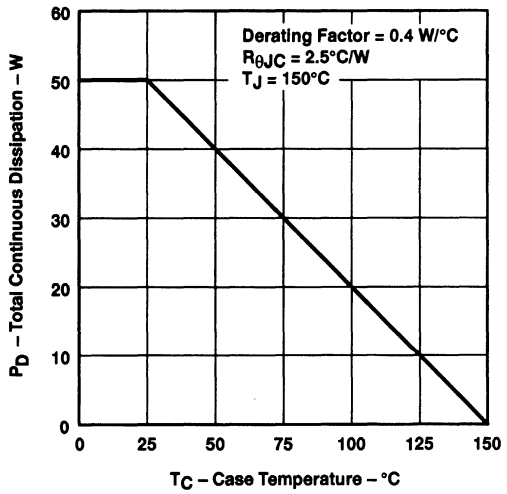


Figure 2

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	9	12	16	V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL}	−0.3†		0.8	V
Peak output voltage from external inductive kickback			45	V
Continuous output sink current			1	A
$\overline{FAULT}$ output sink current			75	μA
Operating free-air temperature, T_A	−40		125	°C

† The algebraic convention, in which the least positive (most negative) value is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
$I_{O(off)}$	Off-state output current		V_O = 12 V,	ENABLE low		15	100	μA
			V_O = 45 V,	ENABLE high		0.6	2	mA
			V_O = 12 V,	ENABLE high	200	400	600	μA
I_{IL}	Low-level input current		V_I = 0 to 0.8 V		−10	25	40	μA
I_{IH}	High-level input current	A inputs			10	25	60	μA
		ENABLE				0.2	1	mA
V_{OL}	Low-level output voltage		I_{OL} = 100 mA			0.1	0.15	V
			I_{OL} = 500 mA			0.3	0.55	
			I_{OL} = 1 A			0.8	1.3	
			$\overline{FAULT}$ output,	I_{OL} = 30 μA		0.2	0.4	
I_{OL}	Low-level output current		$\overline{FAULT}$ output,	V_{OL} = 1 V to 5.5 V	50	90	125	μA
$I_{R(K)}$	Clamp-diode reverse current		V_r = 50 V,	V_O = 0			100	μA
$V_{F(K)}$	Clamp-diode forward voltage		I_f = 1 A				2	V
			I_f = 1.5 A				2.5	
I_{CC}	Supply current		Outputs off,	ENABLE low			0.25	mA
			Outputs on,	T_A = −40°C			120	
			Outputs on,	T_A = 25°C to 125°C			100	

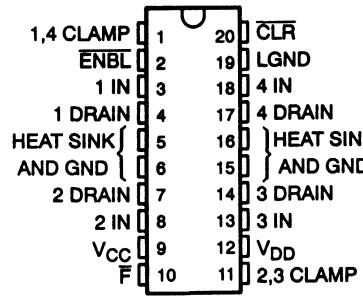
operating characteristics over recommended operating free-air temperature and supply voltages (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
High-level output sense voltage threshold				7	V
Low-level output sense voltage threshold		3			V
Overvoltage shutdown		25.5		31	V
Overvoltage shutdown hysteresis			0.25		V
Overcurrent limiting	T_A = −40°C			1.85	A
	T_A = 25°C to 125°C		1.2	1.5	
Thermal shutdown			155		°C
Thermal shutdown hysteresis			15		°C
Turn-on time			8		μs
Turn-off time			8		μs

‡ All typical values are at V_{CC} = 12 V, T_A = 25°C.

- **Output Voltage up to 60 V**
- **Four Output Channels of 700-mA Nominal Current Per Channel**
- **Pulsed Current . . . 3 A Per Channel**
- **Low $r_{DS(on)}$ . . . 0.5 Ω Typ**
- **Avalanche Energy . . . 50 mJ**
- **Thermal Shutdown Protection With Fault (Overtemperature) Output**
- **NE Package Designed for Heat Sinking**
- **Integral Output Clamp Diodes**
- **Input Transparent Latches for Data Storage**
- **Asynchronous Clear to Turn off All Outputs**
- **Output Parallel Capability for Increased Current Drive up to 12-A Total Pulsed Load Current**

NE PACKAGE
(TOP VIEW)



description

The TPIC2406 is a monolithic, high-voltage, high-current, quadruple power driver designed for use in systems that require high load power. The device contains built-in high-speed output clamp diodes for inductive transient protection. Power driver applications include lamps, relays, solenoids, and dc stepping motors.

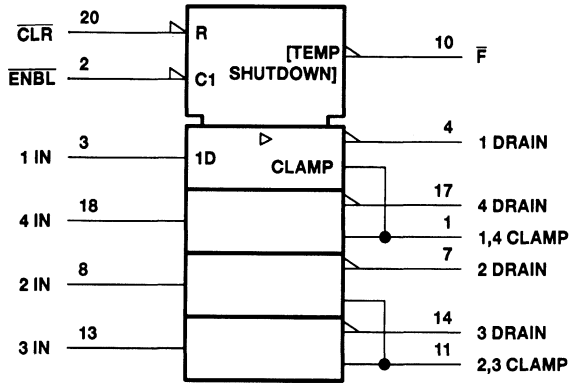
FUNCTION TABLE
(each channel)

FUNCTION	INPUTS			OUTPUT	FAULT
	ENBL	CLR	IN	Y	F
Normal Operation	X	L	X	H	H
	L	H	L	H	H
	L	H	H	L	H
	H	H	X	Q_0	H
Thermal Shutdown	X	X	X	H	L

H = high-level, L = low-level, X = irrelevant

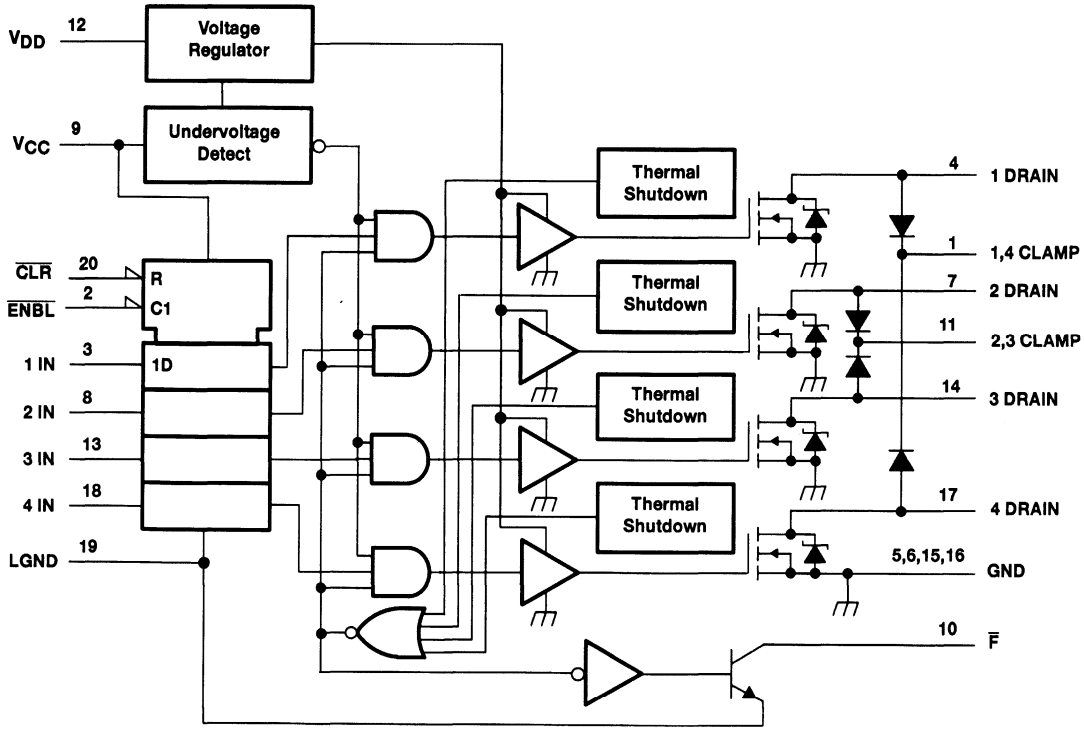
The device features four inverting open-drain outputs, each controlled by an input storage latch with common clear and enable controls. All inputs accept standard TTL- and CMOS-logic levels. The CLR function is asynchronous and turns all four outputs off regardless of data inputs. Taking ENBL low puts the input latch into a transparent mode, allowing the data inputs to affect the output. In this state, all four outputs are held off while CLR is low, but return to the stages on the data inputs when CLR goes high. When ENBL is taken high, the latch is put into a storage mode and the last state of the data inputs is held in the latches. If CLR is taken low, the data in the latches is cleared and all outputs are turned off. If CLR is taken high again, ENBL must be cycled low to read new data into the latch.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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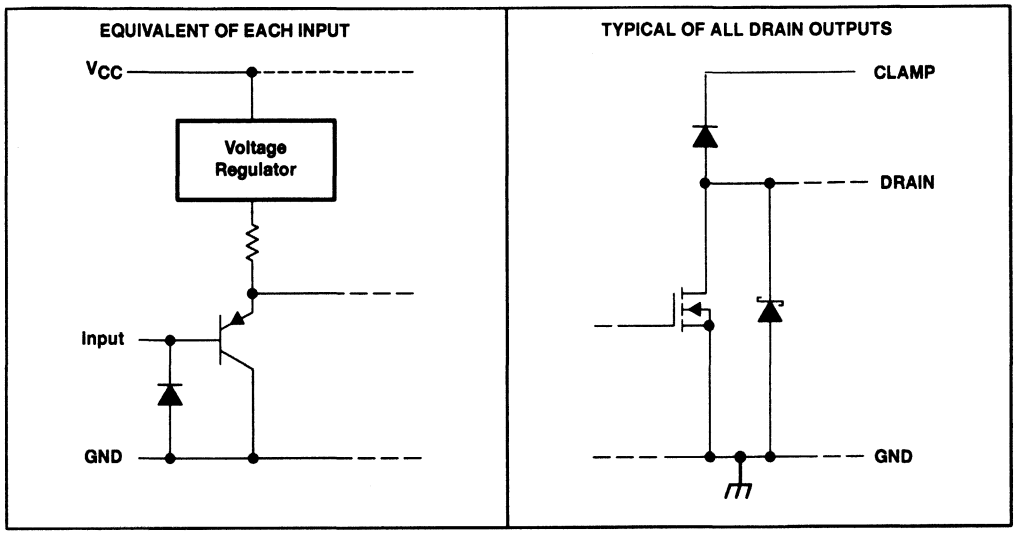
schematics of inputs and outputs



absolute maximum ratings over –40°C to 125°C case temperature range (unless otherwise noted)

Logic supply voltage, V_{CC} (see Note 1)	7 V
Power MOSFET driver supply voltage, V_{DD}	60 V
Logic input voltage, V_I	7 V
Power MOSFET drain-source voltage, V_{DS}	60 V
Output voltage at $\overline{F}$, V_O	7 V
Clamp-diode voltage	60 V
Continuous source-drain diode anode current	1.25 A
Pulsed source-drain diode anode current	6 A
Pulsed drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, $T_A = 25°C$ (see Note 2 and Figures 5 through 8)	3 A
Continuous drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, $T_A = 25°C$	770 mA
Peak drain current, single output, I_{DM}, $T_A = 25°C$ (see Note 3)	12.5 A
Single-pulse avalanche energy, E_{AS}	50 mJ
Continuous total dissipation at or below 25°C free-air temperature (see Note 4)	2.5 W
Continuous total dissipation at or below 100°C case temperature (see Note 4)	6 W
Operating junction temperature range, T_J	–40°C to 150°C
Storage temperature range	–40°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to the five ground (GND and LGND) terminals connected together.
2. Pulse duration = 10 ms, duty cycle = 6%.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 20 mW/°C. For operation above 100°C case temperature, derate linearly at the rate of 120 mW/°C. To avoid exceeding the design maximum junction temperature, these ratings should not be exceeded. Due to variations in individual devices, electrical characteristics, and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Logic supply voltage, V_{CC}		4.5		5.5	V
Output supply voltage, V_{DD}		10		35	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.6	V
Setup time, data before $\overline{ENBL}$ ↑, t_{su} (see Figure 1)		100			ns
Hold time, data after $\overline{ENBL}$ ↑, t_h (see Figure 1)		100			ns
Pulse duration, t_w (see Figure 1)	$\overline{ENBL}$ low	300			ns
	$\overline{CLR}$ low				
Operating case temperature, T_C		−40		125	°C

electrical characteristics, V_{CC} = 5 V, V_{DD} = 14 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		60			V
$V_{F(K)}$	Clamp-diode forward voltage	I_F = 1.25 A,	See Notes 5 and 6			1.6	V
V_{SD}	Source-drain diode forward voltage	I_S = 1.25 A,	See Notes 5 and 6			1.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OL}	Low-level output voltage at $\overline{F}$	I_{OL} = 4 mA			0.4		V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0.4 V			0.1	mA
I_{CC}	Logic supply current	I_O = 0,	All outputs off			10	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, See Notes 5, 6, and 7	$I_N = I_D$, T_C = 85°C,		700		mA
I_{DD}	Output supply current	I_O = 0,	All outputs off			6	mA
$I_{R(K)}$	Clamp-diode reverse current	V_{DS} = 55 V,	V_O = 0			1	μA
		V_{DS} = 55 V,	V_O = 0, T_C = 125°C			10	
I_{DSX}	Off-state drain current	V_R = 55 V				1	μA
		V_R = 55 V,	T_C = 125°C			10	
$I_{O(F)}$	High-level fault leakage current	V_{OH} = 5.5 V				1	μA
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 1.25 A	See Notes 5 and 6		0.5	0.6	Ω
		I_D = 1.25 A, T_C = 125°C			0.8	1	
		I_D = 3 A			0.55	0.65	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at 85°C case temperature.

switching characteristics, V_{CC} = 5 V, V_{DD} = 24 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level drain output from clock	C_L = 30 pF,	See Figure 1		450		ns
t_{PHL}	Propagation delay time, high-to-low-level drain output from clock				550		ns
t_{TLH}	Transition time, low-to-high-level of source-drain output				35		ns
t_{THL}	Transition time, high-to-low-level of source-drain output				30		ns
t_{PLH}	Propagation delay time, low-to-high-level drain output from input	C_L = 30 pF, I_D = I_N = 700 mA	See Figure 2,		380		ns
t_{PHL}	Propagation delay time, high-to-low-level drain output from input				380		ns
t_r	Rise time, low-to-high-level of source-drain output				35		ns
t_f	Fall time, high-to-low-level of source-drain output				70		ns
t_a	Reverse-recovery-current rise time	I_F = 3 A, See Notes 5 and 6,	di/dt = 100 A/µs, See Figure 3		45		ns

NOTES: 5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

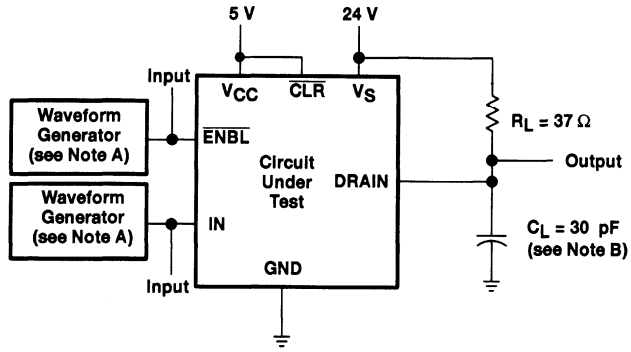
thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance	All four outputs with equal power			8.33	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance				50	

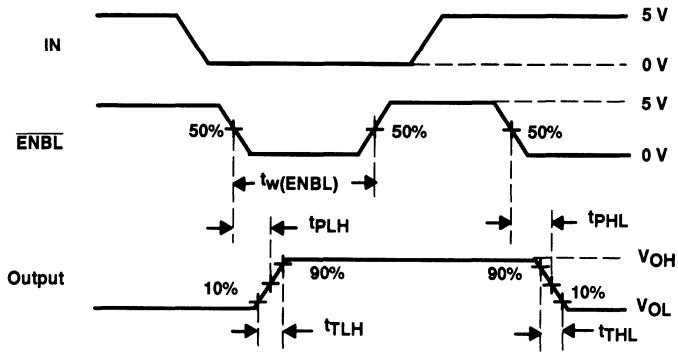
operating characteristics over –40°C to 125°C case temperature range

PARAMETER	MIN	TYP	MAX	UNIT
Undervoltage shutdown	3		4.5	V
Thermal shutdown temperature		155		°C
Thermal shutdown hysteresis		15		°C

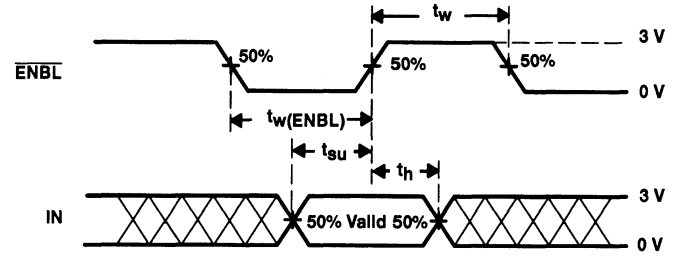
PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT



(b) SWITCHING TIMES FROM ENABLE INPUT

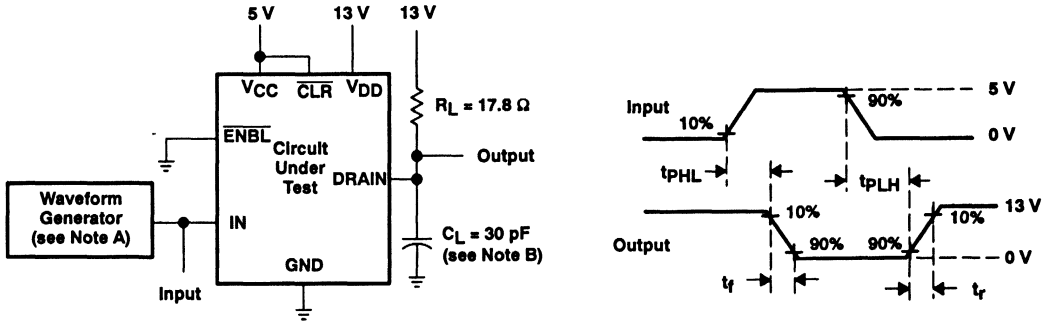


(c) INPUT SETUP AND HOLD WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

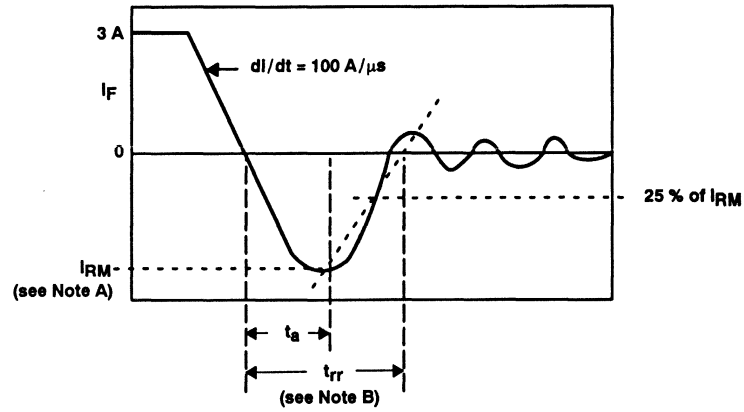


(a) TEST CIRCUIT

(b) VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 5$ ms, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

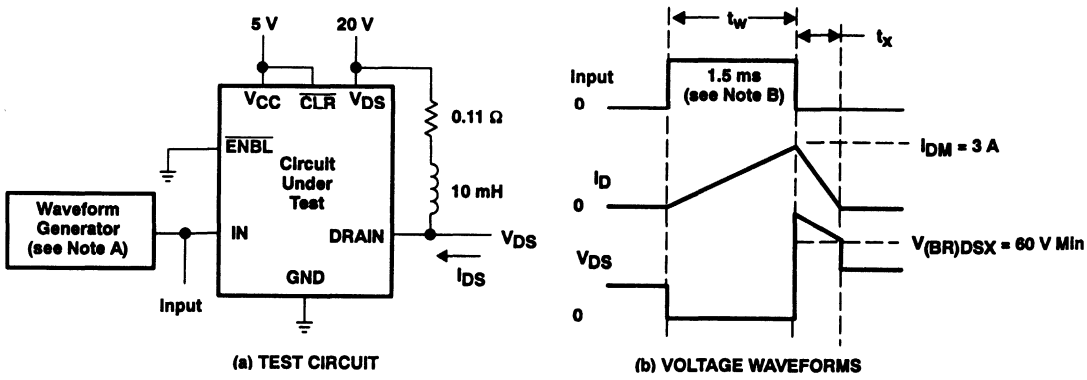
Figure 2. Test Circuit and Voltage Waveforms



NOTES: A. I_{RM} = maximum recovery current.
B. t_{rr} = reverse recovery time.

Figure 3. Reverse-Recovery-Current Waveforms of Source-Drain Diode

PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT (b) VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 1$ ms, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{DM} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{DM} \times V_{(BR)DSX} \times t_x}{2} = 50$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

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MAXIMUM RATINGS

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

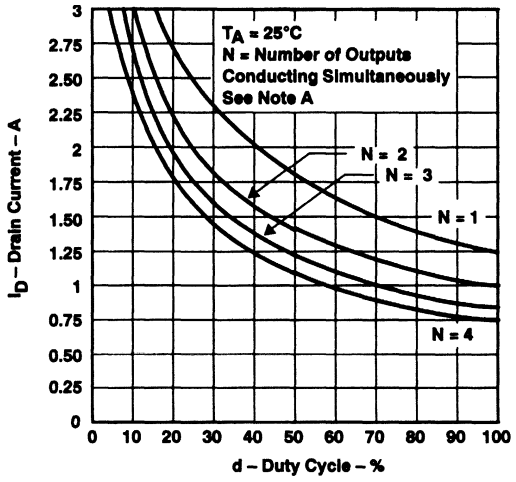


Figure 5

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

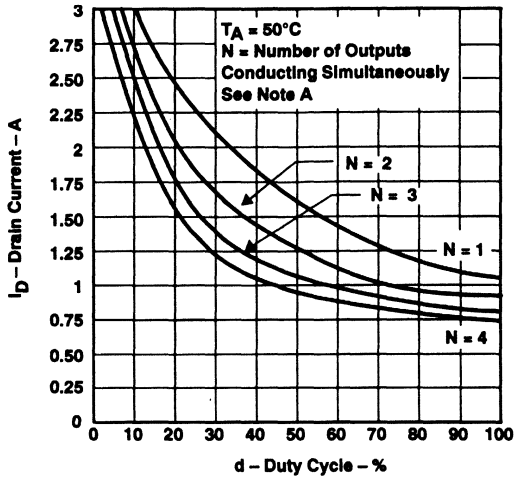


Figure 6

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

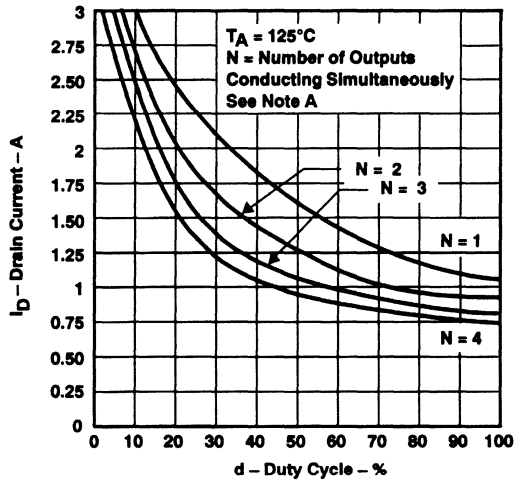


Figure 7

MAXIMUM DRAIN CURRENT
vs
PULSE DURATION

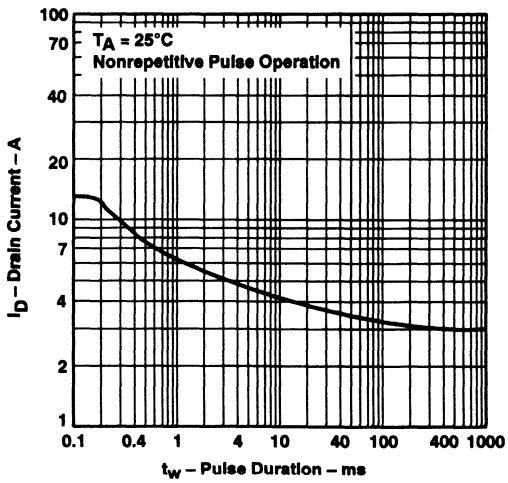
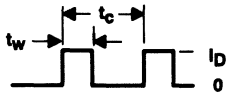


Figure 8

NOTE A: For Figures 5, 6, and 7, $d = \frac{t_W}{t_C} = \frac{10\ ms}{t_C}$, where t_W and t_C are defined by the following:



MAXIMUM RATINGS

MAXIMUM CONTINUOUS DRAIN CURRENT
vs
FREE-AIR TEMPERATURE

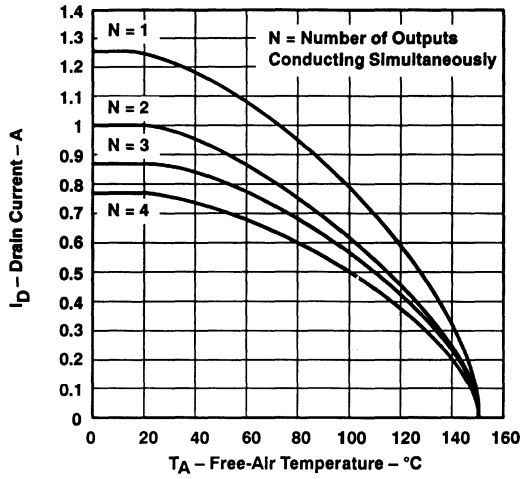
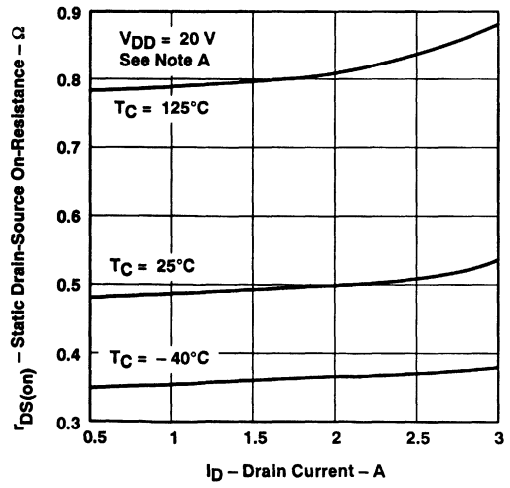


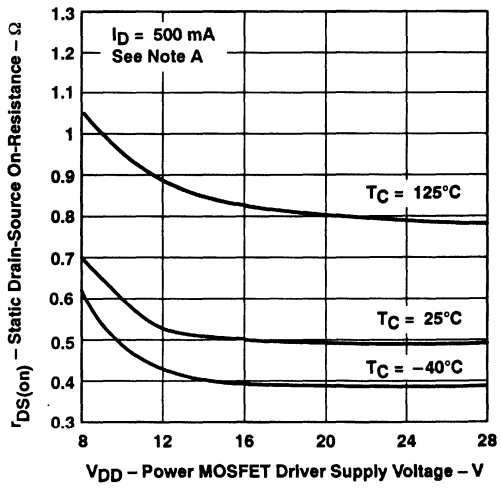
Figure 9

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-RESISTANCE
vs
DRAIN CURRENT



STATIC DRAIN-SOURCE ON-RESISTANCE
vs
POWER MOSFET DRIVER SUPPLY VOLTAGE



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 10

Figure 11

THERMAL INFORMATION

FREE-AIR TEMPERATURE DISSIPATION DERATING CURVE

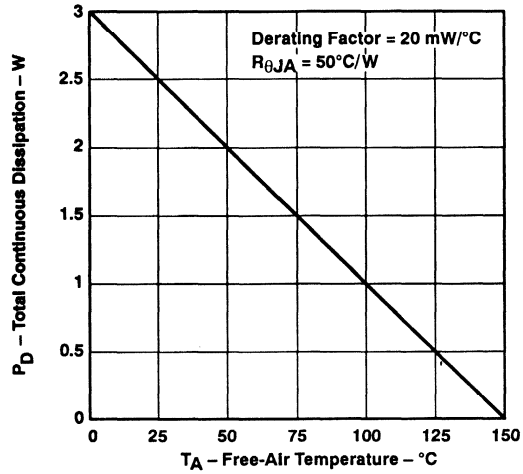


Figure 12

TRANSIENT THERMAL IMPEDANCE vs ON TIME

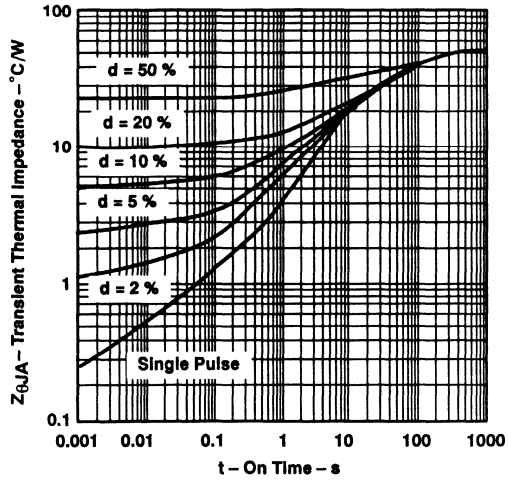


Figure 13

The single-pulse curve in Figure 11 represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta_{JA}} = \left| \frac{t_w}{t_c} \right| R_{\theta_{JA}} + \left| 1 - \frac{t_w}{t_c} \right| Z_{\theta(t_w + t_c)} + Z_{\theta(t_w)} - Z_{\theta(t_c)}$$

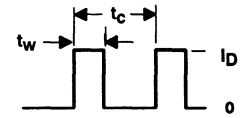
Where:

$Z_{\theta(t_w)}$ = the single-pulse thermal impedance for t = t_w seconds

$Z_{\theta(t_c)}$ = the single-pulse thermal impedance for t = t_c seconds

$Z_{\theta(t_w + t_c)}$ = the single-pulse thermal impedance for t = $t_w + t_c$ seconds

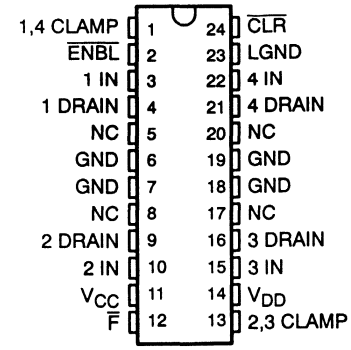
$d = t_w/t_c$



SGLS069 – D3378, FEBRUARY 1990 – REVISED JANUARY 1992

- **Output Voltage up to 60 V**
- **Four Output Channels of 300-mA Typical Current Per Channel**
- **Pulsed Current . . . 1 A Per Channel**
- **Low $r_{DS(on)}$ . . . 0.5 Ω Typ**
- **Thermal Shutdown Protection With Fault (Overtemperature) Output**
- **Integral Output Clamp Diodes**
- **Input Transparent Latches for Data Storage**
- **Asynchronous Clear to Turn off All Outputs**
- **Output Parallel Capability for Increased Current Drive up to 4-A Total Pulsed Load Current**

J PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPIC2406M is a monolithic, intelligent-power quad MOSFET latch designed for use in systems that require high load power. The device contains built-in high-speed output clamp diodes for inductive transient protection. Power driver applications include lamps, relays, solenoids, and dc stepping motors.

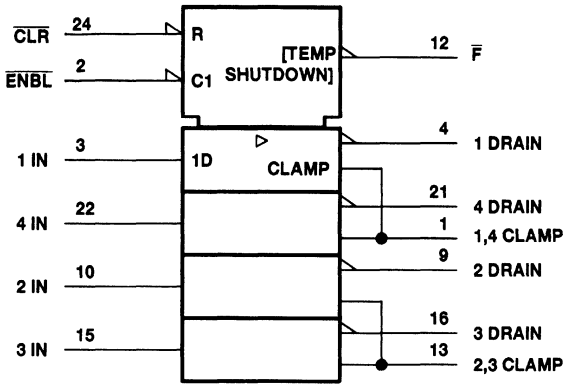
The device features four inverting open-drain outputs, each controlled by an input storage latch with common clear and enable controls. All inputs accept standard TTL- and CMOS-logic levels. The $\overline{CLR}$ function is asynchronous and turns all four outputs off regardless of data inputs. Taking $\overline{ENBL}$ low puts the input latch into a transparent mode, allowing the data inputs to affect the output. In this state, all four outputs are held off while $\overline{CLR}$ is low, but return to the stages on the data inputs when $\overline{CLR}$ goes high. When $\overline{ENBL}$ is taken high, the latch is put into a storage mode and the last state of the data inputs is held in the latches. If $\overline{CLR}$ is taken low, the data in the latches is cleared and all outputs are turned off. If $\overline{CLR}$ is taken high again, $\overline{ENBL}$ must be cycled low to read new data into the latch.

FUNCTION TABLE
(each channel)

FUNCTION	INPUTS			OUTPUT	FAULT
	$\overline{ENBL}$	$\overline{CLR}$	IN	Y	$\overline{F}$
Normal Operation	X	L	X	H	H
	L	H	L	H	H
	L	H	H	L	H
	H	H	X	Q0	H
Thermal Shutdown	X	X	X	H	L

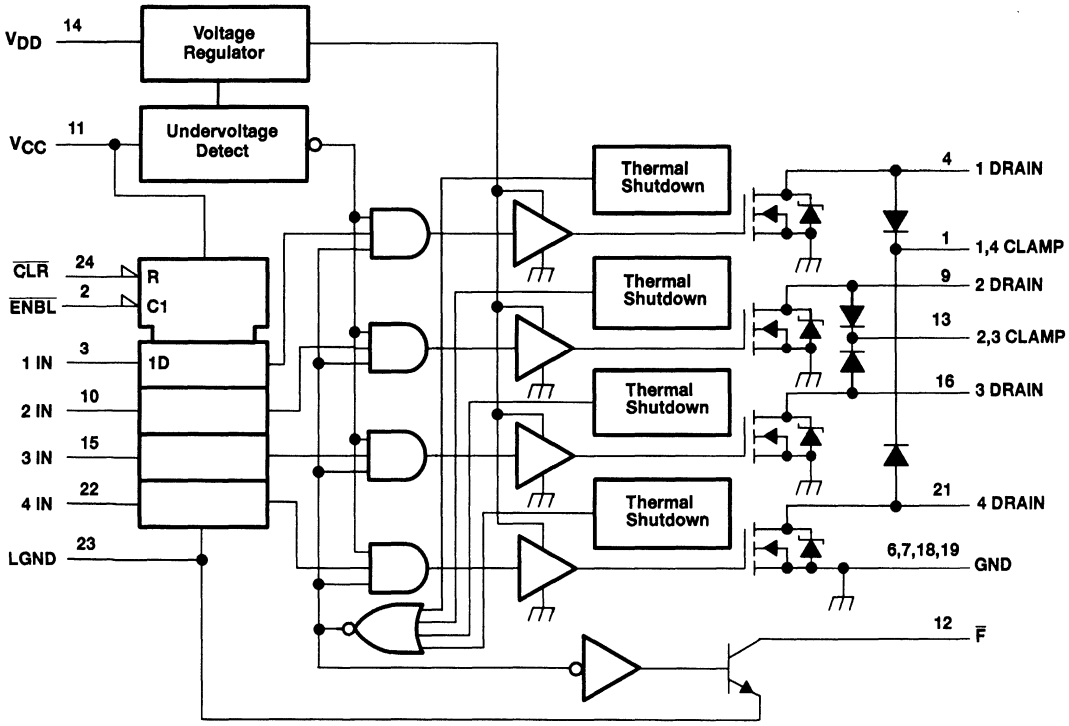
H = high level, L = low level, X = irrelevant

logic symbol†

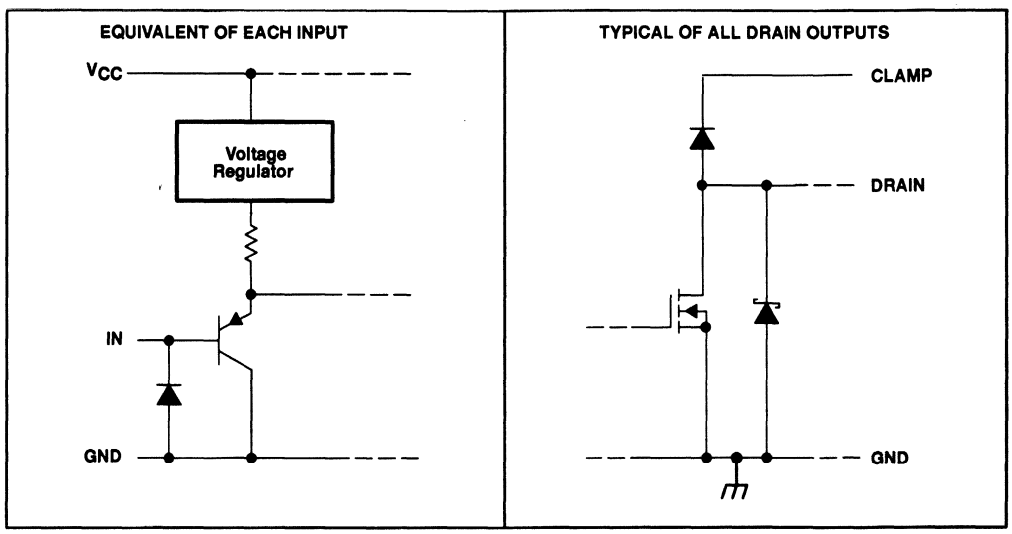


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{CC} (see Note 1)	7 V
Power MOSFET driver supply voltage, V_{DD}	60 V
Logic input voltage, V_I	7 V
Power MOSFET drain-source voltage, V_{DS}	60 V
Output voltage at $\overline{F}$, V_O	7 V
Clamp-diode voltage	60 V
Continuous source-drain diode anode current	300 mA
Pulsed source-drain diode anode current (see Note 2)	1 A
Pulsed drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, $T_A = 25°C$ (see Note 2)	1 A
Continuous drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, $T_A = 25°C$	300 mA
Continuous total dissipation at (or below) $T_A = 25°C$	1050 mW
Operating free-air temperature range, T_A	−55°C to 125°C
Storage temperature range	−55°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to the five ground (GND and LGND) terminals connected together.
2. Pulse duration ≤ 5 ms, duty cycle ≤ 6%

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC}		4.5	5.5	V
Output supply voltage, V_{DD}		10	35	V
High-level input voltage, V_{IH}		2		V
Low-level input voltage, V_{IL}			0.6	V
Setup time, data before $\overline{ENBL}$ ↑, t_{su} (see Figure 1)		100*		ns
Hold time, data after $\overline{ENBL}$ ↑, t_h (see Figure 1)		100*		ns
Pulse duration, t_w (see Figure 1)	$\overline{ENBL}$ low	300*		ns
	$\overline{CLR}$ low			
Operating free-air temperature, T_A		−55	125	°C

* These parameters are not production tested.

electrical characteristics over operating free-air temperature, V_{CC} = 5 V, V_{DD} = 14 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{BRDSX}	Drain-source breakdown voltage	I_D = 1 mA			60			V
$V_{F(K)}$	Clamp-diode forward voltage	I_F = 1 A,	See Note 2				1.8	V
V_{SD}	Source-drain diode forward voltage	I_S = 1 A,	See Note 2				1.5	V
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V,	I_I = −12 mA				−1.5	V
V_{OL}	Low-level output voltage at $\overline{F}$	I_{OL} = 4 mA				0.4		V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0.4 V				0.15	mA
I_{CC}	Logic supply current	I_O = 0,	All outputs off				10	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.225 V,	$I_N = I_D$			300		mA
I_{DD}	Output supply current	I_O = 0,	All outputs off				6	mA
$I_{R(K)}$	Clamp-diode reverse current	V_{DS} = 55 V,	V_O = 0,	T_A = 25°C			1	μA
		V_{DS} = 55 V,	V_O = 0				10	
I_{DSX}	Off-state drain current	V_R = 55 V,	T_A = 25°C				1	μA
		V_R = 55 V					10	
$I_{O(F)}$	High-level fault leakage current	V_{OH} = 5.5 V					1	μA
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 1 A,	T_A = 25°C	See Note 2		0.5	1	Ω
		I_D = 1 A				0.8	1.5	

NOTE 2: Pulse duration ≤ 5 ms, duty cycle ≤ 6%.

switching characteristics, V_{CC} = 5 V, V_{DD} = 24 V, T_A = 25°C (unless otherwise noted)

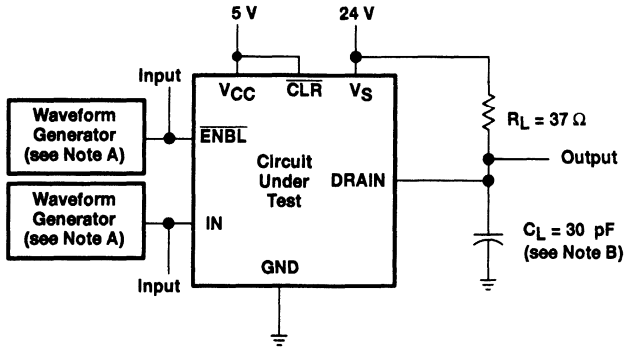
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level drain output from clock	C_L = 30 pF,	See Figure 1		450		ns
t_{PHL}	Propagation delay time, high-to-low-level drain output from clock				550		ns
t_{TLH}	Transition time, low-to-high-level of source-drain output				35		ns
t_{THL}	Transition time, high-to-low-level of source-drain output				30		ns
t_{DLH}	Delay time, low-to-high-level drain output from input	C_L = 30 pF, I_D = I_N = 700 mA,	T_A = Full range†, See Figure 2		380		ns
t_{DHL}	Delay time, high-to-low-level drain output from input				380		ns
$t_{r(LH)}$	Rise time, low-to-high-level of source-drain output				35		ns
$t_{f(HL)}$	Fall time, high-to-low-level of source-drain output				70		ns

† Full range is T_A = −55°C to 125°C.

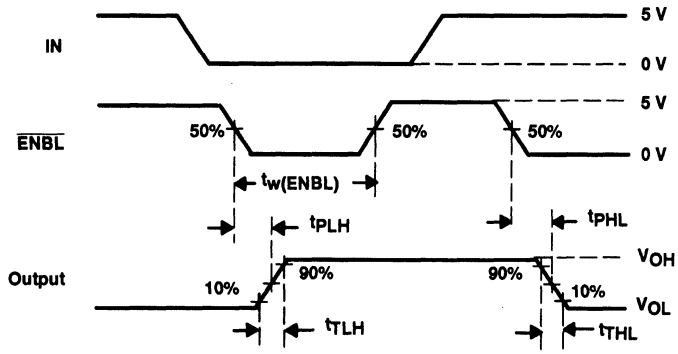
operating characteristics over operating free-air temperature range

PARAMETER	MIN	TYP	MAX	UNIT
Undervoltage shutdown	3		4.5	V
Thermal shutdown temperature		155		°C
Thermal shutdown hysteresis		15		°C

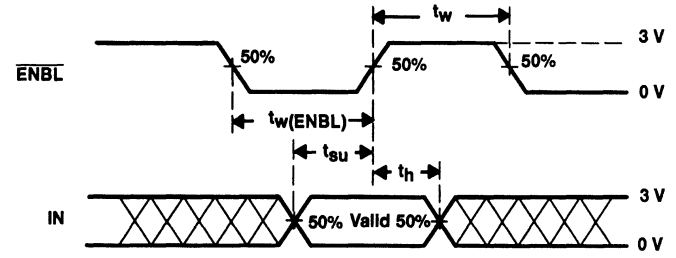
PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT



(b) SWITCHING TIMES FROM ENABLE INPUT

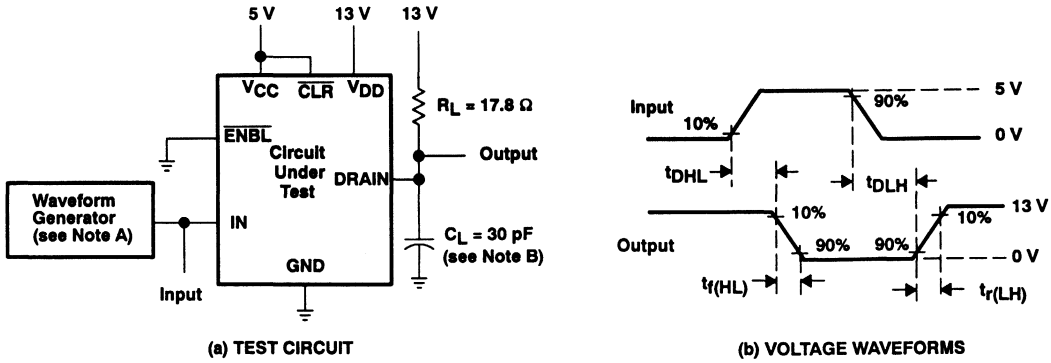


(c) INPUT SETUP AND HOLD WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Switching Times

PARAMETER MEASUREMENT INFORMATION



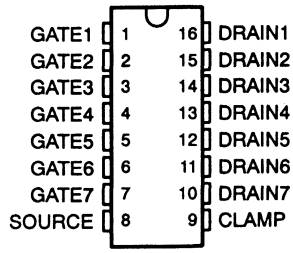
NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 5$ ms, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Switching Times

SLDS050A – D4044, SEPTEMBER 1992 – REVISED OCTOBER 1992

- **Seven 0.5-A Independent Output Channels**
- **Integrated Clamp Diode With Each Output**
- **Low $r_{DS(on)}$ . . . 0.5 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 3 A Per Channel**
- **Avalanche Energy . . . 22 mJ**

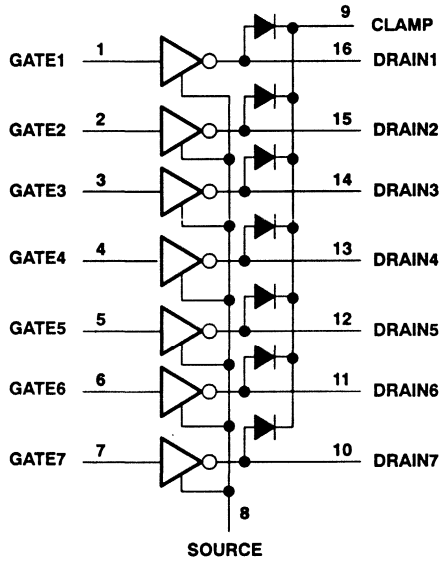
N PACKAGE
(TOP VIEW)



description

The TPIC2701 is a monolithic power DMOS transistor array that consists of seven independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains. The TPIC2701 is pin-for-pin functionally compatible with the Texas Instruments ULN2001A through ULN2004A.

logic diagram



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Gate-source voltage, V_{GS}	±20 V
Clamp-drain voltage, V_{CD}	60 V
Continuous source-drain diode current	0.5 A
Pulsed drain current, each output, I_D (see Note 1 and Figure 17)	3 A
Pulsed clamp current, I_{CL} (see Note 1 and Figure 18)	3 A
Continuous drain current, each output, all outputs on	0.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	22 mJ
Continuous total dissipation at (or below) T_A = 25°C (see Note 2)	1.4 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 11 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 μA, V_{GS} = 0		60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 0.5 A, V_{GS} = 15 V, See Notes 3 and 4			0.25	0.4	V
I_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{GS} = 0	T_C = 25°C		0.05	1	μA
			T_C = 125°C		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = −20 V, V_{DS} = 0			10	100	nA
$r_{DS(on)}$	Forward drain-source on-state resistance	V_{GS} = 15 V, I_D = 0.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C		0.5	0.8	Ω
			T_C = 125°C		0.8	1.3	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 0.5 A, See Notes 3 and 4		0.5	0.8		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz			105		pF
C_{oss}	Short-circuit output capacitance, common source				65		
C_{rss}	Short-circuit reverse transfer capacitance, common source				15		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts with a single output transistor conducting.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 0.5 A, V_{GS} = 0		0.9	1.4	V
$t_{rr(SD)}$	Reverse-recovery time	I_S = 0.5 A, V_{GS} = 0, V_{DS} = 48 V, di/dt = 25 A/μs, See Figure 1		165		ns
Q_{RR}	Total source-drain diode charge			250		nC

clamp diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_F	Forward on-voltage	I_F = 0.5 A		1	1.5	V
V_{BR}	Breakdown voltage	I_R = 1 μA	60			V
I_R	Reverse leakage current	V_R = 48 V		0.05	1	μA
$t_{rr(CD)}$	Reverse-recovery time	I_F = 0.1 A, di/dt = 25 A/μs, V_{CD} = 48 V, See Figure 1		90		ns
Q_{RR}	Total source-drain diode charge			100		nC

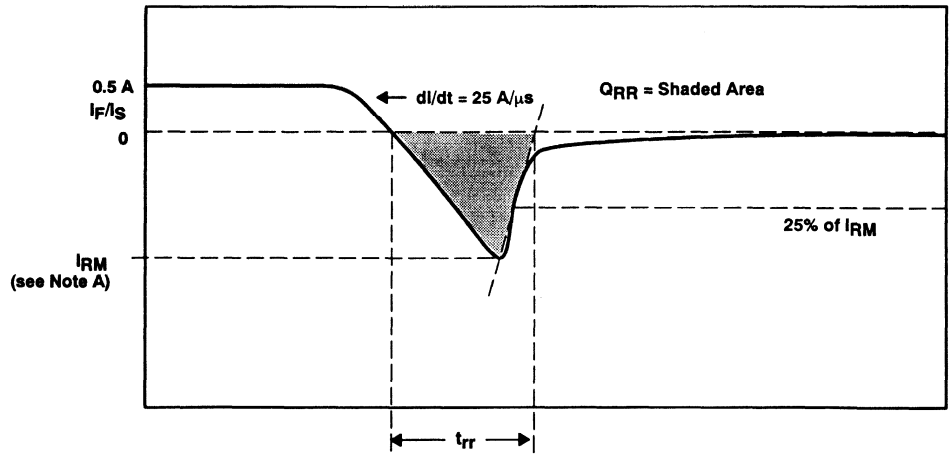
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 100 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		10		ns
$t_{d(off)}$	Turn-off delay time			30		
t_r	Rise time			15		
t_f	Fall time			5		
Q_g	Total gate charge	V_{DS} = 48 V, I_D = 0.25 A, V_{GS} = 10 V, See Figure 3		2.8	3.6	nC
Q_{gs}	Gate-source charge			1.6	2	
Q_{gd}	Gate-drain charge			1.2	1.6	

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			90	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain and Clamp Diodes

PARAMETER MEASUREMENT INFORMATION

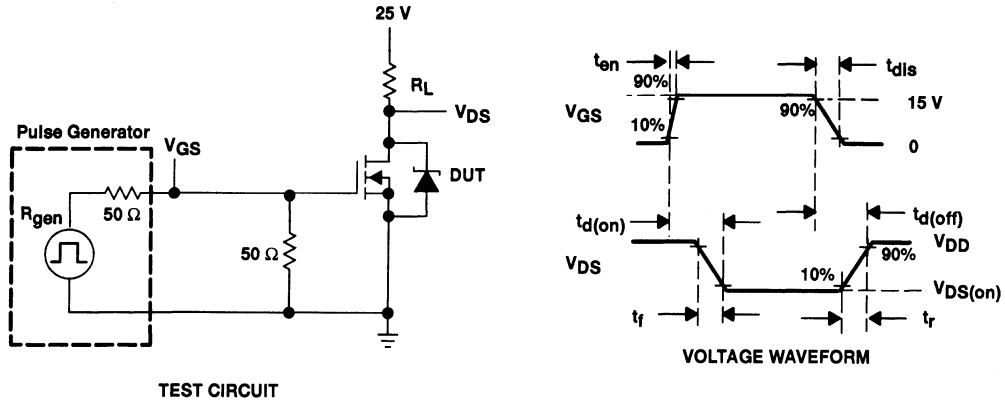


Figure 2. Resistive Switching

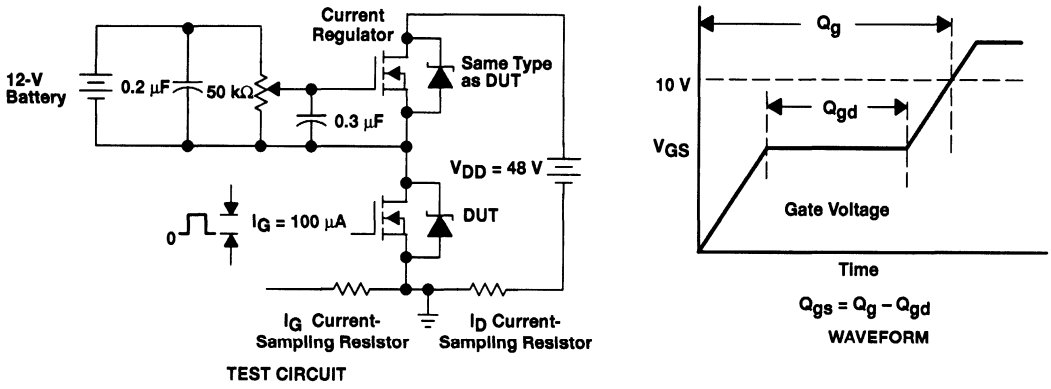
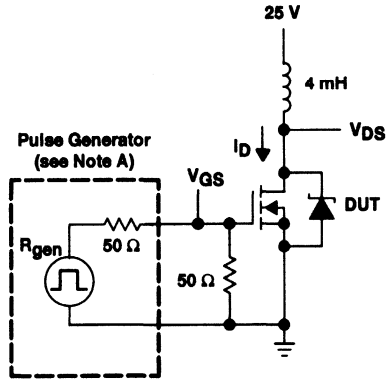
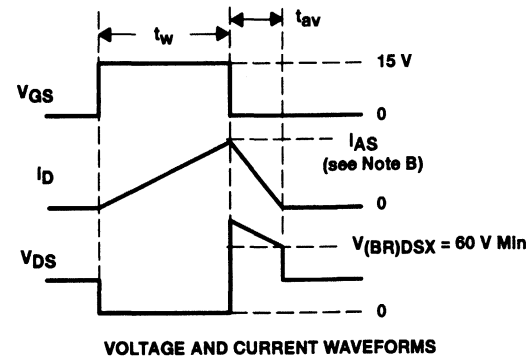


Figure 3. Gate Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 2.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 22$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

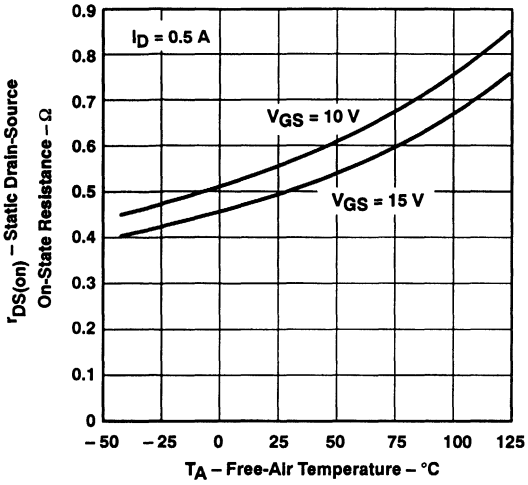


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

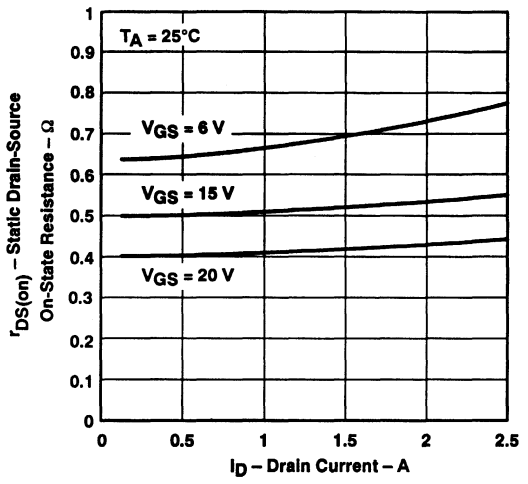


Figure 6

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

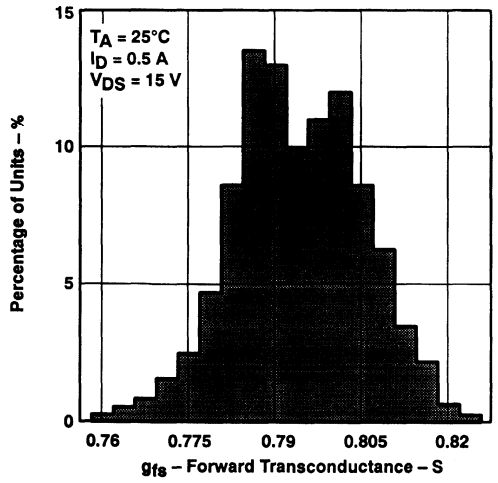


Figure 7

DRAIN-TO-SOURCE CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

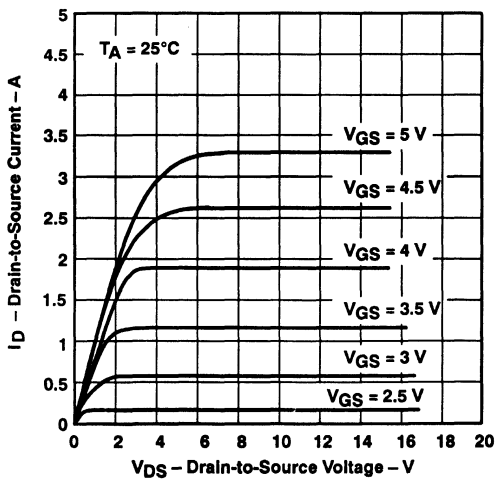


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

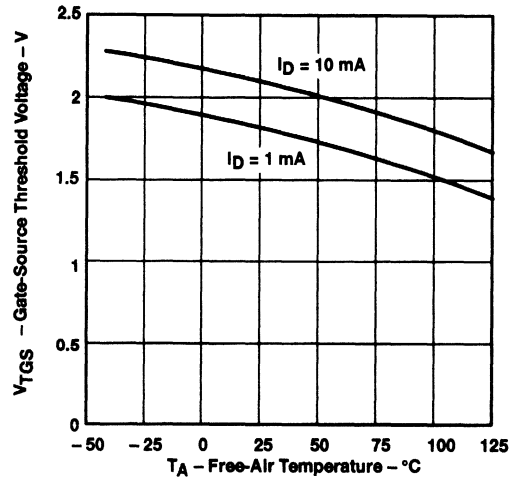


Figure 9

GATE-SOURCE VOLTAGE
vs
GATE CHARGE

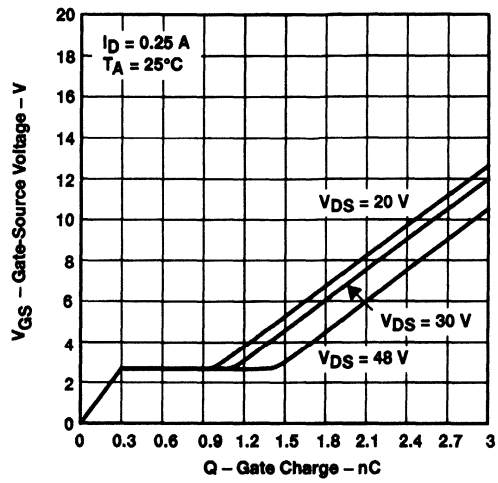


Figure 10

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN DIODE VOLTAGE

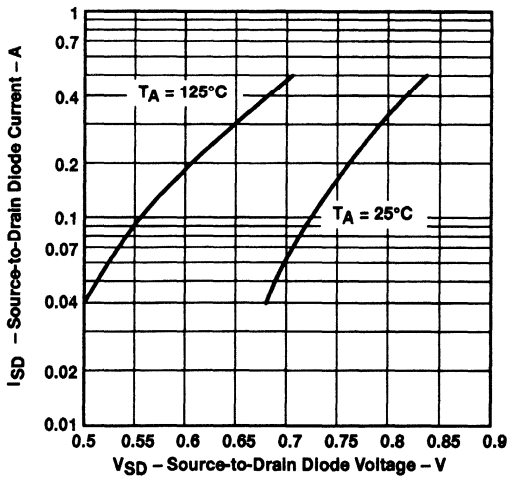


Figure 11

SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN DIODE VOLTAGE

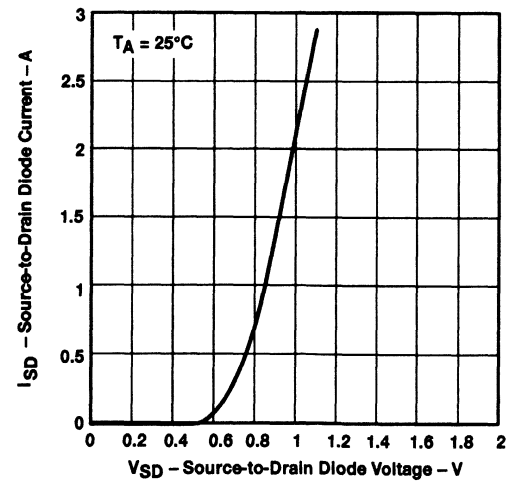


Figure 12

TYPICAL CHARACTERISTICS

CLAMP-DIODE CURRENT
vs
CLAMP-DIODE VOLTAGE

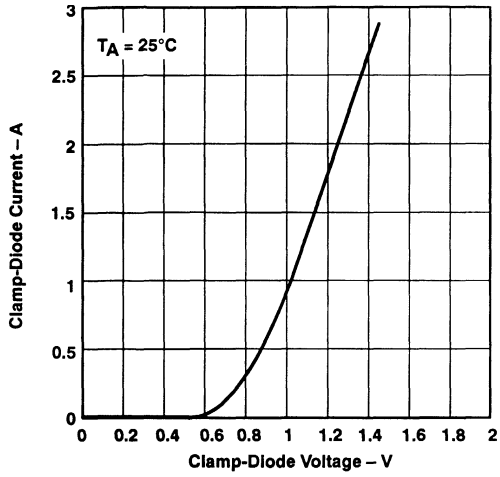


Figure 13

CLAMP-DIODE REVERSE RECOVERY TIME
vs
REVERSE dI/dt

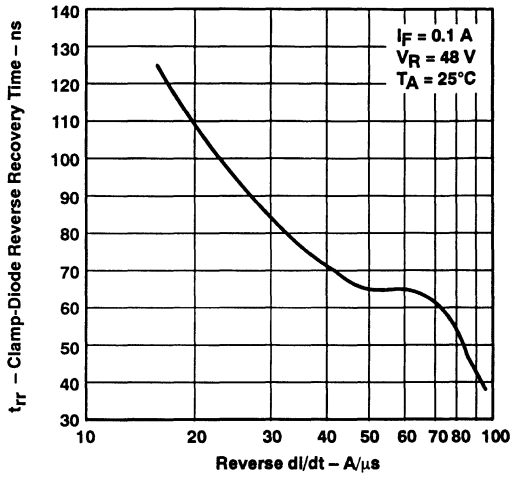
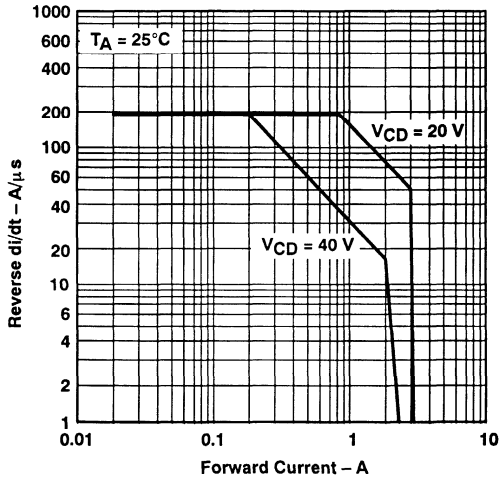


Figure 14

REVERSE di/dt
vs
FORWARD CURRENT



NOTE : $V_{CD} = V_{clamp} - V_{drain}$

Figure 15

TYPICAL CHARACTERISTICS

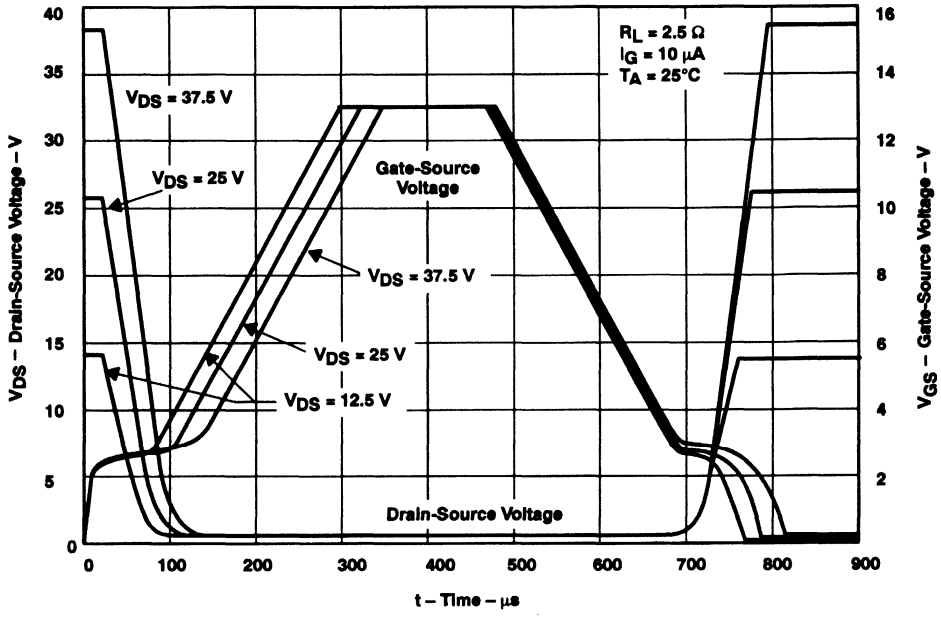


Figure 16. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

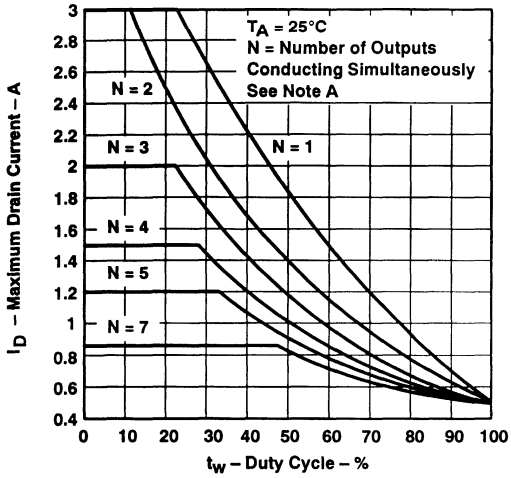


Figure 17

MAXIMUM CLAMP-DIODE CURRENT
vs
DUTY CYCLE

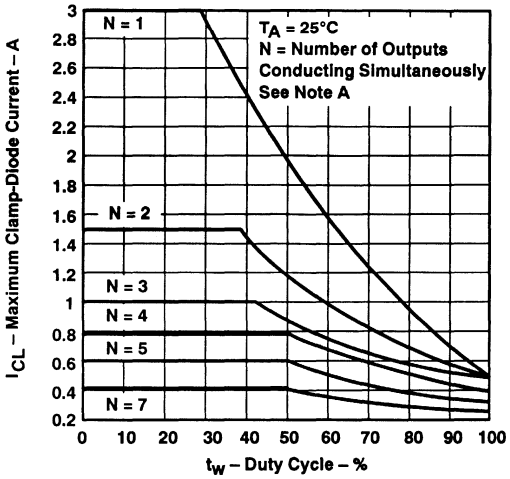
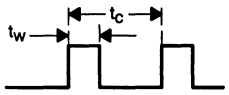


Figure 18



NOTE A: For Figures 17 and 18, $d = t_w/t_c = 10\ ms / t_c$, where t_w and t_c are defined by the following:

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

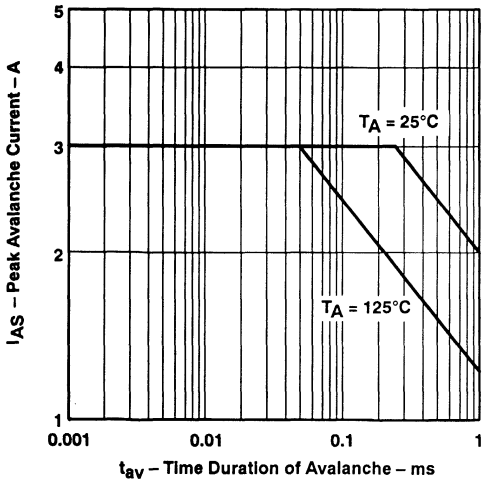


Figure 19

MAXIMUM DRAIN CURRENT
vs
DRAIN-SOURCE VOLTAGE

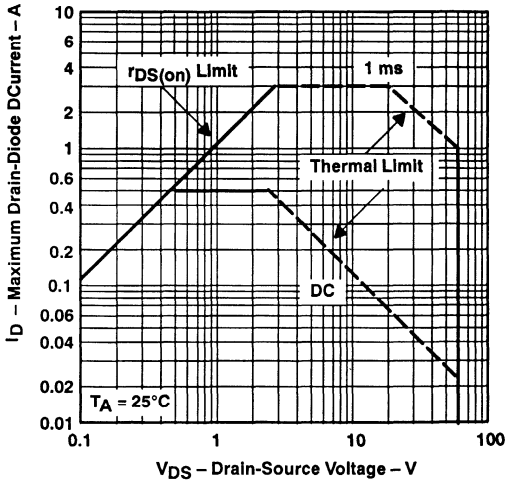
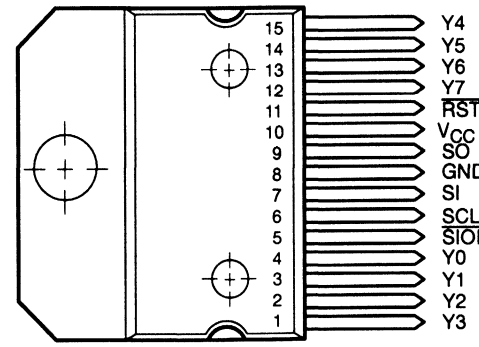


Figure 20

- **8-Bit Serial-In Parallel-Out Driver**
- **1-A Output Current Capability Per Channel or 8-A Total Current**
- **Overcurrent Limiting and Out-of-Saturation Voltage Protection on Driver Outputs**
- **Contains Eight Open-Collector Saturating Sink Outputs With Low On-State Voltage**
- **High-Impedance Inputs With Hysteresis Are Compatible With TTL or CMOS Levels**
- **Very Low Standby Power 20 mW Typical**
- **Status of Output Drivers May Be Monitored at Serial Output**
- **3-State Serial Output Permits Serial Cascading or Wire-AND Device Connections**
- **25-V Transient Clamping With Inductive Switching on Outputs, 40-mJ Rating Per Driver Output**

KV PACKAGE
(TOP VIEW)



The tab is electrically connected to GND.

description

The TPIC2801 octal intelligent-power switch is a monolithic BIDFET† integrated circuit designed to sink currents up to 1 A at 30 V simultaneously at each of eight driver outputs under serial input data control. Status of the individual driver outputs is available in serial data format. The driver outputs have overcurrent limiting and out-of-saturation voltage protection features. Applications include driving solenoids, relays, dc motors, lamps, and other medium-current or high-voltage loads.

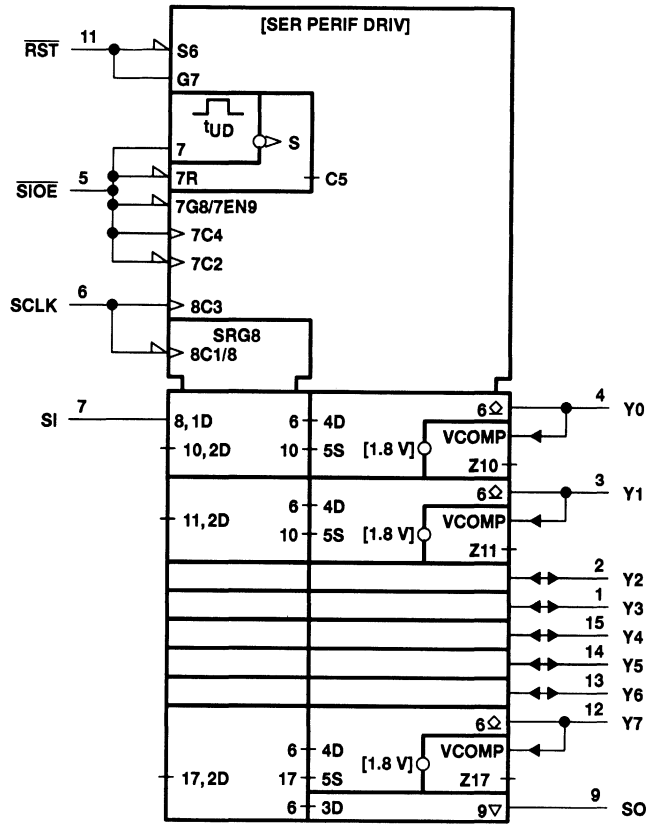
The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit parallel latch, which independently controls each of the eight Y-output drivers.

Data is entered into the device serially via the serial input (SI) and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic-high bit at SI turns the corresponding output driver (Y_n)off. A logic-low bit at SI turns the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of serial clock (SCLK) input in 8-bit bytes with data for the Y7 output (most significant bit) first and data for Y0 output (least significant bit) last. Both SI and SCLK are active when serial input-output enable ($\overline{SIOE}$) input is low and are disabled when $\overline{SIOE}$ is high.

Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal out-of-saturation threshold voltage reference level. The logic state of the comparator output is dependent upon whether the Y output is greater or smaller than the reference voltage level. An activated driver output is unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level except when the internal unlatch enable is low and disabled. The high-to-low transition of $\overline{SIOE}$ transfers the logic state of the comparator output to the shift register.

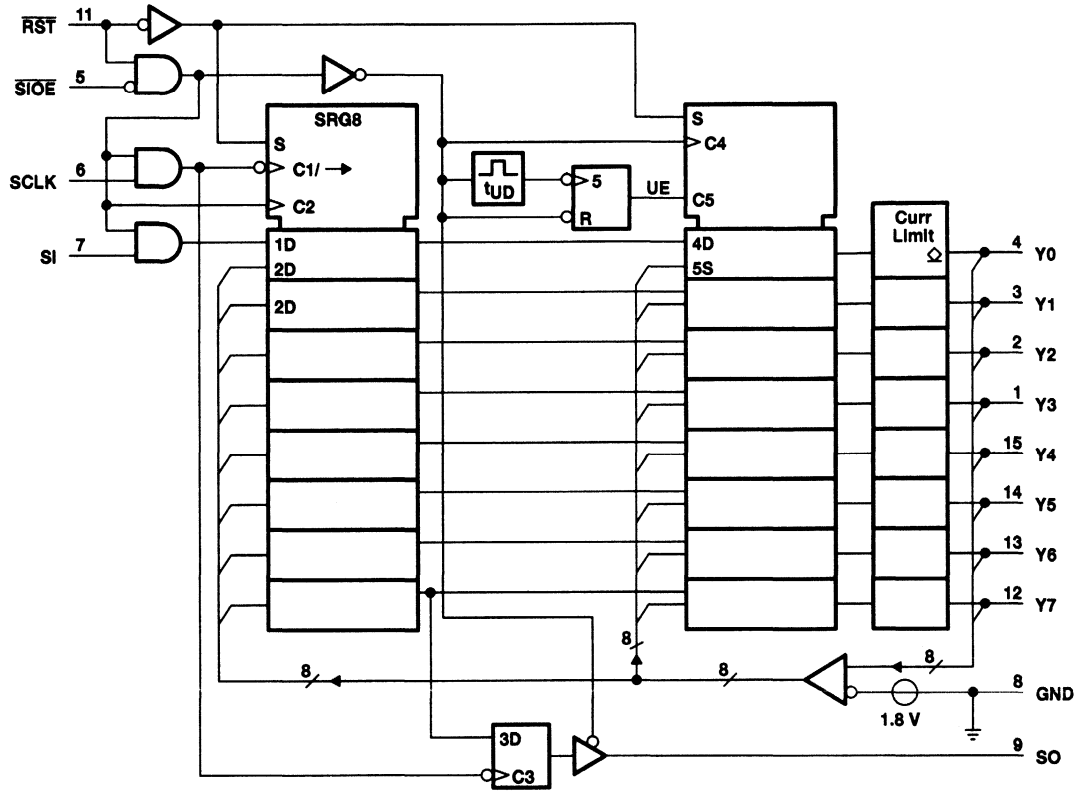
† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

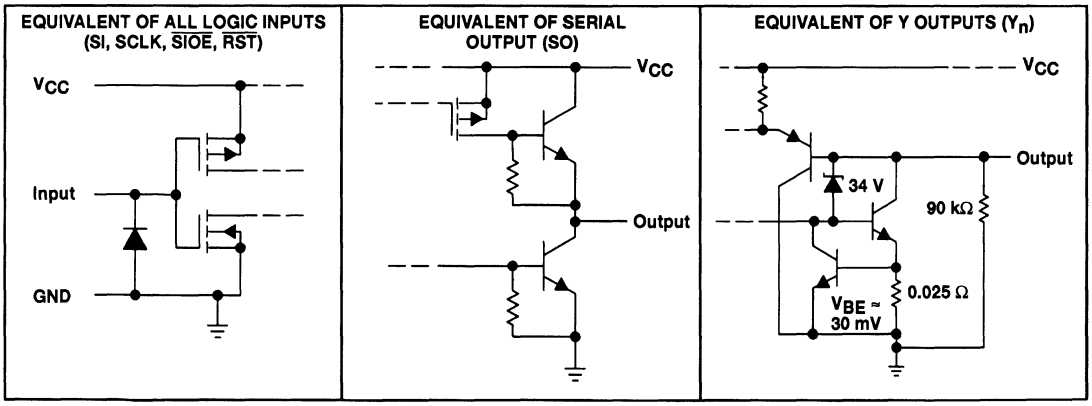
logic diagram (positive logic)



Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
GND	8		Ground. Common return for entire chip. The current from this terminal is potentially as high as 4 A if all outputs are on. GND is used for both logic and power circuits.
$\overline{RST}$	11	I	Reset. An asynchronous reset is provided for the shift register and the parallel latches. This terminal is active when low and has no internal pullup. When active, it causes the power outputs to turn off. A power-on clear can be implemented using an RC network to V_{CC}.
SCLK	6	I	Serial clock. This terminal clocks the shift register. The serial output (SO) changes state on the rising edge of SCLK and serial input (SI) data is accepted on the falling edge.
SI	7	I	Serial input. This terminal is the serial data input. A high on this terminal programs a particular output off, and a low turns it on.
$\overline{SIOE}$	5	I	Serial input-output enable. Data is transferred from the shift registers to the power outputs on the rising edge of this signal. The falling edge of this signal parallel loads the output voltage sense bits from the power output stages into the shift register. The output driver for SO is enabled when this terminal is low, provided $\overline{RST}$ is high.
SO	9	O	Serial output. This terminal is the serial 3-state output from the shift register and is in a high-impedance state when $\overline{SIOE}$ is high or $\overline{RST}$ is low. A high for a data bit on this terminal indicates that the corresponding power output (Y_n) is high. This means that the output was programmed to be off the last time a byte was input to the device or that the output faulted and was latched off by the output voltage-sense indicator. A low on this output indicates that the corresponding power output (Y_n) is low (on output stage or open-circuit condition).
V_{CC}	10		5-V supply voltage
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	4 3 2 1 15 14 13 12	O	Power outputs. These outputs are provided with current limiting and voltage sense for fault indication and protection. The nominal load current for these outputs is 500 mA, and the current limiting is set to a minimum of 1.2 A. The active-low outputs also have voltage clamps set at about 35 V for recirculation of inductive load current. Internal 90-kΩ pulldown resistors are provided at each output. These resistors hold the output low during an open-circuit condition.

schematic of inputs and outputs



All resistor and voltage values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... – 0.3 V to 7 V
Input voltage, V_I ..... 7 V
Output voltage range, V_O ..... – 0.3 V to 7 V
Input current, I_I ..... –15 mA
Peak output sink current at Y, I_O repetitive, t_w = 10 ms, duty cycle = 50%,
(see Notes 2 and 3) ..... internally limited
Continuous output current at Y, I_O (see Note 3) ..... 1 A
Peak current through GND: Nonrepetitive t_w = 0.2 ms ..... – 8 A
Repetitive, t_w = 10 ms, duty cycle = 50% ..... – 6 A
Continuous current through GND ..... – 4.5 A
Output clamp energy, E_{OK} (after turning off I_O(on) = 0.5 A) ..... 40 mJ
Continuous dissipation at (or below) T_A = 25°C (see Note 4) ..... 3.575 W
Continuous dissipation at (or below) T_C = 75°C (see Note 4) ..... 25 W
Operating case or virtual junction temperature range ..... – 55°C to 150°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network GND.
2. Each Y output is individually current limited with a typical overcurrent limit of about 1.4 A.
3. Multiple Y outputs of this device can conduct rated current simultaneously; however, power dissipation (average) over a short time interval must fall within the continuous dissipation range and the GND current must fall within the GND-terminal current range.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. To avoid exceeding the maximum virtual junction temperature, these ratings must not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	0.7 V_{CC}		5.25	V
Low-level input voltage, V_{IL}	–0.3		0.2 V_{CC}	V
Output voltage, $V_{O(off)}$			30	V
Continuous output current, $I_{O(on)}$			1	A
Operating case temperature, T_C	–40	25	105	°C

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

driver array outputs (Y0 to Y7)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OK}	Output clamp voltage	I_O = 0.5 A,	Output programmed off and current shunted to GND	30	36	40	V
$V_{O(on)}$	On-state output voltage	With output programmed on	I_{OL} = 0.5 A		0.4	0.5	V
			I_{OL} = 0.75 A		0.6	1	V
			I_{OL} = 1 A, During unlatch disable		0.8	1.5	V
V_{TOS}	Out-of-saturation threshold voltage	With output programmed on and an overcurrent fault condition		1.6	1.8	2	V
$I_{O(off)}$	Off-state output current	V_O = 24 V with output programmed off				1	mA
$I_{O(cl)}$	Output current limit	V_O = 3 V with output programmed on		1.05	1.4		A

shift register (inputs SI, $\overline{SIOE}$, SCLK, and $\overline{RST}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{T+}	Positive-going threshold voltage			0.7 V_{CC}	V
V_{T-}	Negative-going threshold voltage		0.2 V_{CC}		V
V_{hys}	Hysteresis voltage ($V_{T+} - V_{T-}$)		0.85	2.25	V
I_I	Input current	V_I = 0 to V_{CC}		±10	µA
C_i	Input capacitance	V_I = 0 to V_{CC}		20	pF

shift register (output SO)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	I_O = 1.6 mA			0.2	0.4	V
V_{OH}	High-level output voltage	I_O = – 0.8 mA		V_{CC} –1.3			V
I_O	Output current	V_O = 0 to V_{CC},	$\overline{SIOE}$ input high			±10	µA
I_{CC}	Supply current	All outputs on, I_O = 0.5 A at all outputs	T_J = 105°C			150	mA
			T_J = 25°C			200	
			T_J = –40°C			250	
		All outputs off	T_J = 25°C		4	10	
C_o	Output capacitance	V_O = 0 to V_{CC},	$\overline{SIOE}$ input high			20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

timing requirements over receommended ranges of supply voltage and operating case temperature (see Figure 1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, SCLK	See Note 5	0	500	kHz
$t_{w(SCLKH)}$	Pulse duration, SCLK high		840		ns
$t_{w(SCLKL)}$	Pulse duration, SCLK low		840		ns
$t_{w(RST)}$	Pulse duration, $\overline{RST}$ low		1000		ns
t_{su1}	Setup time, $\overline{SIOE}\downarrow$ before SCLK$\uparrow$		1000		ns
t_{su2}	Setup time, SCLK$\downarrow$ before $\overline{SIOE}\uparrow$		1000		ns
t_{su3}	Setup time, SI high before SCLK$\downarrow$		500		ns
t_{h1}	Hold time, SI low after SCLK$\downarrow$		500		ns
t_r	Rise time (SCLK, SI, $\overline{SIOE}$)			2	µs
t_f	Fall time (SCLK, SI, $\overline{SIOE}$)			2	µs

NOTE 5: For cascaded operation, the clock pulse durations [t_w (SCLKL) and t_w (SCLKH)] must be a minimum of 700 ns (giving a maximum clock frequency of 632 kHz).

thermal characteristics

PARAMETER		MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case temperature		3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient temperature		35	°C/W

switching characteristics over recommended ranges of supply voltage and operating case temperature

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{en}	Enable time	$\overline{SIOE}\downarrow$	SO	C_L = 20 pF, R_L = 2 kΩ, See Figure 2		1000	ns
t_{dis}	Disable time	$\overline{SIOE}\uparrow$	SO	C_L = 20 pF, R_L = 2 kΩ, See Figure 2		1000	ns
t_{d1}	Delay time, valid data	SCLK$\uparrow$	SO	C_L = 200 pF, See Figure 3		740	ns
t_{d2}	Delay time, unlatch disable	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 5 Ω, See Figure 4	75	250	µs
$t_{r(SO)}$	Rise time, SO			C_L = 200 pF, See Figure 3		150	ns
$t_{f(SO)}$	Fall time, SO			C_L = 200 pF, See Figure 3		150	ns
$t_{d(on)}$	Delay time, turn on	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 28 Ω, I_{OL} = 500 mA, See Figure 5		10	µs
$t_{d(off)}$	Delay time, turn off	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 28 Ω, I_{OL} = 500 mA, See Figure 5		10	µs
t_v	Valid time, SO output data remains valid after SCLK high	SCLK$\uparrow$	SO	C_L = 200 pF, See Figure 3	0		ns

PARAMETER MEASUREMENT INFORMATION

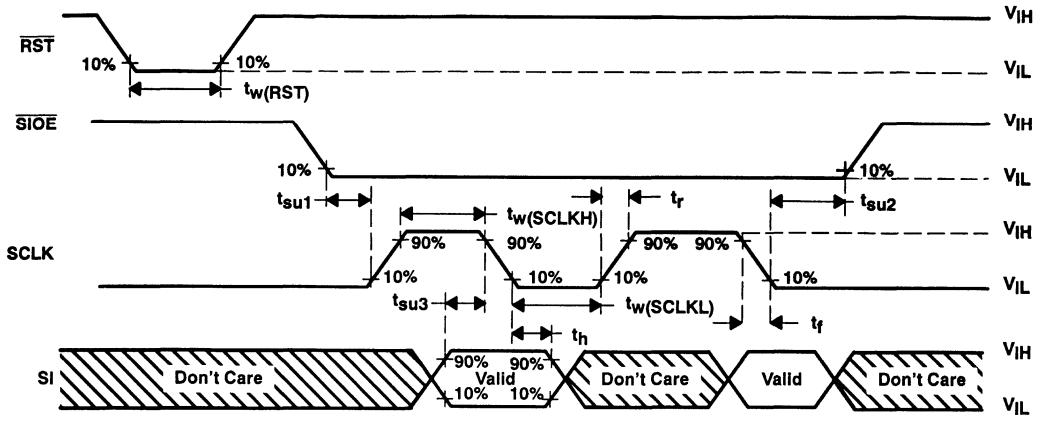
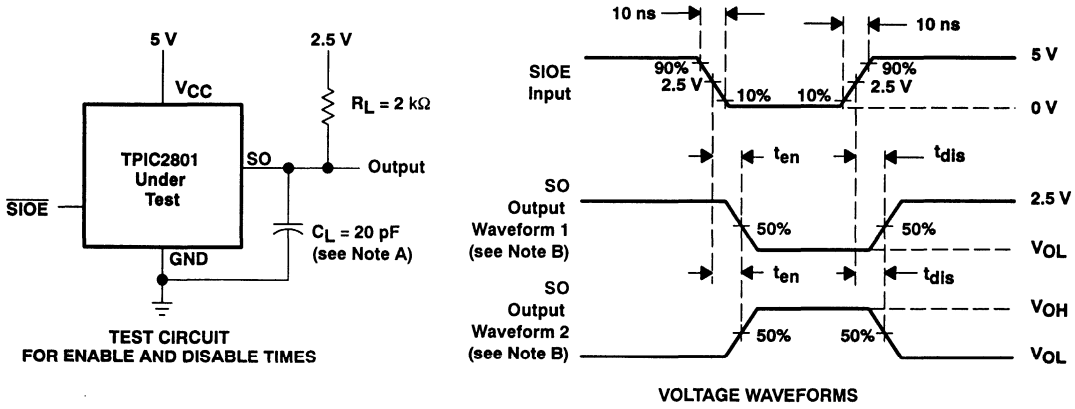


Figure 1. Input Timing Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control when $\overline{SIOE}$ is high. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control when $\overline{SIOE}$ is high.

Figure 2. Test Circuit and Voltage Waveforms for Enable and Disable Times

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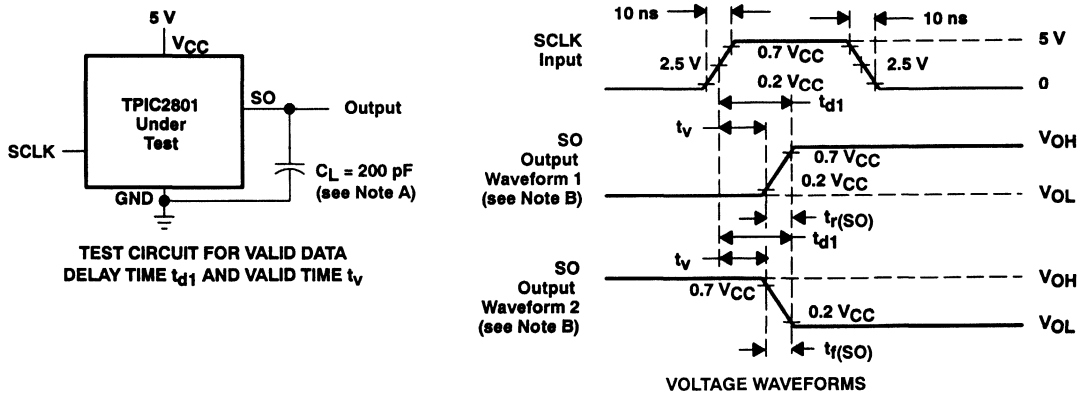
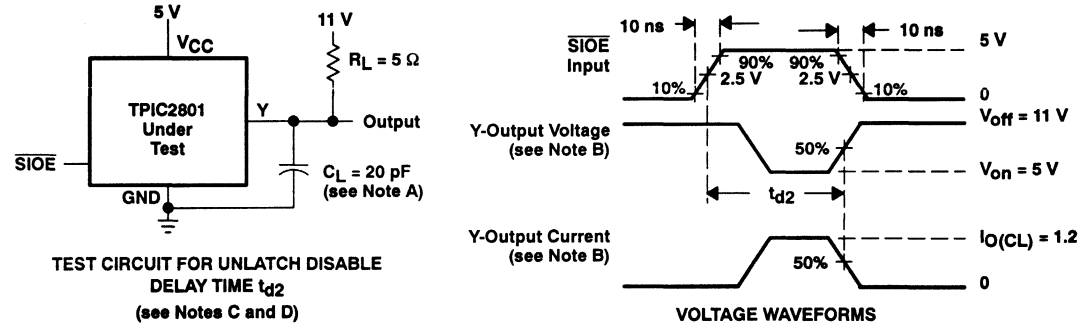
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from low to high. Waveform 2 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from high to low.

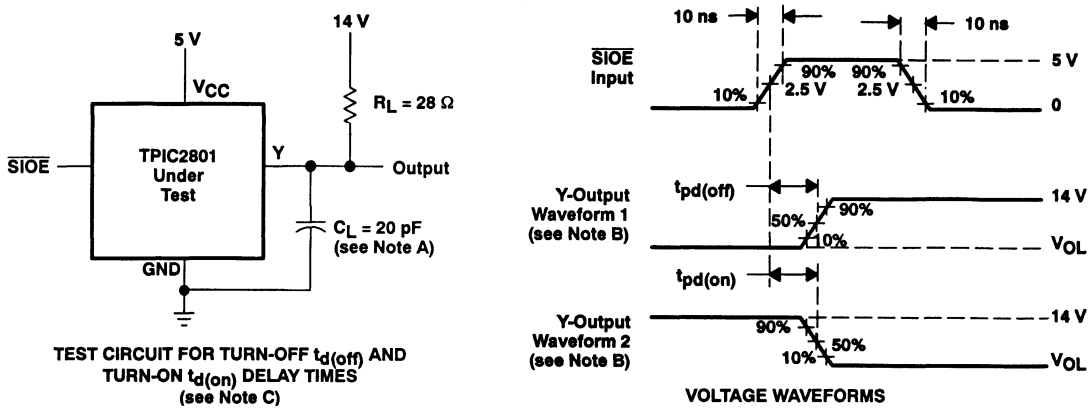
Figure 3. Test Circuit and Voltage Waveforms for Delay Times



NOTES: A. C_L includes probe and jig capacitance.
B. Output voltage and current waveforms are for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from being off to being on.
C. t_{d2} = delay until Y-output current goes off under fault condition.
D. Load voltage V_S and load resistance R_L are selected such that on-state voltage at the Y output under test, V_{on} is greater than the maximum out-of-saturation hold voltage, V_{TOS}. Thus $V_{OL} = V_{on} > V_{TOS(max)} = 1.98$ V.

Figure 4. Test Circuit and Voltage and Current Waveforms for Unlatch Disable Delay

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT FOR TURN-OFF $t_{d(off)}$ AND TURN-ON $t_{d(on)}$ DELAY TIMES (see Note C)

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from on to off. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

C. $t_{d(off)} = t_{PLH}$, $t_{d(on)} = t_{PHL}$.

Figure 5. Test Circuit and Voltage Waveforms for Turn-Off and Turn-On Delay Times

APPLICATION INFORMATION

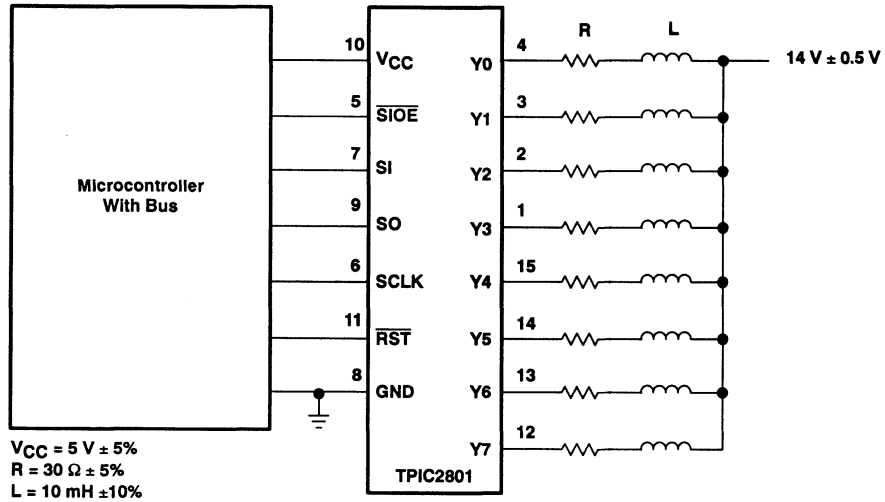


Figure 6. Microcontroller Driving Eight Loads Using a TPIC2801 for Load Interface

PRINCIPLES OF OPERATION

timing data transfer

Figure 7 shows the overall 8-bit data-byte transfer to and from the TPIC2801 interface bus. The logic state of the eight output drivers, Y0 through Y7, is latched into the shift register at time t_0 on the high-to-low transition of $\overline{SIOE}$. Therefore, the SO output data (DY0, DY1 . . .) represent the conditions at the Y-driver outputs at time t_0. The data at the SO output is updated on the low-to-high transition of SCLK.

Input data present at the SI input is clocked into the shift register on the high-to-low transition of SCLK. As shown in Figure 6 on the SI input, input data DI7 is clocked at time t_1, DI6 is clocked at time t_2, etc. Eight SCLK pulses are used to serially load the eight bits of new data into the device. After all the new data is serially loaded, the low-to-high transition of $\overline{SIOE}$ parallel loads the new data to the eight driver output latches, which in turn directly control the eight Y-driver outputs.

An unlimited amount of data can be shifted through the shift register (into the SI and out the SO), and this allows other devices to be cascaded in a daisy chain with the TPIC2801. Once the last data bit is shifted into the TPIC2801, the $\overline{SIOE}$ input is pulled high. The clock (SCLK) input is low at both transitions of the $\overline{SIOE}$ input to avoid any false clocking of the shift register. The SCLK input is gated by the $\overline{SIOE}$ input, so the SCLK input is ignored whenever $\overline{SIOE}$ is high. At the rising edge of $\overline{SIOE}$, the shift register data is latched into the parallel latch and the output stages are actuated by the new data. An internal 100-µs delay timer is also started on this rising edge. During the time delay, the outputs are protected only by the analog current-limiting circuits, since the resetting of the parallel latches by fault conditions are inhibited during this time period. This allows the device to overcome any high switching currents that can flow during turn on. Once the delay ends, the output voltages are sensed by the comparators and any output voltages higher than nominally 1.8 V are latched off.

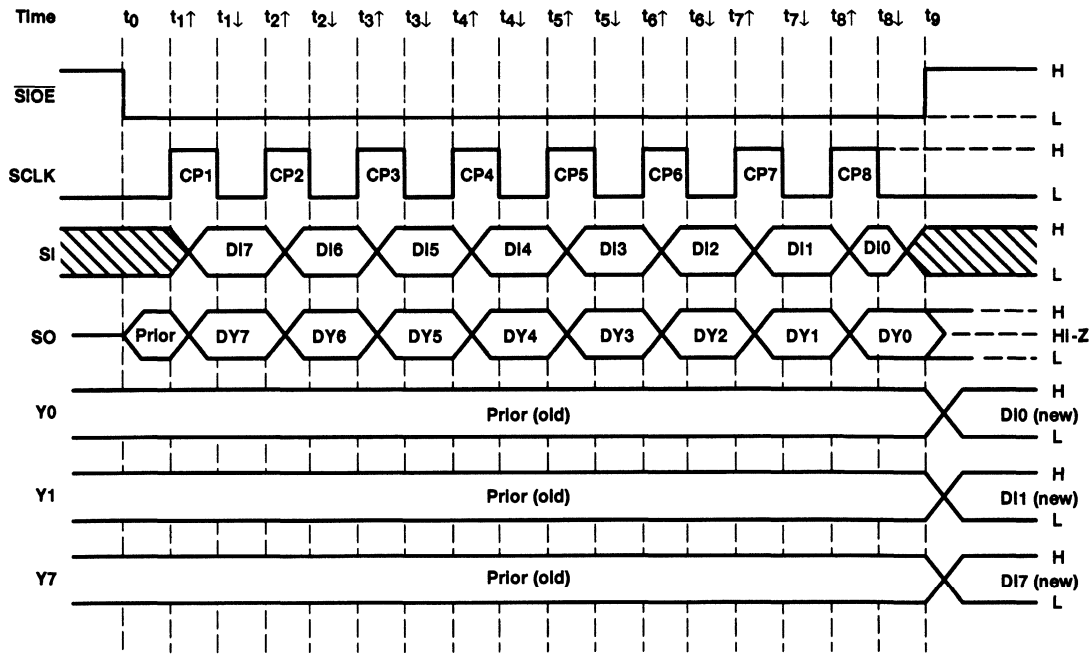


Figure 7. Data-Byte Transfer Timing

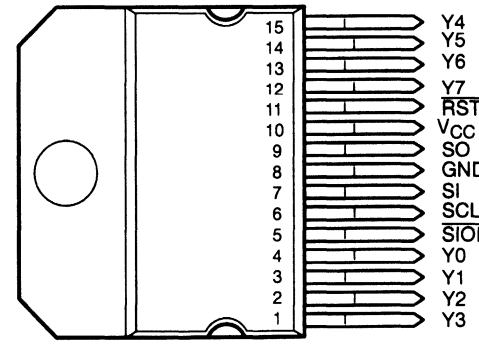
PRINCIPLES OF OPERATION

fault-conditions check

Open-circuit conditions on any output can be monitored or checked by programming that output off. After a short delay (microseconds), another control byte can be clocked into the device. If the diagnostic bit for that output comes back as a low, it indicates that the output is low and open circulted. A current overload condition can be detected by programming an output on. After waiting an appropriate length of time, another byte is clocked into the TPIC2801. The diagnostic bit clocked back from the TPIC2801 in the subsequent data transfer indicates a low output. If a high returns, a current overload is indicated. A quick overall check is done by clocking in a test control byte. After a sufficient time delay, clock in another control byte (same byte is used). The diagnostic data is exclusive ORed with the original control byte. If a fault condition exists, a high results from the subsequent exclusive OR.

- **8-Bit Serial-In Parallel-Out Driver**
- **1-A Output Current Capability Per Channel or 8-A Total Current**
- **Overcurrent Limiting and Out-of-Saturation Voltage Protection on Driver Outputs**
- **Contains Eight Open-Collector Saturating Sink Outputs With Low On-State Voltage**
- **High-Impedance Inputs With Hysteresis Are Compatible With TTL or CMOS Levels**
- **Very Low Standby Power 20 mW Typical**
- **Status of Output Drivers May Be Monitored at Serial Output**
- **3-State Serial Output Permits Serial Cascading or Wire-AND Device Connections**
- **35-V Transient Clamping With Inductive Switching on Outputs, 40-mJ Rating Per Driver Output**

KV PACKAGE
(TOP VIEW)



The tab is electrically connected to GND.

description

The TPIC2801A octal intelligent-power switch is a monolithic BIDFET† integrated circuit designed to sink currents up to 1 A at 35 V simultaneously at each of eight driver outputs under serial input data control. Status of the individual driver outputs is available in serial data format. The driver outputs have overcurrent limiting and out-of-saturation voltage protection features. Applications include driving solenoids, relays, dc motors, lamps, and other medium-current or high-voltage loads.

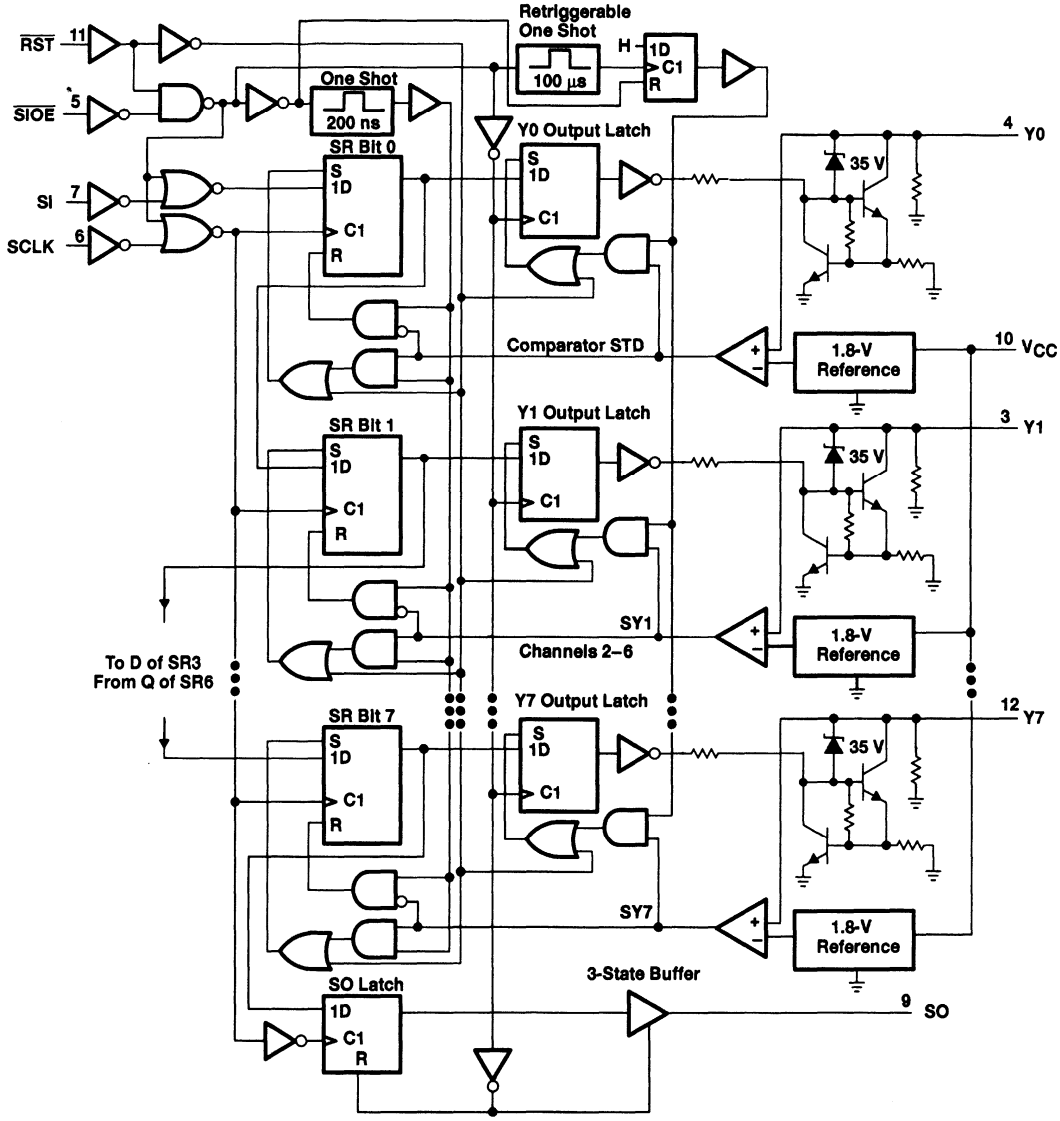
The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit parallel latch, which independently controls each of the eight Y-output drivers.

Data is entered into the device serially via the serial input (SI) and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic-high SI bit n turns the corresponding output driver (Y_n) off. A logic-low bit at SI turns the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of the serial clock (SCLK) input in 8-bit bytes with data for the Y7 output (most significant bit) first and data for Y0 output (least significant bit) last. Both SI and SCLK are active when the serial input-output enable ($\overline{SIOE}$) input is low and are disabled when $\overline{SIOE}$ is high.

Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal out-of-saturation threshold voltage reference level. The logic state of the comparator output is dependent upon whether the Y output is greater or smaller than the reference voltage level. While $\overline{SIOE}$ is held high, an activated driver output is unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level except when the internal unlatch enable is low and disabled. The high-to-low transition of $\overline{SIOE}$ transfers the logic state of the comparator output to the shift register.

†BIDFET – Bipolar double-diffused, N-channel and P-channel MOS transistors are on the same chip. This is a patented process.

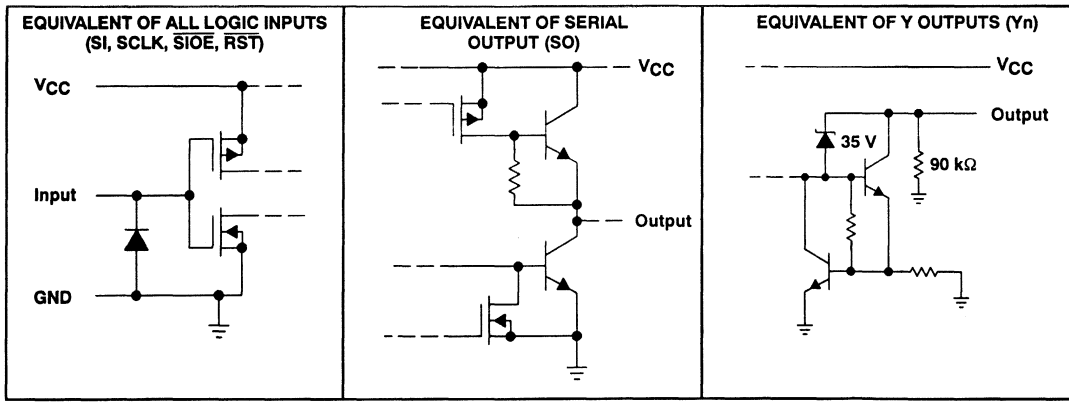
functional block diagram



Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
GND	8		Ground. Common return for entire chip. The output current from this terminal is potentially as high as 8 A if all outputs are on. GND is used for both logic and power circuits.
$\overline{RST}$	11	I	Reset. An asynchronous reset is provided for the shift register and the parallel latches. This terminal is active when low and has no internal pullup. When active, it causes the power outputs to turn off. A power-on clear can be implemented using an RC network to V_{CC}.
SCLK	6	I	Serial clock. This terminal clocks the shift register. The serial output (SO) changes state on the rising edge of SCLK, and serial input (SI) data is accepted on the falling edge.
SI	7	I	Serial Input. A high on this terminal programs a particular output to be off, and a low turns it on.
$\overline{SIOE}$	5	I	Serial input-output enable. Data is transferred from the shift registers to the power outputs on the rising edge of this signal. The falling edge of this signal parallel loads the output voltage sense bits from the power output stages into the shift register. The output driver SO is enabled when this terminal is low, provided $\overline{RST}$ is high.
SO	9	O	Serial output. This terminal is the serial 3-state output from the shift register and is in a high-impedance state when $\overline{SIOE}$ is high or $\overline{RST}$ is low. A high for a data bit on this terminal indicates that the corresponding power output (Y_n) is high. This means that the output was programmed to be off the last time a byte was input to the device or that the output faulted and was latched off by the output voltage-sense indicator. A low on this output indicates that the corresponding power output (Y_n) is low (on output stage or open-circuit condition).
V_{CC}	10		5-V supply voltage
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	4 3 2 1 15 14 13 12	O	Power outputs. These outputs are provided with current limiting and voltage sense for fault indication and protection. The nominal load current for these outputs is 500 mA, and the current limiting is set to a minimum of 1.05 A. The active-low outputs also have voltage clamps set at about 35 V for recirculation of inductive load current. Internal 90-kΩ pulldown resistors are provided at each output. These resistors hold the output low during an open-circuit condition.

schematic of inputs and outputs



All resistor and voltage values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... – 0.3 V to 7 V
Input voltage, V_I ..... 7 V
Output voltage range at SO, V_O ..... – 0.3 V to 7 V
Input current, I_I ..... –15 mA
Peak output sink current at Y, I_O repetitive, t_w = 10 ms, duty cycle = 50%,
(see Notes 2 and 3) ..... internally limited
Continuous output current at Y, I_O (see Note 3) ..... 1 A
Peak current through GND: Nonrepetitive t_w = 0.2 ms ..... – 8 A
Repetitive t_w = 10 ms, duty cycle = 50% ..... – 6 A
Output clamp energy, E_{OK} (after turning off I_O(on) = 0.5 A) ..... 40 mJ
Continuous current through GND ..... – 4.5 A
Continuous dissipation at (or below) T_A = 25°C (see Note 4) ..... 3.575 W
Continuous dissipation at (or below) T_C = 75°C (see Note 4) ..... 25 W
Operating case or virtual junction temperature range ..... – 55°C to 150°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network GND.
2. Each Y output is individually current limited with a typical overcurrent limit of about 1.4 A.
3. Multiple Y outputs of this device can conduct rated current simultaneously; however, power dissipation (average) over a short time interval must fall within the continuous dissipation range and GND current range.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. To avoid exceeding the maximum virtual junction temperature, these ratings must not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	0.75 V_{CC}		5.25	V
Low-level input voltage, V_{IL}	–0.3		0.2 V_{CC}	V
Output voltage, $V_{O(off)}$			30	V
Continuous output current, $I_{O(on)}$			1	A
Operating case temperature, T_C	–40	25	105	°C

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current	All outputs on, I_O = 0.5 A at all outputs	T_J = 105°C			150	mA
			T_J = 25°C			200	
			T_J = –40°C			250	
		All outputs off	T_J = 25°C		4	10	

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted) (continued)

driver array outputs (Y0 to Y7)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OK}	Output clamp voltage	I_O = 0.5 A,	Output programmed off and current shunted to GND	30	36	40	V
$V_{O(on)}$	On-state output voltage	With one output programmed on and conducting	I_{OL} = 0.5 A		0.4	0.5	V
			I_{OL} = 0.75 A		0.6	1	V
			I_{OL} = 1 A, During unlatch disable		0.8	1.5	V
V_{TOS}	Out-of-saturation threshold voltage	With output programmed on and an overcurrent fault condition		1.6	1.8	2.1	V
$I_{O(off)}$	Off-state output current	V_O = 24 V with output programmed off				1	mA
$I_{O(cl)}$	Output current limit	V_O = 3 V with output programmed on		1.05	1.4		A

shift register (Inputs SI, $\overline{SIOE}$, SCLK, and $\overline{RST}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{T+}	Positive-going threshold voltage			0.75 V_{CC}	V
V_{T-}	Negative-going threshold voltage		0.2 V_{CC}		V
V_{hys}	Hysteresis voltage ($V_{T+} - V_{T-}$)		0.85	2.25	V
I_I	Input current	V_I = 0 to V_{CC}		±10	µA
C_i	Input capacitance	V_I = 0 to V_{CC}		20	pF

shift register (output SO)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	I_O = 1.6 mA			0.2	0.4	V
V_{OH}	High-level output voltage	I_O = – 0.8 mA		V_{CC} –1.3			V
I_O	Output current	V_O = 0 to V_{CC},	$\overline{SIOE}$ input high			±20	µA
C_o	Output capacitance	V_O = 0 to V_{CC},	$\overline{SIOE}$ input high			20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

timing requirements over recommended ranges of supply voltage and operating case temperature (see Figure 1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, SCLK	See Note 5	0	1	MHz
$t_{w(SCLKH)}$	Pulse duration, SCLK high		410		ns
$t_{w(SCLKL)}$	Pulse duration, SCLK low		410		ns
$t_{w(RST)}$	Pulse duration, $\overline{RST}$ low		1000		ns
t_{su1}	Setup time, $\overline{SIOE}$↓ before SCLK↑		1		µs
t_{su2}	Setup time, SCLK↓ before $\overline{SIOE}$↑		1		µs
t_{su3}	Setup time, SI high before SCLK↓		150		ns
t_{h1}	Hold time, SI low after SCLK↓		150		ns
t_r	Rise time, SCLK, SI, $\overline{SIOE}$			90	ns
t_f	Fall time, SCLK, SI, $\overline{SIOE}$			90	ns

NOTE 5: For cascaded operation, the clock pulse durations [$t_{w(SCLKL)}$ and $t_{w(SCLKH)}$] must be a minimum of 700 ns (giving a maximum clock frequency of 632 kHz).

thermal characteristics

PARAMETER		MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case temperature		3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient temperature		35	°C/W

switching characteristics over recommended ranges of supply voltage and operating case temperature

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{en}	Enable time	$\overline{SIOE}\downarrow$	SO	C_L = 20 pF, R_L = 1 kΩ, See Figure 2		1000	ns
t_{dis}	Disable time	$\overline{SIOE}\uparrow$	SO	C_L = 20 pF, R_L = 1 kΩ, See Figure 2		1000	ns
t_{d1}	Delay time, valid data	SCLK↑	SO	C_L = 200 pF, See Figure 3		550	ns
t_{d2}	Delay time, unlatch disable	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 5 Ω, See Figure 4	75	250	µs
$t_{r(SO)}$	Rise time		SO	C_L = 200 pF, See Figure 3		150	ns
$t_{f(SO)}$	Fall time		SO	C_L = 200 pF, See Figure 3		150	ns
$t_{d(on)}$	Delay time, turn on	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 28 Ω, I_{OL} = 500 mA, See Figure 5		10	µs
$t_{d(off)}$	Delay time, turn off	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 28 Ω, I_{OL} = 500 mA, See Figure 5		10	µs
t_v	Valid time, SO output data remains valid after SCLK high	SCLK↑	SO	C_L = 200 pF, See Figure 3	0		ns

PARAMETER MEASUREMENT INFORMATION

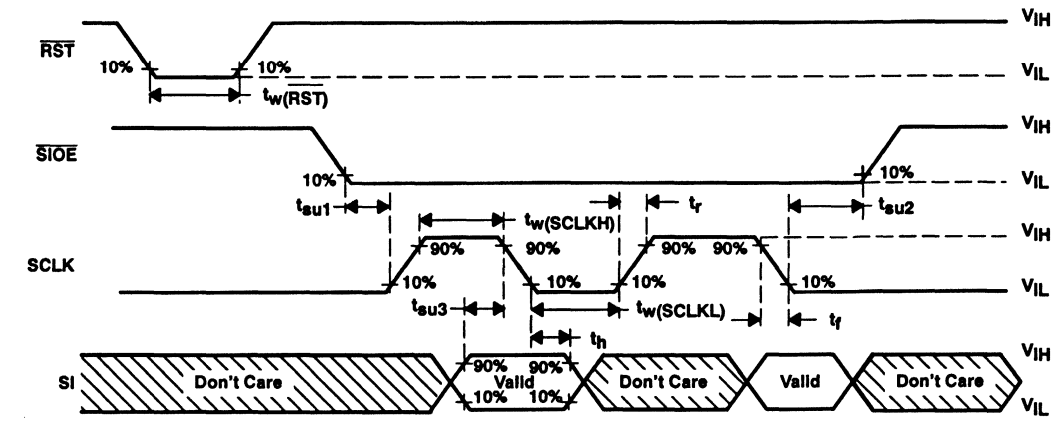
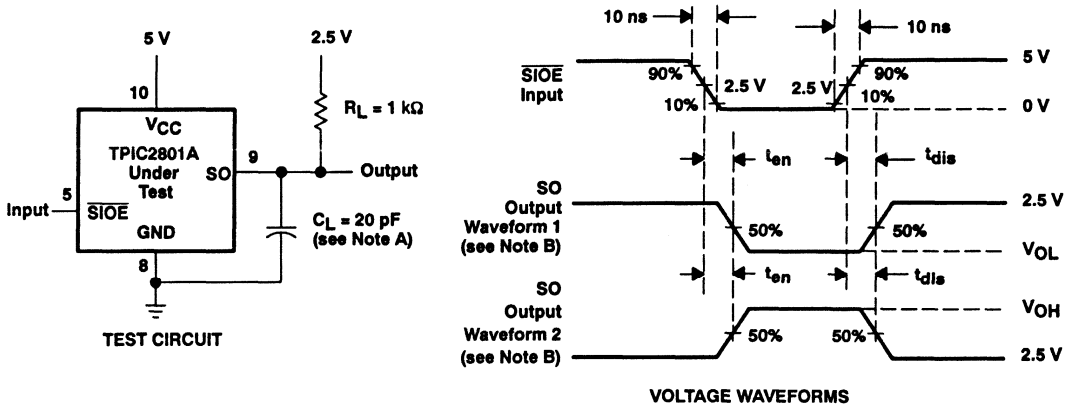


Figure 1. Input Timing Diagram

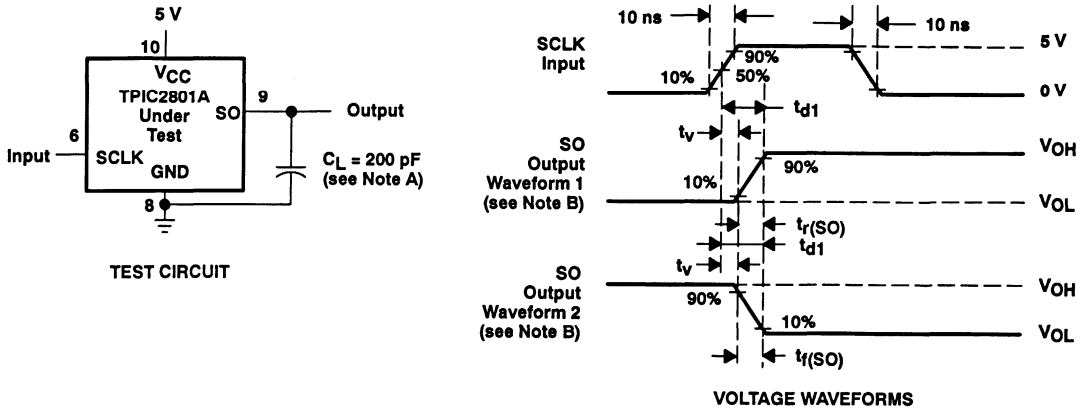


NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control when $\overline{SIOE}$ is high. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

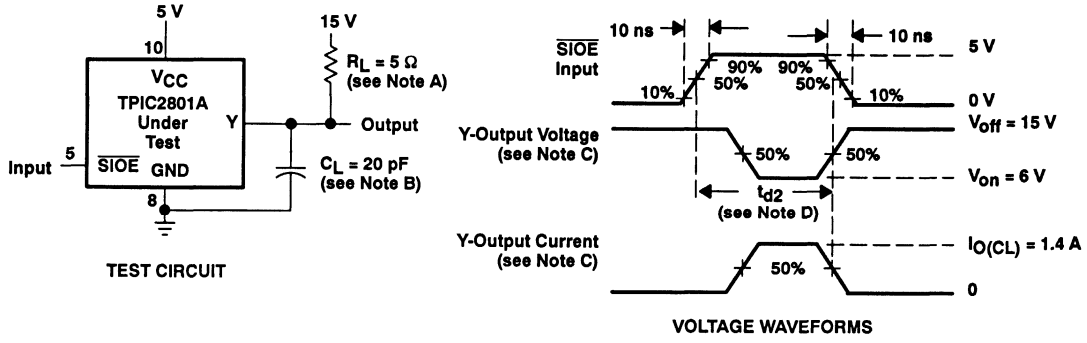
Figure 2. Enable and Disable Times Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from high to low. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

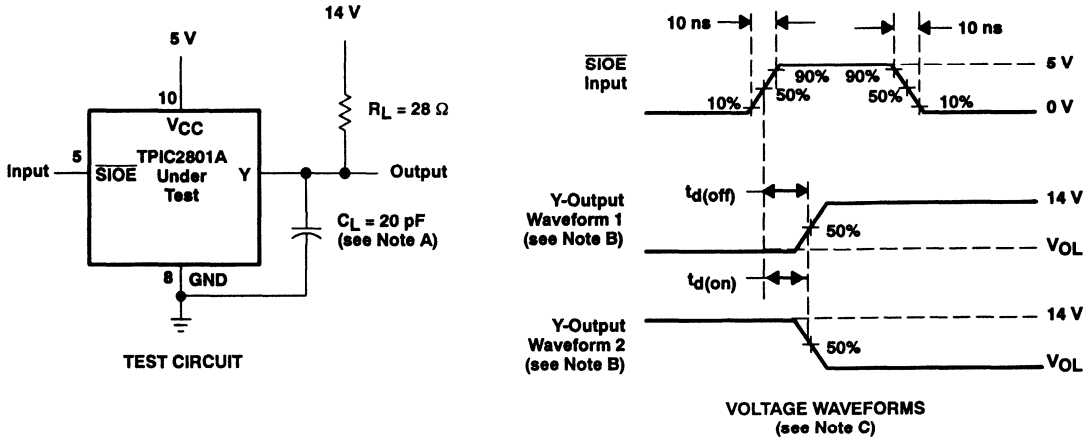
Figure 3. Delay Times Test Circuit and Voltage Waveforms



NOTES: A. Load voltage V_S and load resistance R_L are selected such that on-state voltage at the Y output under test, V_{on} is greater than the maximum out-of-saturation hold voltage, V_{TOS}. Thus $V_{OL} = V_{on} > V_{TOS(max)} = 2.1$ V.
B. C_L includes probe and jig capacitance.
C. Output voltage and current waveforms are for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.
D. t_{d2} = delay until Y-output current goes off under fault condition.

Figure 4. Unlatch Disable Delay Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from on to off. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

C. $t_{d(off)} = t_{PLH}$, $t_{d(on)} = t_{PHL}$

Figure 5. Turn-Off and Turn-On Delay Times Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

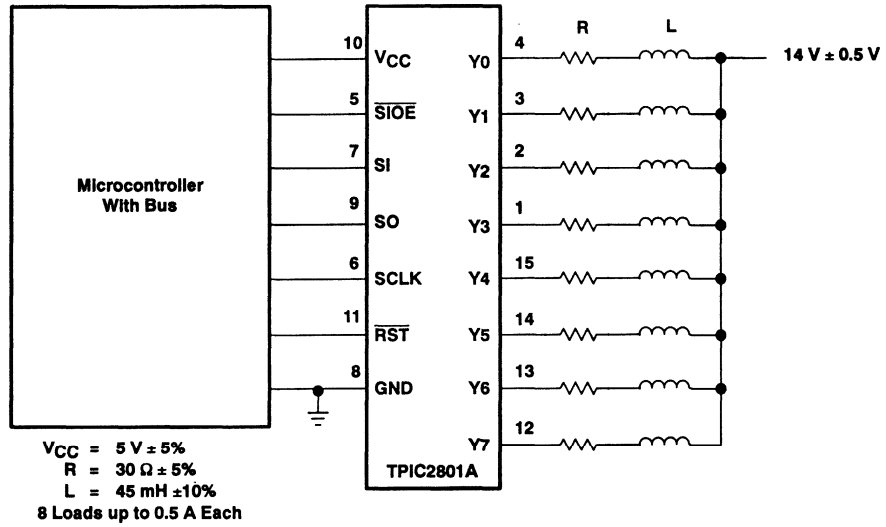


Figure 6. Microcontroller Driving Eight Loads Using a TPIC2801A for Load Interface

PRINCIPLES OF OPERATION

timing data transfer

Figure 7 shows the overall 8-bit data-byte transfer to and from the TPIC2801A interface bus. The logic state of the eight output drivers, Y0 through Y7, is latched into the shift register at time t_0 on the high-to-low transition of $\overline{SIOE}$. Therefore, the SO output data (DY0, DY1 . . .) represents the conditions at the Y-driver outputs at time t_0. The data at the SO output is updated on the low-to-high transition of SCLK.

Input data present at the SI input is clocked into the shift register on the high-to-low transition of SCLK. As shown in Figure 7 on the SI input, input data DI7 is clocked at time t_1, DI6 is clocked at time t_2, etc. Eight SCLK pulses are used to serially load the eight bits of new data into the device. After all the new data is serially loaded, the low-to-high transition of SIOE parallel loads the new data to the eight driver output latches, which in turn directly control the eight Y-driver outputs.

An unlimited amount of data can be shifted through the shift register (into the SI and out the SO), and this allows other devices to be cascaded in a daisy chain with the TPIC2801A. Once the last data bit is shifted into the TPIC2801A, the $\overline{SIOE}$ input is pulled high. The clock (SCLK) input is low at both transitions of the $\overline{SIOE}$ input to avoid any false clicking of the shift register. The SCLK input is gated by the $\overline{SIOE}$ input, so the SCLK input is ignored whenever $\overline{SIOE}$ is high. At the rising edge of $\overline{SIOE}$, the shift register data is latched into the parallel latch and the output stages are actuated by the new data. An internal 100-µs delay timer is also started on this rising edge. During the time delay, the outputs are protected only by the analog current-limiting circuits, since the resetting of the parallel latches by fault conditions is inhibited during this time period. This allows the device to overcome any high switching currents that can flow during turn on. Once the delay ends, the output voltages are sensed by the comparators and any output voltages higher than nominally 1.8 V are latched off.

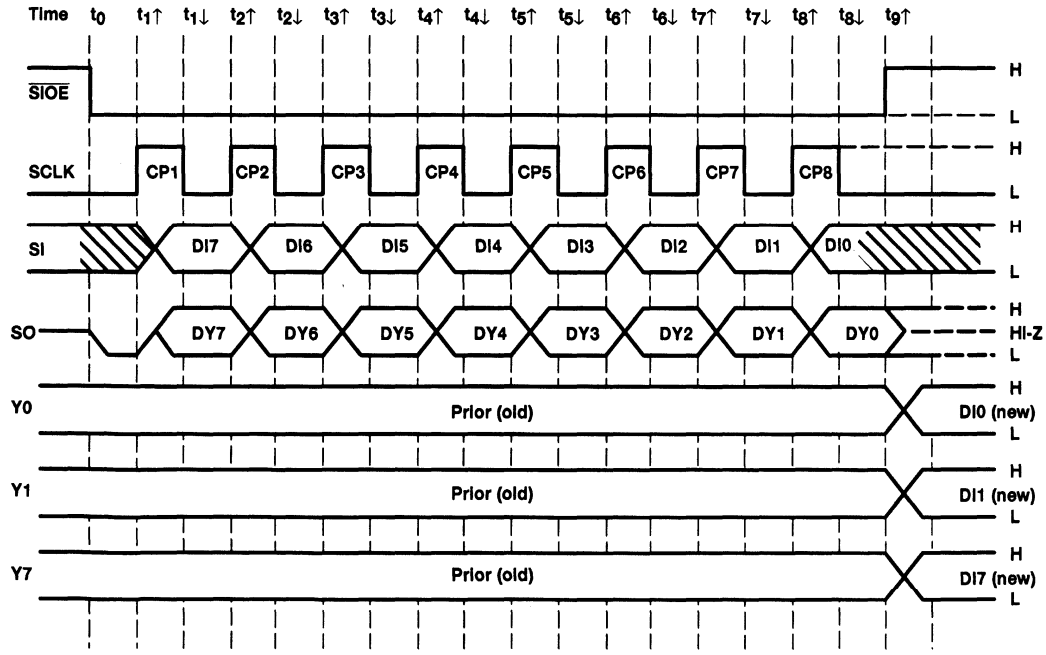


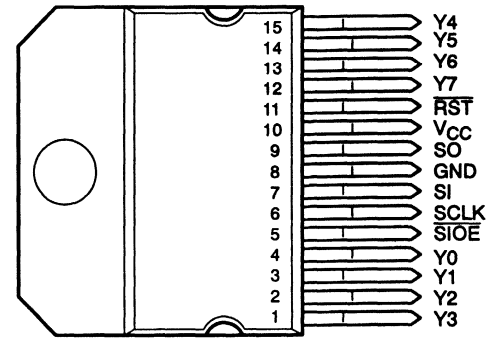
Figure 7. Data-Byte Transfer Timing

fault-conditions check

Open-circuit conditions on any output can be monitored or checked by programming that output off. After a short delay (microseconds), another control byte can be clocked into the device. If the diagnostic bit for that output comes back low, it indicates that the output is low and open circuited. A current overload condition is detected by programming an output on. After waiting an appropriate length of time, another byte is clocked into the TPIC2801A. The diagnostic bit clocked back from the TPIC2801A in the subsequent data transfer indicates a low output. If a high returns, a current overload is indicated. A quick overall check is done by clocking in a test control byte and after a sufficient time delay, clock in another control byte. The diagnostic data is exclusive ORed with the original control byte. If a fault condition exists, a high results from the subsequent exclusive OR.

- **8-Bit Serial-In Parallel-Out Driver**
- **1-A Output Current Capability Per Channel or 8-A Total Current**
- **Overcurrent Limiting and Out-of-Saturation Voltage Protection on Driver Outputs**
- **Contains Eight Open-Collector Saturating Sink Outputs With Low On-State Voltage**
- **High-Impedance Inputs With Hysteresis Are Compatible With TTL or CMOS Levels**
- **Exceptionally Low On-State Supply Current 50 mA**
- **Very Low Standby Power 20 mW Typical**
- **Status of Output Drivers May Be Monitored at Serial Output**
- **3-State Serial Output Permits Serial Cascading or Wire-AND Device Connections**
- **45-V Transient Clamping With Inductive Switching on Outputs, 20-mJ Rating Per Driver Output**

KV PACKAGE
(TOP VIEW)



The tab is electrically connected to GND.

description

The TPIC2802 octal intelligent-power switch is a monolithic BIDFET† integrated circuit designed to sink currents up to 1 A at 45 V simultaneously at each of eight driver outputs under serial input data control. Furthermore, use of a Darlington output structure enables an 80% reduction in the on-state supply current compared with earlier designs. Status of the individual driver outputs is available in serial data format. The driver outputs have overcurrent limiting and out-of-saturation voltage protection features. Applications include driving solenoids, relays, dc motors, lamps, and other medium-current or high-voltage loads.

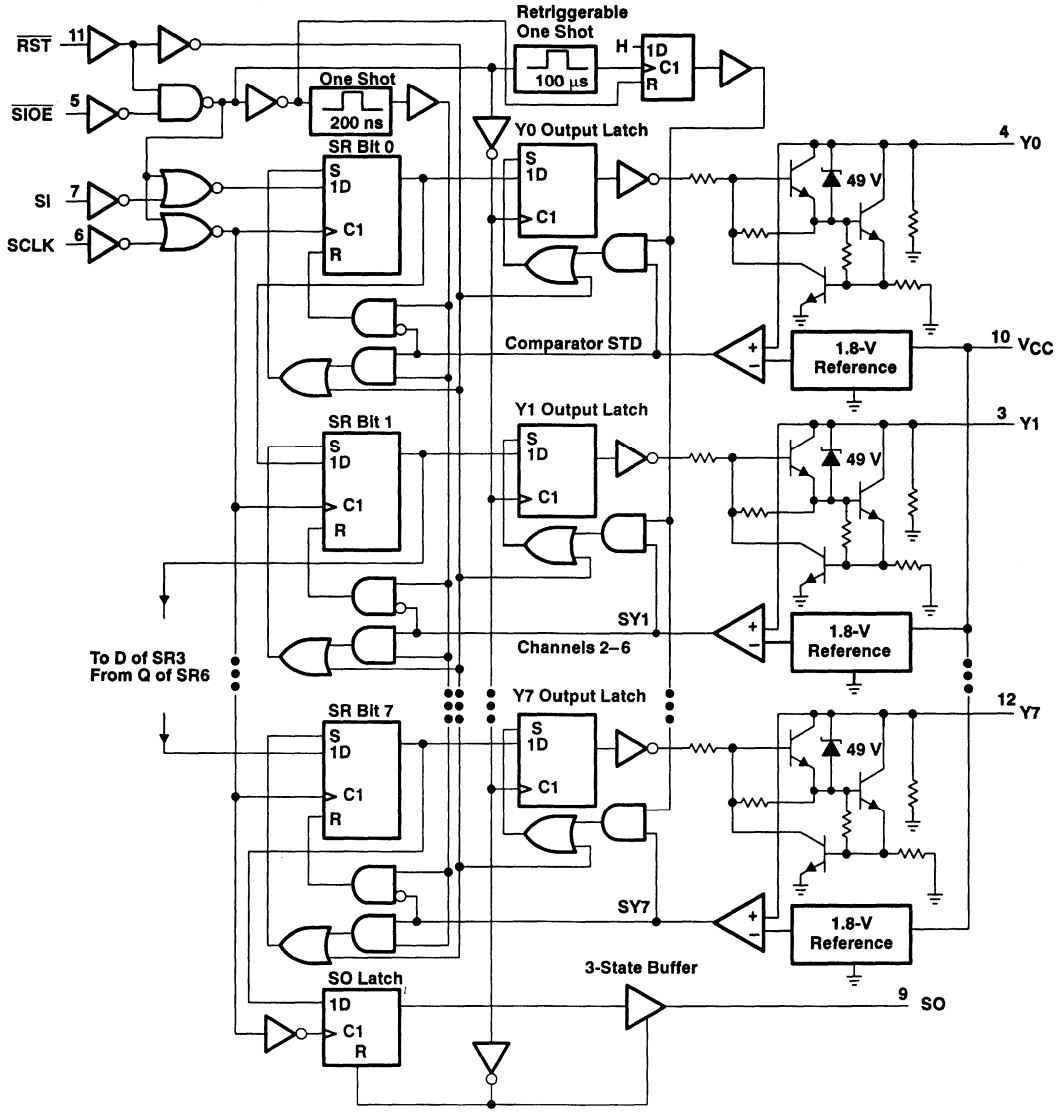
The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit parallel latch, which independently controls each of the eight Y-output drivers.

Data is entered into the device serially via the serial input (SI) and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic-high SI bit n turns the corresponding output driver (Y_n)off. A logic-low bit at SI turns the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of the serial clock (SCLK) input in 8-bit bytes with data for the Y7 output (most significant bit) first and data for Y0 output (least significant bit) last. Both SI and SCLK are active when the serial input-output enable ($\overline{SIOE}$) input is low and are disabled when $\overline{SIOE}$ is high.

Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal out-of-saturation threshold voltage reference level. The logic state of the comparator output is dependent upon whether the Y output is greater or smaller than the reference voltage level. While $\overline{SIOE}$ is held high, an activated driver output is unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level except when the internal unlatch enable is low and disabled. The high-to-low transition of $\overline{SIOE}$ transfers the logic state of the comparator output to the shift register.

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

functional block diagram

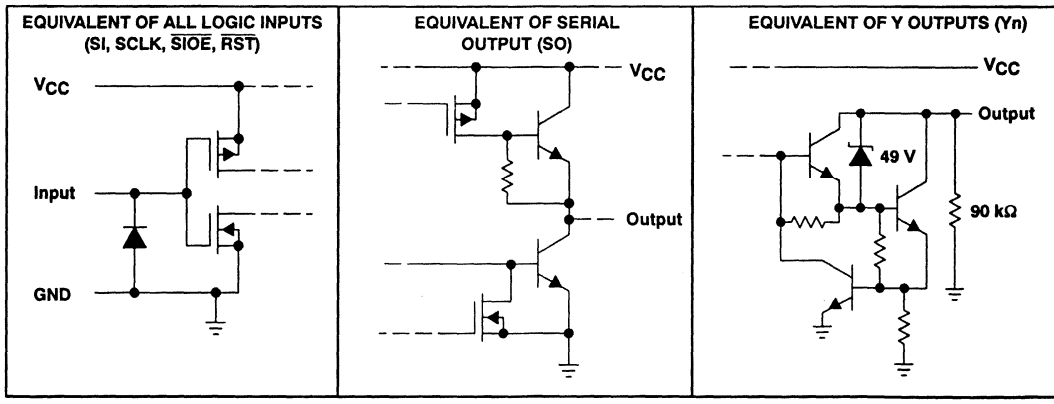


TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
GND	8		Ground. Common return for entire chip. The output current from this terminal is potentially as high as 8 A if all outputs are on. GND is used for both logic and power circuits.
$\overline{RST}$	11	I	Reset. An asynchronous reset is provided for the shift register and the parallel latches. This terminal is active when low and has no internal pullup. When active, it causes the power outputs to turn off. A power-on clear can be implemented using an RC network to V_{CC}.
SCLK	6	I	Serial clock. This terminal clocks the shift register. The serial output (SO) changes state on the rising edge of SCLK and serial input (SI) data is accepted on the falling edge.
SI	7	I	Serial Input. A high on this terminal programs a particular output to be off, and a low turns it on.
$\overline{SIOE}$	5	I	Serial input-output enable. Data is transferred from the shift registers to the power outputs on the rising edge of this signal. The falling edge of this signal parallel loads the output voltage sense bits from the power output stages into the shift register. The output driver SO is enabled when this terminal is low, provided $\overline{RST}$ is high.
SO	9	O	Serial output. This terminal is the serial 3-state output from the shift register and is in a high-impedance state when $\overline{SIOE}$ is high or $\overline{RST}$ is low. A high for a data bit on this terminal indicates that the corresponding power output (Y_n) is high. This means that the output was programmed to be off the last time a byte was input to the device or that the output faulted and was latched off by the output voltage-sense indicator. A low on this output indicates that the corresponding power output (Y_n) is low (on output stage or open-circuit condition).
V_{CC}	10		5-V supply voltage
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	4 3 2 1 15 14 13 12	O	Power outputs. These outputs are provided with current limiting and voltage sense for fault indication and protection. The nominal load current for these outputs is 500 mA, and the current limiting is set to a minimum of 1 A. The active-low outputs also have voltage clamps set at about 45 V for recirculation of inductive load current. Internal 90-kΩ pulldown resistors are provided at each output. These resistors hold the output low during an open-circuit condition.

schematic of inputs and outputs



All resistor and voltage values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... – 0.3 V to 7 V
Input voltage, V_I ..... 7 V
Output voltage range, SO ..... – 0.3 V to 7 V
Input current, I_I ..... –15 mA
Peak output sink current at Y, I_O repetitive, t_w = 10 ms, duty cycle = 50%,
(see Notes 2 and 3) ..... internally limited
Continuous output current at Y, I_O (see Note 3) ..... 1 A
Peak current through GND terminal: Nonrepetitive t_w = 0.2 ms ..... – 8 A
Repetitive t_w = 10 ms, duty cycle = 50% ..... – 6 A
Continuous current through GND terminal ..... – 4.5 A
Single-pulse avalanche energy rating, E_{AS} (see Note 4) ..... 20 mJ
Avalanche current, $I_{AS(max)}$ (see Note 5) ..... 1 A
Continuous dissipation at (or below) T_A = 25°C (see Note 6) ..... 3.575 W
Continuous dissipation at (or below) T_C = 75°C (see Note 6) ..... 25 W
Operating case or virtual-junction temperature range ..... – 55°C to 150°C
Storage temperature range ..... – 65°C to 150°C
Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network GND.
2. Each Y output is individually current limited with a typical overcurrent limit of about 1.8 A.
3. Multiple Y outputs of this device can conduct rated current simultaneously; however, power dissipation (average) over a short time interval must fall within the continuous dissipation range and the GND terminal current range.
4. V_{CC} = 20 V, starting T_J = 25°C, L = 310 mH, I_{AS} = 0.28 A.
5. V_{CC} = 10 V, starting T_J = 25°C, L = 8 mH, I_{AS} = 1 A (see Figure 6).
6. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. To avoid exceeding the maximum virtual-junction temperature, these ratings must not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	0.75 V_{CC}		5.25	V
Low-level input voltage, V_{IL}	–0.3		0.2 V_{CC}	V
Output voltage, $V_{O(off)}$			45	V
Continuous output current, $I_{O(on)}$			1	A
Operating case temperature, T_C	–40	25	105	°C

electrical characteristics over recommended operating virtual junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	All outputs on, I_O = 0.5 A at all outputs			50	mA
		All outputs off, T_J = 25°C		4	10	

electrical characteristics over recommended operating virtual junction temperature range (unless otherwise noted) (continued)

driver array outputs (Y0 to Y7)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OK}	Output clamp voltage	I_O = 0.5 A, Output programmed off and current shunted to ground		45	49		V
$V_{O(on)}$	On-state output voltage	With one output programmed on and conducting	I_{OL} = 0.175 A			1	V
			I_{OL} = 0.5 A		1	1.3	V
			I_{OL} = 0.75 A		1.2	1.5	V
			I_{OL} = 1 A, During unlatch disable		1.4	1.6	V
V_{TOS}	Out-of-saturation threshold voltage	With output programmed on and an overcurrent fault condition		1.6	1.8	2.1	V
$I_{O(off)}$	Off-state output current	V_O = 24 V with output programmed off				600	μA
$I_{O(cl)}$	Output current limit	V_O = 3 V with output programmed on		1	1.8		A
	Internal output pulldown resistor			40	90		kΩ

shift register (Inputs SI, $\overline{SCLK}$, SCLK, and $\overline{RST}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{T+}	Positive-going threshold voltage			0.75 V_{CC}	V
V_{T-}	Negative-going threshold voltage		0.1 V_{CC}		V
V_{hys}	Hysteresis voltage ($V_{T+} - V_{T-}$)		0.85	2.5	V
I_I	Input current	V_I = 0 to V_{CC}		±10	μA
C_i	Input capacitance	V_I = 0 to V_{CC}		20	pF

shift register (output SO)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	I_O = 1.6 mA			0.2	0.4	V
V_{OH}	High-level output voltage	I_O = – 0.8 mA		V_{CC} –1.3			V
I_O	Output current	V_O = 0 to V_{CC},	$\overline{SIOE}$ input high			±20	μA
C_o	Output capacitance	V_O = 0 to V_{CC},	$\overline{SIOE}$ input high			20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

timing requirements over recommended ranges of supply voltage and operating case temperature (see Figure 1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, SCLK	See Note 7	0	1	MHz
$t_{w(SCLKH)}$	Pulse duration, SCLK high		410		ns
$t_{w(SCLKL)}$	Pulse duration, SCLK low		410		ns
$t_{w(RST)}$	Pulse duration, $\overline{RST}$ low		1200		ns
t_{su1}	Setup time, $\overline{SIOE}$↓ before SCLK↑		1		μs
t_{su2}	Setup time, SCLK↓ before $\overline{SIOE}$↑		1		μs
t_{su3}	Setup time, SI high before SCLK↓		150		ns
t_{h1}	Hold time, SI low after SCLK↓		150		ns
t_r	Rise time, SCLK, SI, $\overline{SIOE}$			90	ns
t_f	Fall time, SCLK, SI, $\overline{SIOE}$			90	ns

NOTE 7: For cascaded operation, the clock pulse durations ($t_{w(SCLKL)}$ and $t_{w(SCLKH)}$) must be a minimum of 700 ns (giving a maximum clock frequency of 632 kHz).

thermal characteristics

PARAMETER		MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case temperature		3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient temperature		35	°C/W

switching characteristics over recommended ranges of supply voltage and operating case temperature

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{en}	Enable time	$\overline{SIOE}\downarrow$	SO	C_L = 20 pF, R_L = 1 kΩ, See Figure 2		1000	ns
t_{dis}	Disable time	$\overline{SIOE}\uparrow$	SO	C_L = 20 pF, R_L = 1 kΩ, See Figure 2		1000	ns
t_{d1}	Delay time, valid data	SCLK↑	SO	C_L = 200 pF, See Figure 3		550	ns
t_{d2}	Delay time, unlatch disable	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 5 Ω, See Figure 4	75	450	µs
$t_{r(SO)}$	Rise time		SO	C_L = 200 pF, See Figure 3		150	ns
$t_{f(SO)}$	Fall time		SO	C_L = 200 pF, See Figure 3		150	ns
$t_{d(on)}$	Delay time, turn on	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 28 Ω, I_{OL} = 500 mA, See Figure 5		10	µs
$t_{d(off)}$	Delay time, turn off	$\overline{SIOE}\uparrow$	Y_n	C_L = 20 pF, R_L = 28 Ω, I_{OL} = 500 mA, See Figure 5		10	µs
t_v	Valid time, SO output data remains valid after SCLK high	SCLK↑	SO	C_L = 200 pF, See Figure 3	0		ns

PARAMETER MEASUREMENT INFORMATION

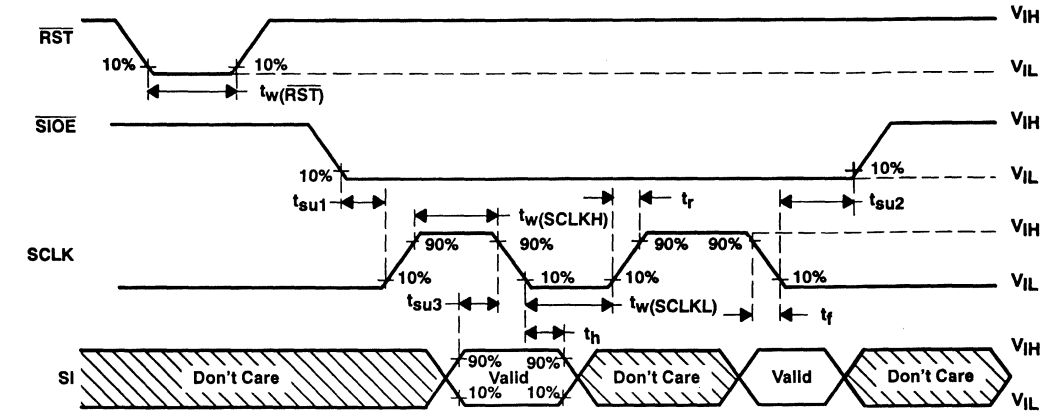
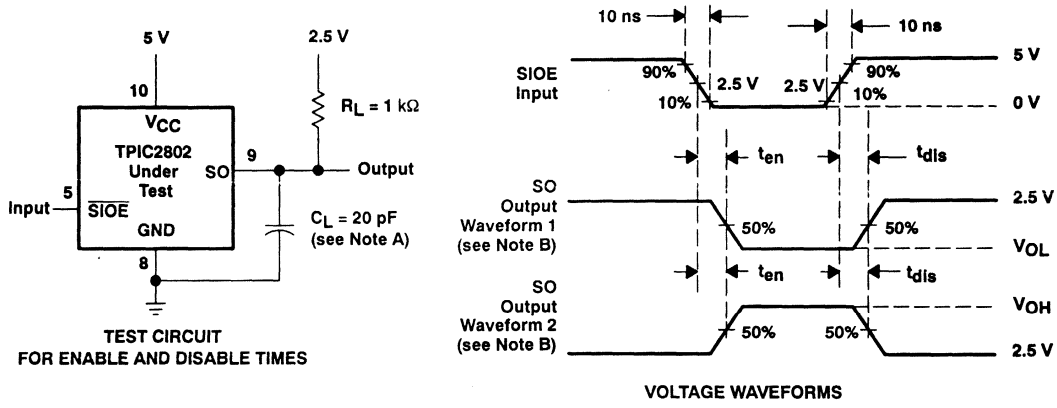


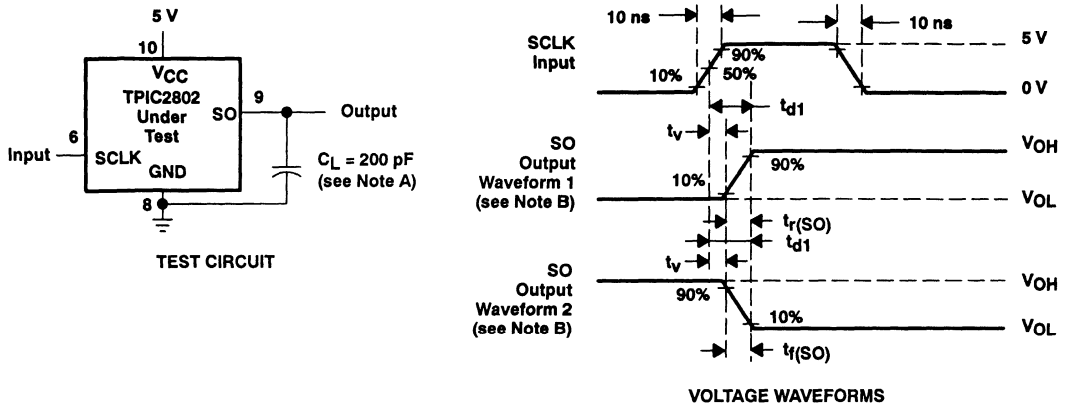
Figure 1. Input Timing Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control when $\overline{SIOE}$ is high. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

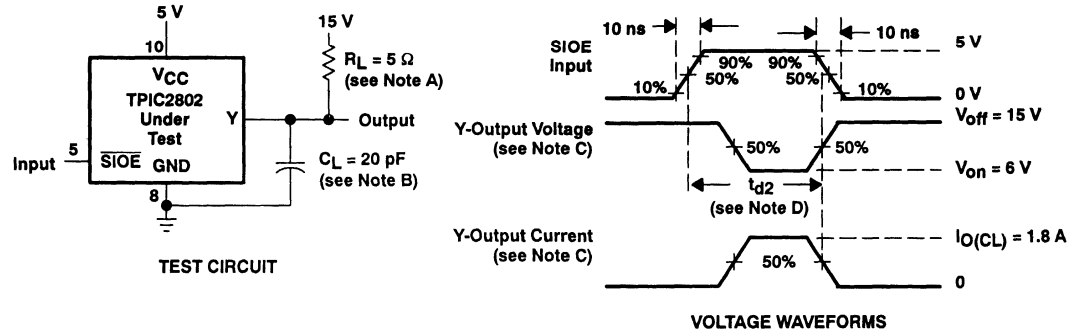
Figure 2. Test Circuit and Voltage Waveforms for Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION



NOTES: C. C_L includes probe and jig capacitance.
D. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from high to low. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

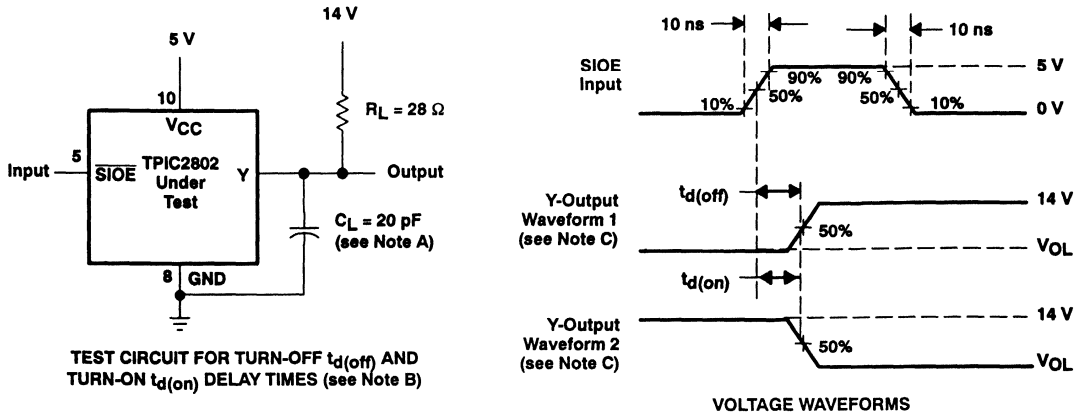
Figure 3. Test Circuit and Voltage Waveforms for Delay Times



NOTES: A. Load voltage V_S and load resistance R_L are selected such that on-state voltage at the Y output under test, V_{on} is greater than the maximum out-of-saturation hold voltage, V_{TOS}. Thus $V_{OL} = V_{on} > V_{TOS(max)} = 2.1$ V.
B. C_L includes probe and jig capacitance.
C. Output voltage and current waveforms are for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.
D. t_{d2} = delay until Y-output current goes off under fault condition.

Figure 4. Test Circuit and Voltage Waveforms for Unlatch Disable Delay

PARAMETER MEASUREMENT INFORMATION

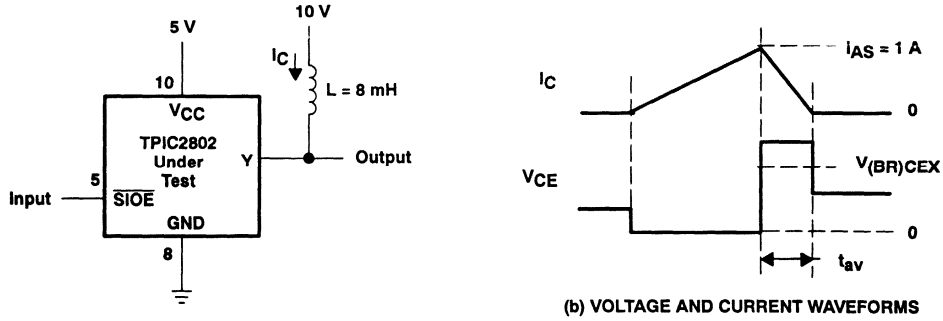


TEST CIRCUIT FOR TURN-OFF $t_{d(off)}$ AND TURN-ON $t_{d(on)}$ DELAY TIMES (see Note B)

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. $t_{d(off)} = t_{PLH}$, $t_{d(on)} = t_{PHL}$
C. Waveform 1 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from on to off. Waveform 2 is for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from off to on.

Figure 5. Test Current and Voltage and Current Waveforms for Turn-Off and Turn-On Delay Times



(a) TEST CIRCUIT

(b) VOLTAGE AND CURRENT WAVEFORMS

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

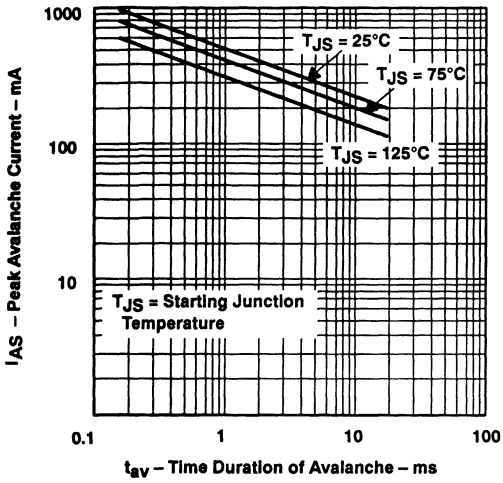


Figure 7

PEAK AVALANCHE CURRENT
vs
JUNCTION TEMPERATURE

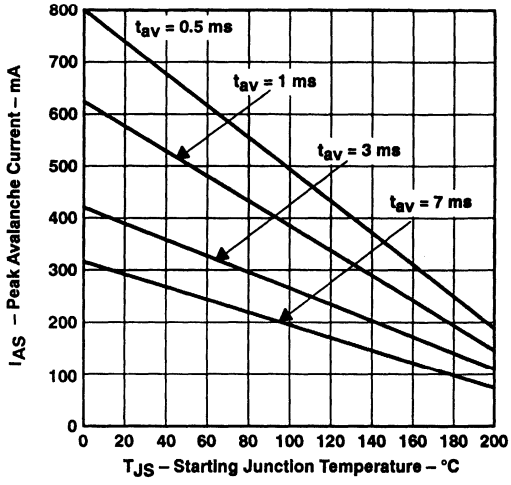


Figure 8

APPLICATION INFORMATION

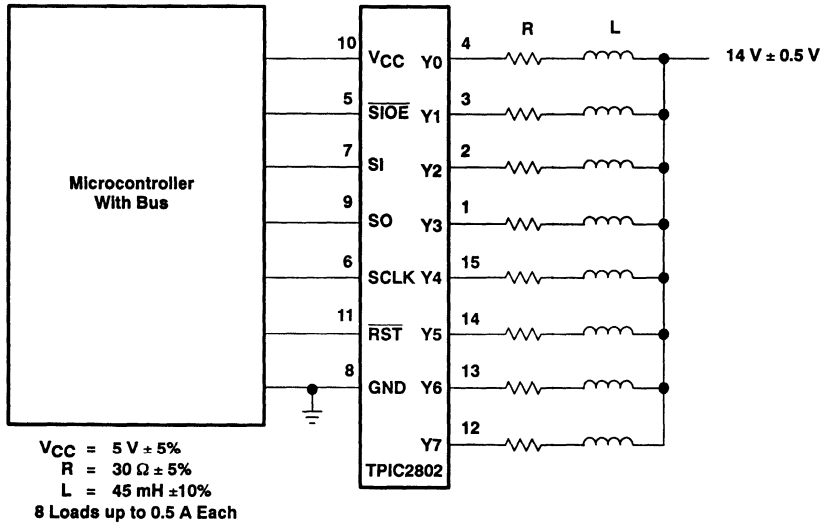


Figure 9. Microcontroller Driving Eight Loads Using a TPIC2802 for Load Interface

PRINCIPLES OF OPERATION

timing data transfer

Figure 10 shows the overall 8-bit data-byte transfer to and from the TPIC2802 interface bus. The logic state of the eight output drivers, Y0 through Y7, is latched into the shift register at time t_0 on the high-to-low transition of $\overline{SIOE}$. Therefore, the SO output data (DY0, DY1 . . .) represent the conditions at the Y-driver outputs at time t_0. The data at the SO output is updated on the low-to-high transition of SCLK.

Input data present at the SI input is clocked into the shift register on the high-to-low transition of SCLK. As shown in Figure 10 on the SI input, input data DI7 is clocked at time t_1, DI6 is clocked at time t_2, etc. Eight SCLK pulses are used to serially load the eight bits of new data into the device. After all the new data is serially loaded, the low-to-high transition of SIOE parallel loads the new data to the eight driver output latches, which in turn directly control the eight Y-driver outputs.

An unlimited amount of data can be shifted through the shift register (into the SI and out the SO), and this allows other devices to be cascaded in a daisy chain with the TPIC2802. Once the last data bit has been shifted into the TPIC2802, the $\overline{SIOE}$ input is pulled high. The clock (SCLK) input is low at both transitions of the $\overline{SIOE}$ input to avoid any false clicking of the shift register. The SCLK input is gated by the $\overline{SIOE}$ input, so the SCLK input is ignored whenever $\overline{SIOE}$ is high. At the rising edge of $\overline{SIOE}$, the shift register data is latched into the parallel latch and the output stages are actuated by the new data. An internal 100-µs delay timer is also started on this rising edge. During the time delay, the outputs are protected only by the analog current-limiting circuits, since the resetting of the parallel latches by fault conditions are inhibited during this time period. This allows the device to overcome any high switching currents that can flow during turn-on. Once the delay ends, the output voltages are sensed by the comparators and any output voltages higher than nominally 1.8 V are latched off.

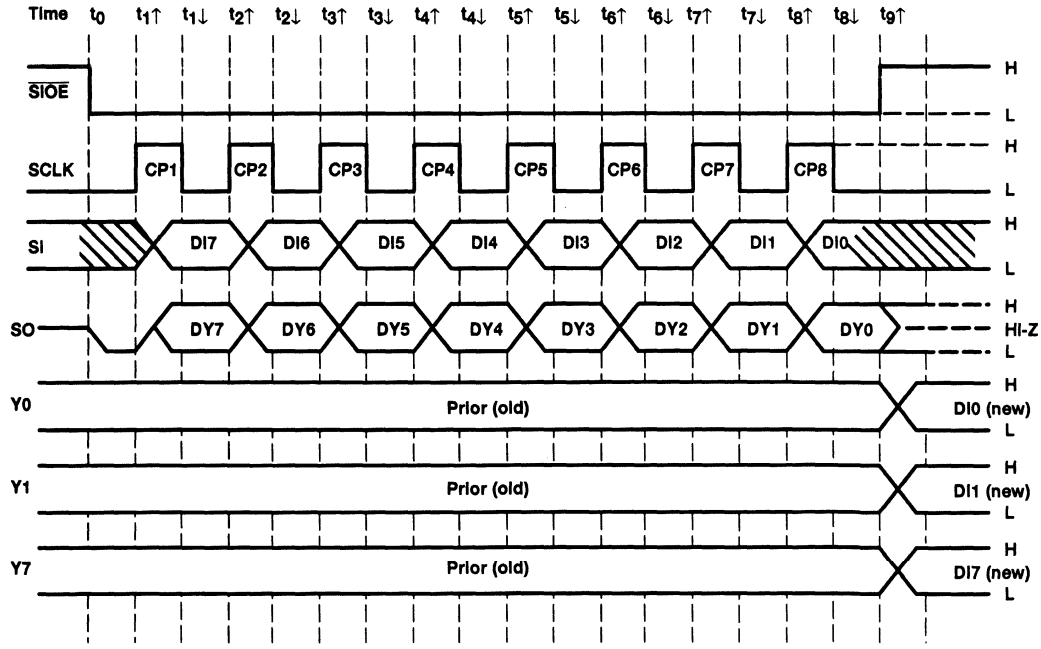


Figure 10. Data-Byte Transfer Timing

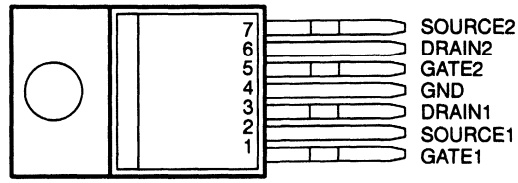
fault-conditions check

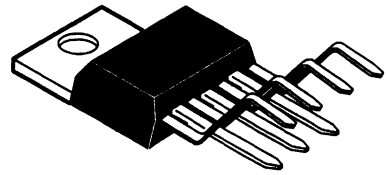
Open-circuit conditions on any output can be monitored or checked by programming that output off. After a short delay (microseconds), another control byte can be clocked into the device. If the diagnostic bit for that output comes back low, it indicates that the output is low and open circuited. A current overload condition can be detected by programming an output on. After waiting an appropriate length of time, another byte is clocked into the TPIC2802. The diagnostic bit clocked back from the TPIC2802 in the subsequent data transfer indicates a low output. If a high returns, a current overload is indicated. A quick overall check can be done by clocking in a test control byte and after a sufficient time delay, clock in another control byte. The diagnostic data is exclusive ORed with the original control byte. If a fault condition exists, a high results from the subsequent exclusive OR.

SLDS051 – D4046, SEPTEMBER 1992

- **Two 7.5-A Independent Output Channels, Continuous Current Per Channel**
- **Low $r_{DS(on)}$ . . . 0.09 Ω Typical**
- **Output Voltage . . . 60 V**
- **Pulsed Current . . . 15 A Per Channel**
- **Avalanche Energy . . . 120 mJ**

KV PACKAGE
(TOP VIEW)





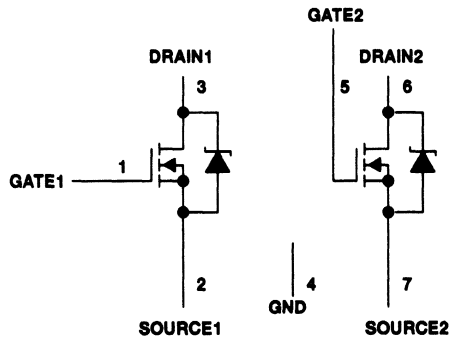
To ensure correct device operation, the source and the drain of the same transistor cannot simultaneously be taken below GND.

The tab is electrically connected to GND.

description

The TPIC5201 is a power monolithic DMOS array that consists of dual independent N-channel enhancement-mode DMOS transistors.

schematic



absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Source-GND voltage	60 V
Drain-GND voltage	60 V
Gate-source voltage, V_{GS}	±20 V
Continuous source-drain diode current	7.5 A
Pulsed drain current, each output, all outputs on, I_D (see Note 1)	15 A
Continuous drain current, each output, all outputs on	7.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	120 mJ
Continuous power dissipation at (or below) T_A = 25°C (see Note 2)	2 W
Continuous power dissipation at (or below) T_C = 75°C, all outputs on (see Note 2)	31 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. Pulse duration = 10 ms, duty cycle = 6%

2. For operation above 25°C free-air temperature, derate linearly at the rate of 16 mW/°C. For operation above 75°C case temperature, and with all outputs conducting, derate linearly at the rate of 0.42 W/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

electrical characteristics, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 μA, V_{GS} = 0		60			V
V_{TGS}	Gate-source threshold voltage	I_D = 1 mA, V_{DS} = V_{GS}		1.2	1.75	2.4	V
$V_{DS(on)}$	Drain-source on-state voltage	I_D = 7.5 A, V_{GS} = 15 V, See Notes 3 and 4			0.68	0.94	V
V_{DSS}	Zero-gate-voltage drain current	V_{DS} = 48 V, V_{DS} = 0	T_C = 25°C		0.07	1	μA
			T_C = 125°C		1.3	10	
I_{GSSF}	Forward gate current, drain short circuited to source	V_{GS} = 20 V, V_{DS} = 0			10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	V_{GS} = −20 V, V_{DS} = 0			10	100	nA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{GS} = 15 V, I_D = 7.5 A, See Notes 3 and 4 and Figures 5 and 6	T_C = 25°C		0.09	0.125	Ω
			T_C = 125°C		0.15	0.21	
g_{fs}	Forward transconductance	V_{DS} = 15 V, I_D = 5 A, See Notes 3 and 4		2.5	4.7		S
C_{iss}	Short-circuit input capacitance, common source	V_{DS} = 25 V, V_{GS} = 0, f = 300 kHz			490		pF
C_{oss}	Short-circuit output capacitance, common source				285		
C_{rss}	Short-circuit reverse transfer capacitance, common source				90		

NOTES: 3. Technique should limit $T_J - T_C$ to 10°C maximum.
4. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-drain diode characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SD}	Forward on voltage	I_S = 7.5 A, V_{GS} = 0, di/dt = 100 A/μs, V_{DS} = 48 V, See Figure 1		0.8	1.3	V
t_{rr}	Reverse-recovery time			200		ns
Q_{RR}	Total source-drain diode charge			1.5		μC

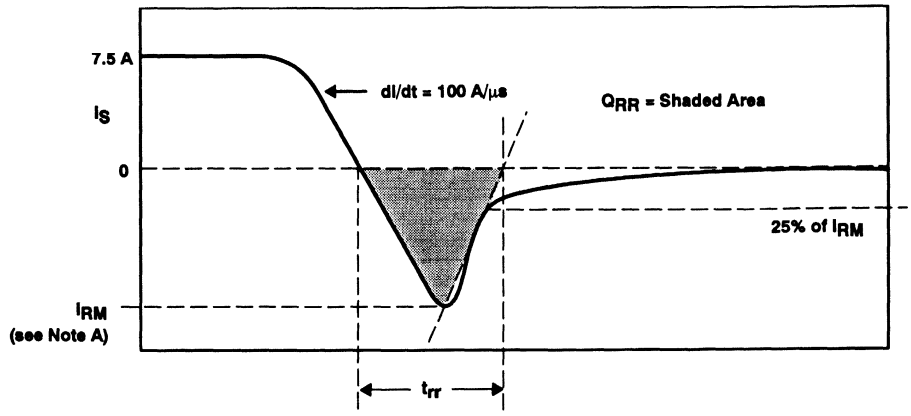
resistive-load switching characteristics, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time	V_{DD} = 25 V, R_L = 6.7 Ω, t_{en} = 10 ns, t_{dis} = 10 ns, See Figure 2		12		ns
t_r	Rise time			43		
$t_{d(off)}$	Turn-off delay time			100		
t_f	Fall time			5		
Q_g	Total gate charge	V_{DD} = 48 V, I_D = 2.5 A, V_{GS} = 15, See Figure 3		13.6	18	nC
Q_{gs}	Gate-source charge			8.3	11	
Q_{gd}	Gate-drain charge			5.3	7	
L_D	Internal drain inductance			7		nH
L_S	Internal source inductance			7		

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power			62.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	All outputs with equal power			2.4	°C/W
		One output dissipating power			3.3	°C/W

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain Diode

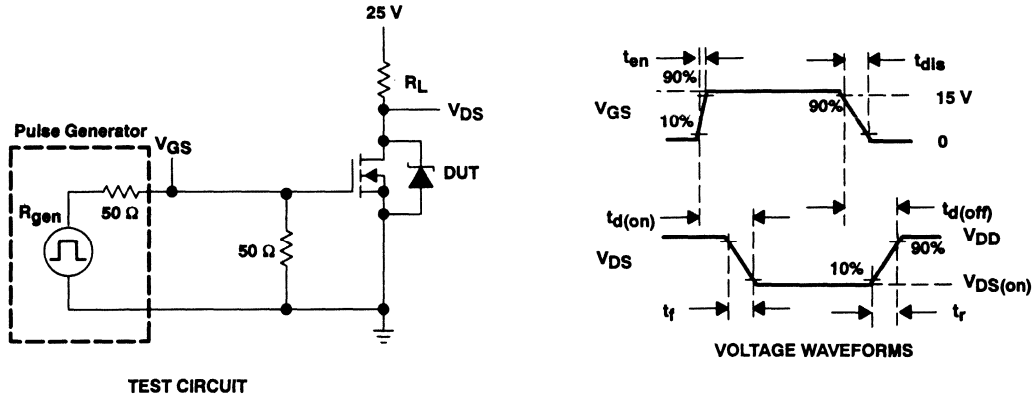


Figure 2. Resistive Switching

PARAMETER MEASUREMENT INFORMATION

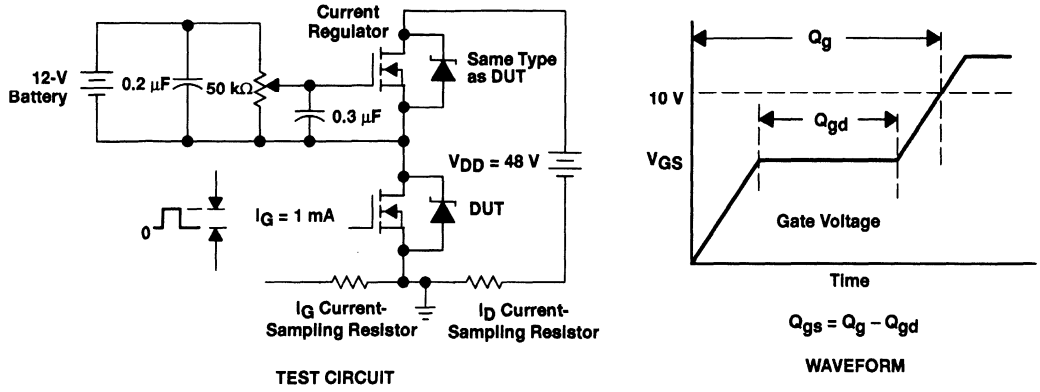
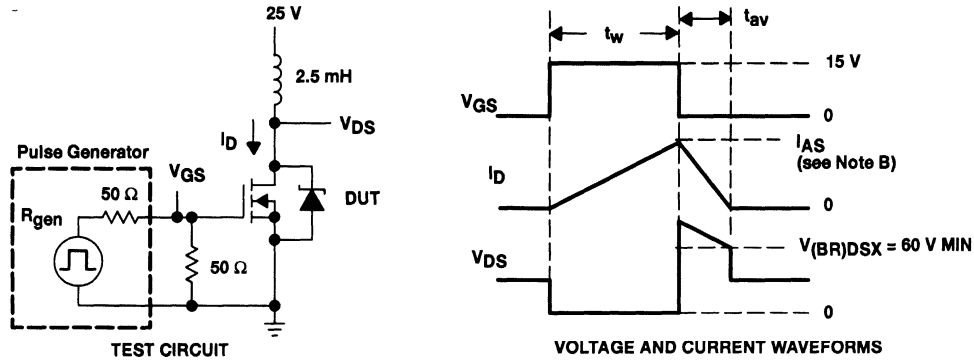


Figure 3. Gate Charge Test Circuit and Waveform



NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 7.5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 120$ mJ min.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
CASE TEMPERATURE

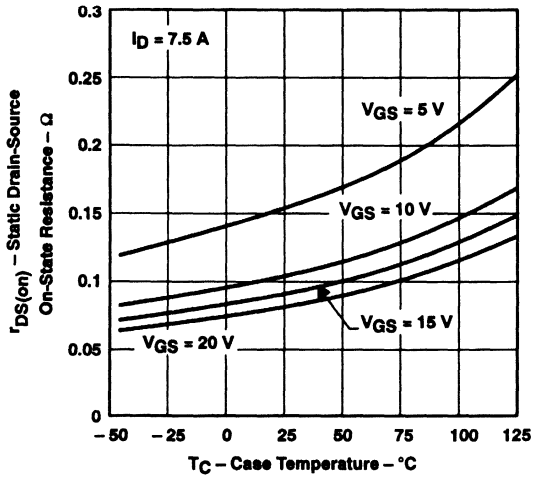


Figure 5

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

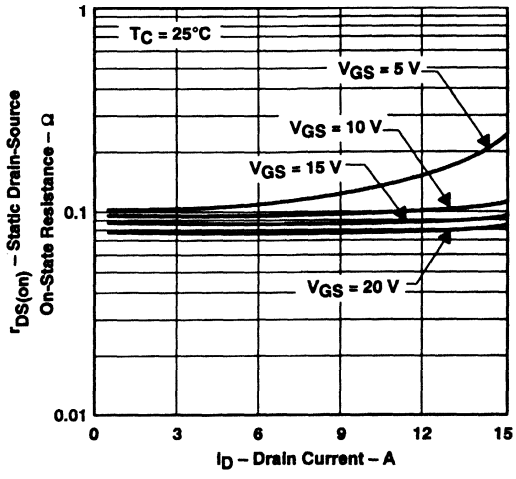


Figure 6

DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE

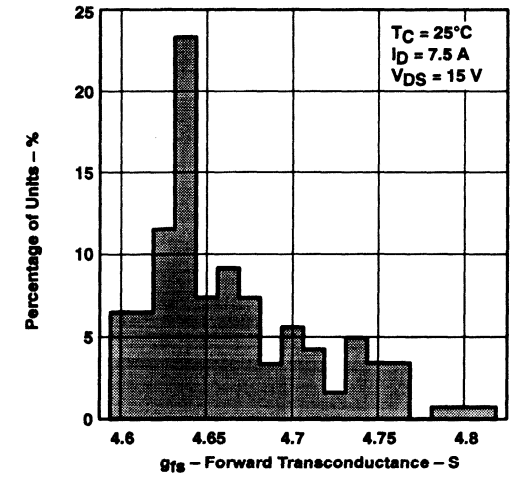


Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

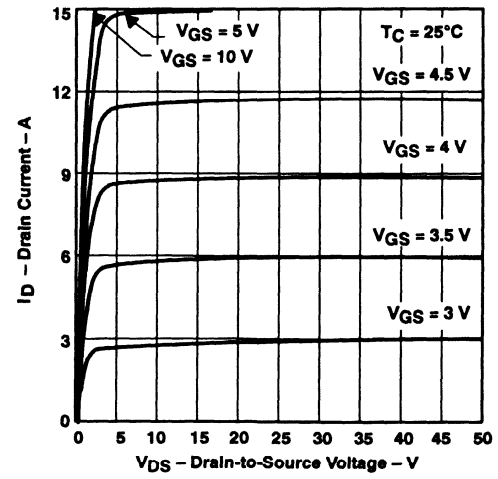


Figure 8

TYPICAL CHARACTERISTICS

GATE-SOURCE THRESHOLD VOLTAGE
vs
CASE TEMPERATURE

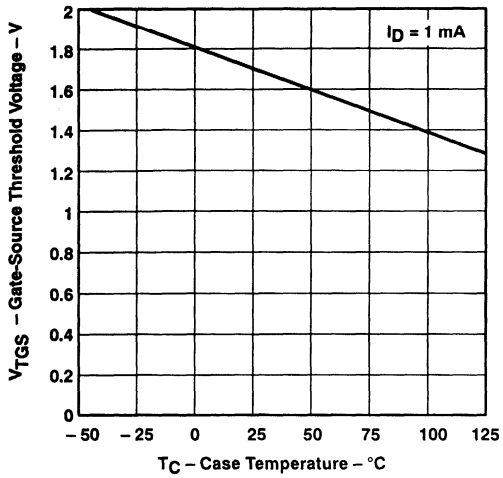


Figure 9

SOURCE-DRAIN DIODE CURRENT
vs
SOURCE-DRAIN VOLTAGE

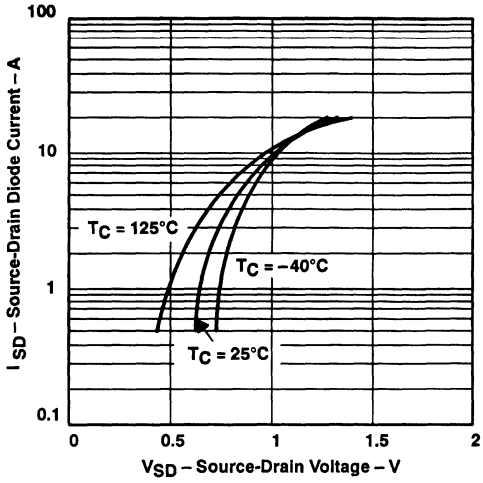


Figure 10

GATE-SOURCE VOLTAGE
vs
GATE CHARGE

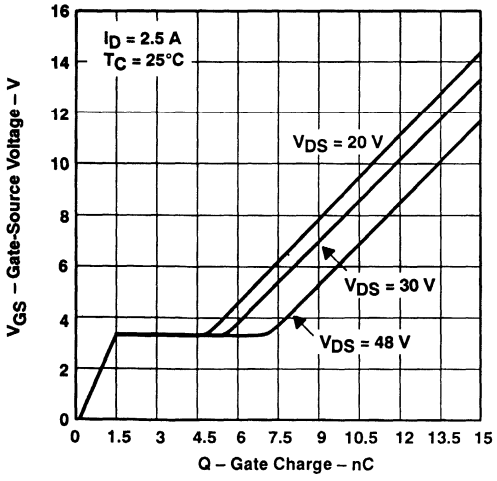


Figure 11

REVERSE-RECOVERY TIME
vs
REVERSE dI/dt

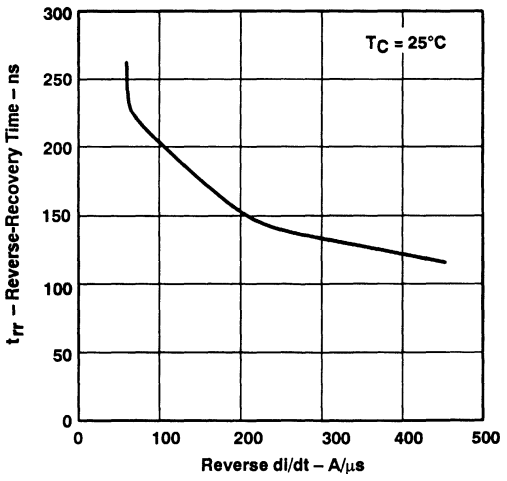


Figure 12

TYPICAL CHARACTERISTICS

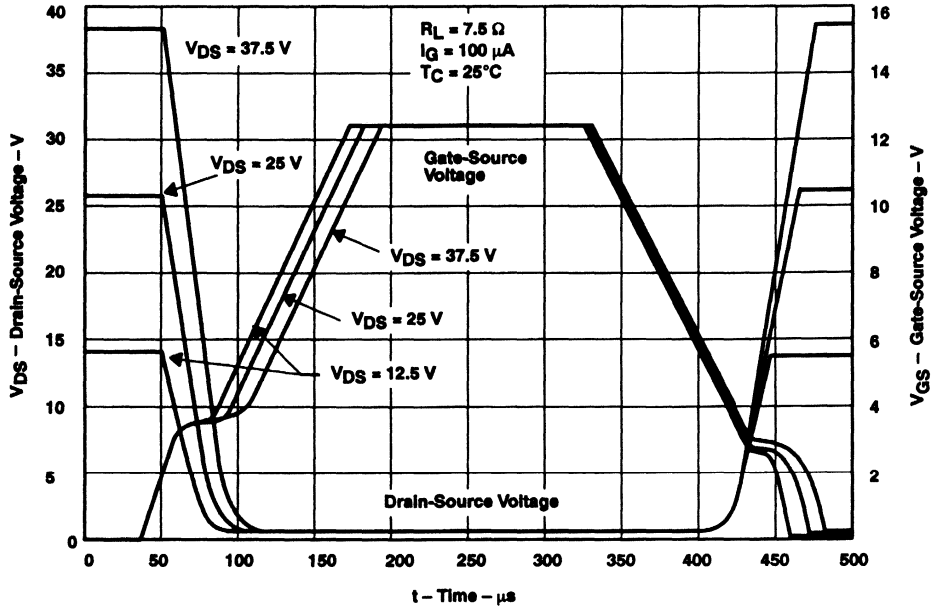


Figure 13. Resistive Switching Waveforms

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT vs DRAIN-SOURCE VOLTAGE

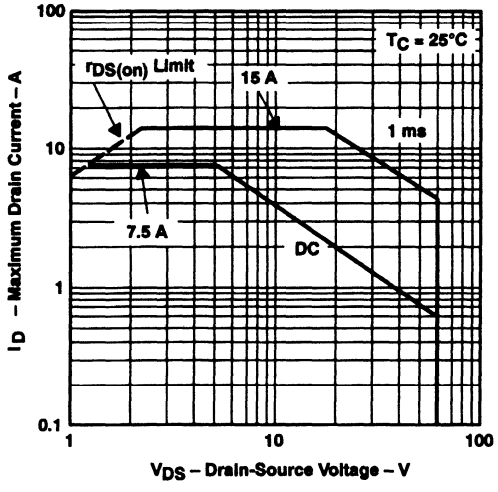


Figure 14

MAXIMUM PEAK AVALANCHE CURRENT vs TIME DURATION OF AVALANCHE

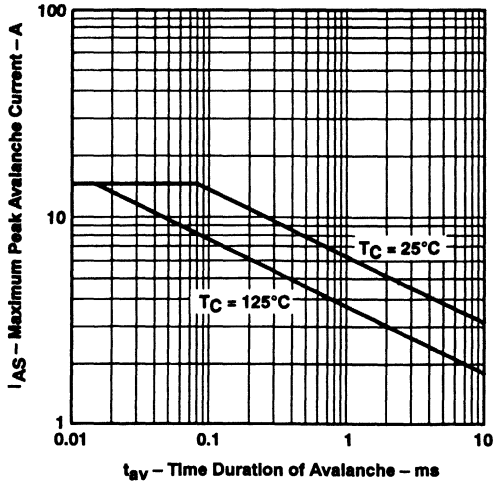
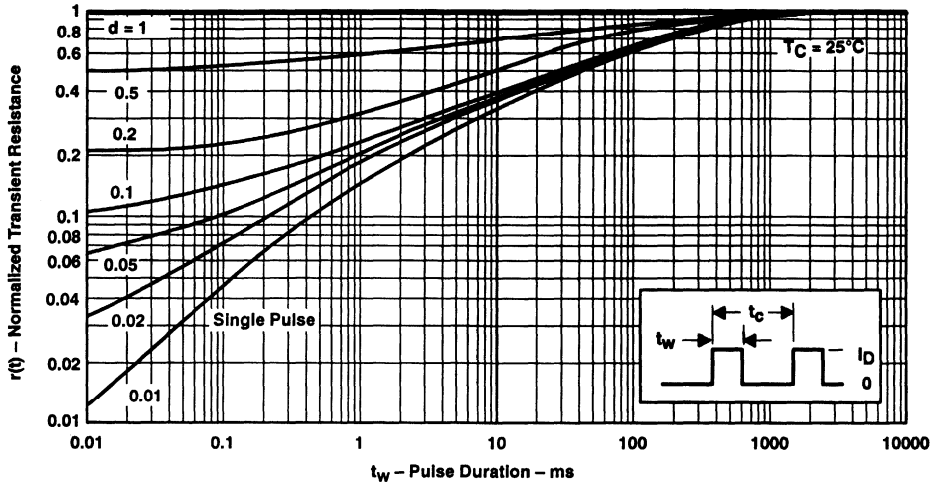


Figure 15

THERMAL INFORMATION

**NORMALIZED TRANSIENT THERMAL IMPEDANCE
vs
SQUARE-WAVE PULSE DURATION**

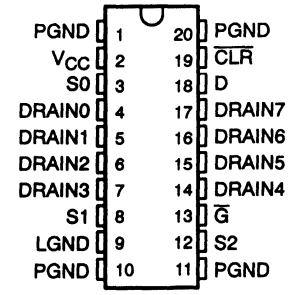


NOTES: $Z_{\theta JC}(t) = r(t)\ R_{\theta JC}$
t_w = pulse duration
t_c = period
d = duty cycle = t_w/t_c

Figure 16

- **Low $r_{DS(on)}$ . . . 1.3 Ω Typical**
- **Avalanche Energy . . . 75 mJ**
- **Eight Power DMOS Transistor Outputs of 250-mA Continuous Current**
- **1.5-A Pulsed Current Per Output**
- **Output Clamp Voltage at 45 V**
- **Four Distinct Function Modes**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)



description

This power logic 8-bit addressable latch controls open-drain DMOS transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of storing single-line data in eight addressable latches and 3-to-8 decoder or demultiplexer with active-low DMOS outputs.

FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
$\overline{CLR}$	$\overline{G}$	D			
H	L	H	L	Q_{io}	Addressable Latch
H	L	L	H	Q_{io}	
H	H	X	Q_{io}	Q_{io}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

LATCH SELECTION TABLE

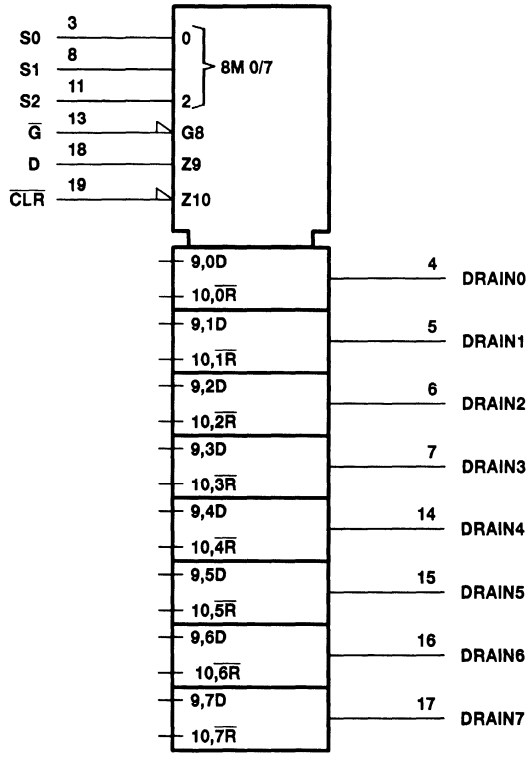
SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1, 10, 11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 9, logic ground (LGND) and pins 1, 10, 11, and 20, power ground (PGND) must be externally made in a manner that reduces crosstalk between the logic and load circuits.

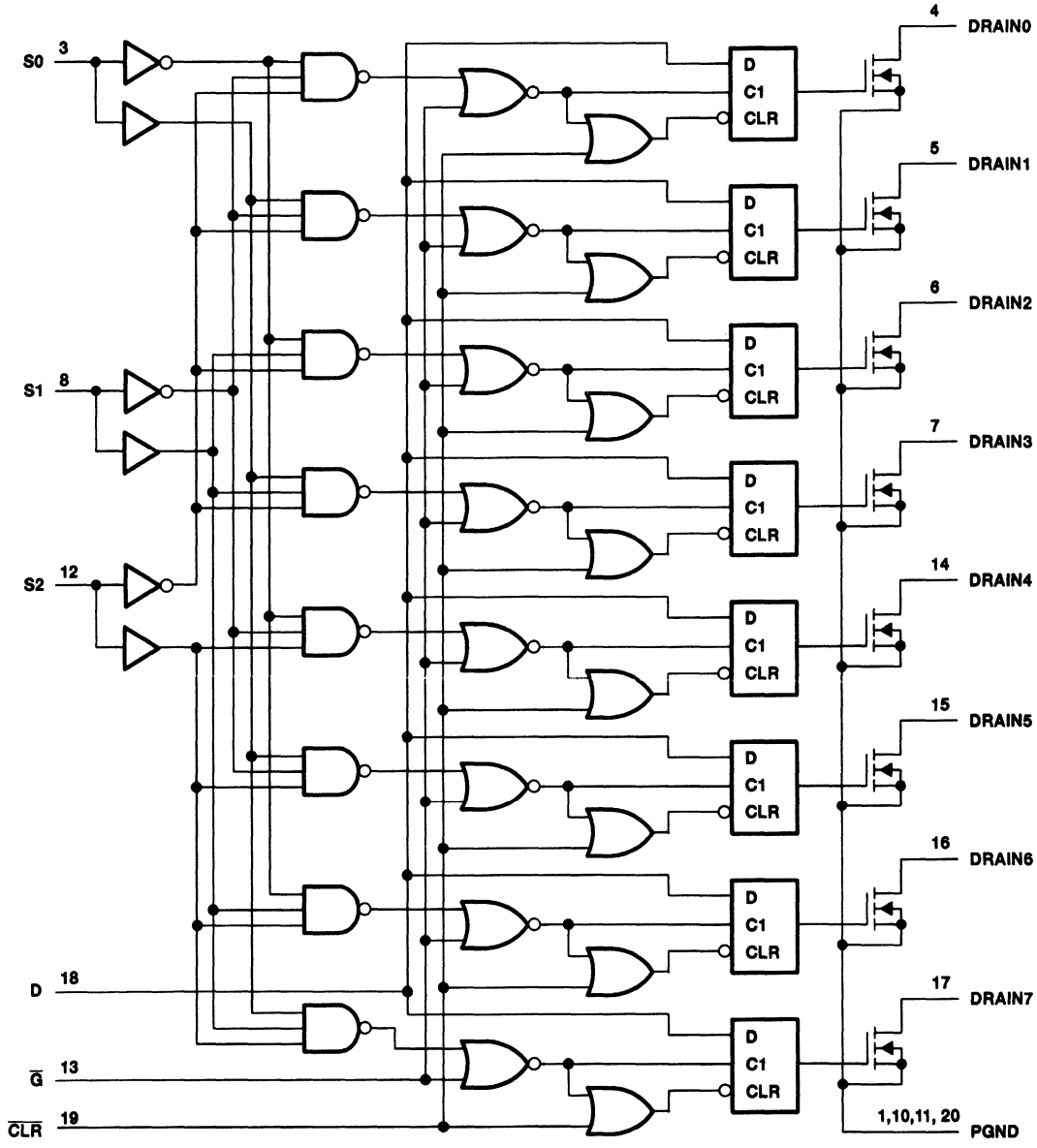
The TPIC6259 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic symbol†

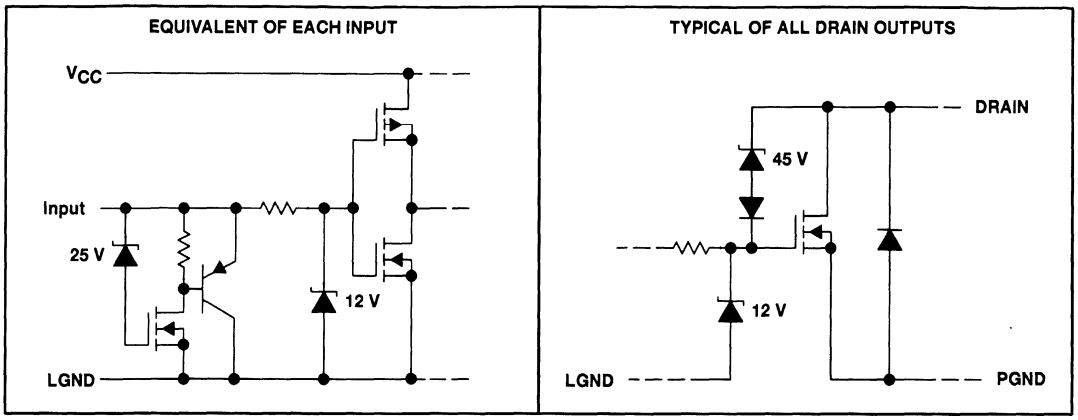


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	250 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Note 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total dissipation	See Dissipating Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
4. DRAIN supply voltage = 15 V, starting junction temperature, (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−1.8	1.5	A
Setup time, D high before $\overline{G}\uparrow$, t_{su} (see Figure 2)	10		ns
Hold time, D high after $\overline{G}\uparrow$, t_h (see Figure 2)	5		ns
Pulse duration, t_w (see Figure 2)	15		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, $V_I = V_{CC}$				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				−1	µA
I_{CC}	Logic supply current	I_O = 0, All inputs low			15	100	µA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, $I_N = I_D$, T_C = 85°C, See Notes 5, 6, and 7			250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 8 and 9		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from D	C_L = 30 pF, I_D = 250 mA, See Figures 1, 2, and 10		625		ns
t_{PHL}	Propagation delay time, high-to-low-level output from D			140		ns
t_r	Rise time, drain output			650		ns
t_f	Fall time, drain output			400		ns
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION

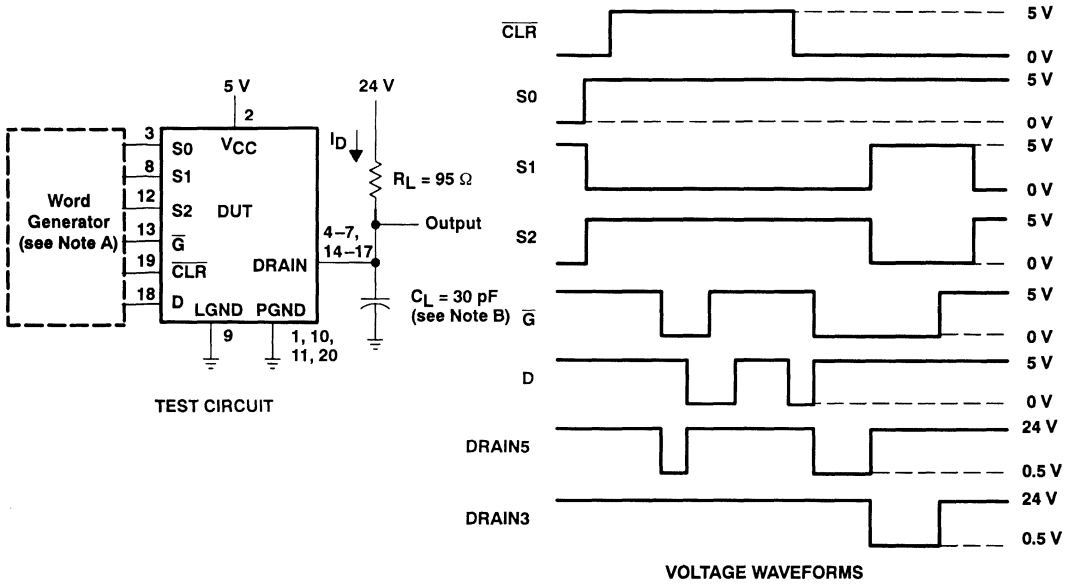


Figure 1. Typical Operation Mode

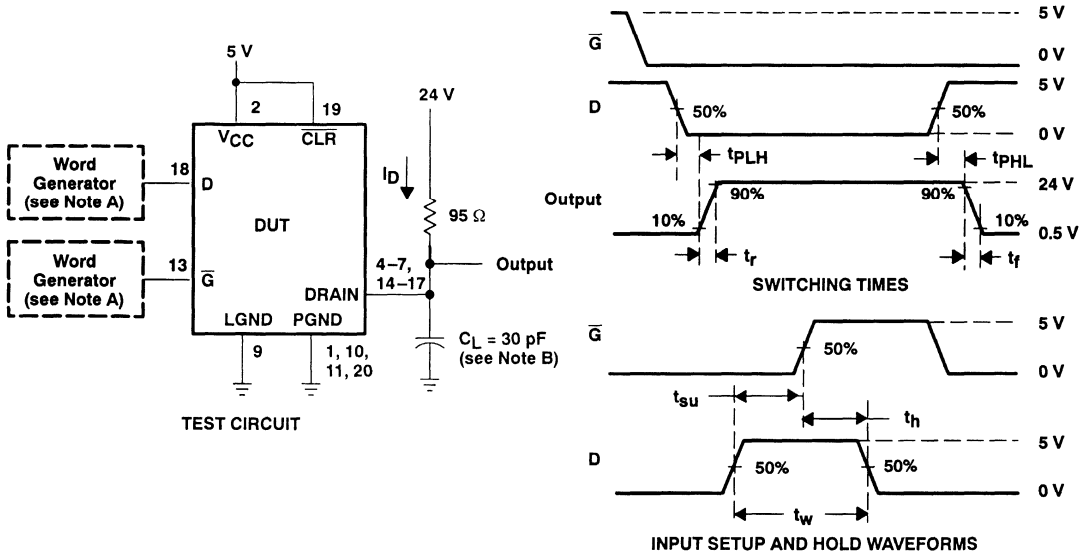
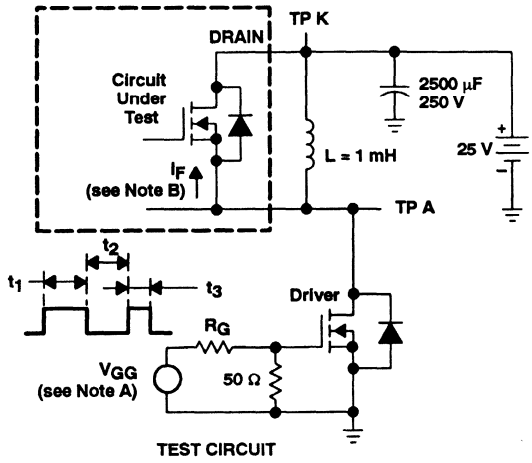


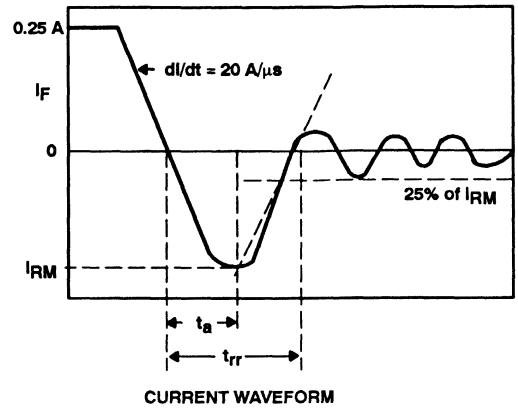
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

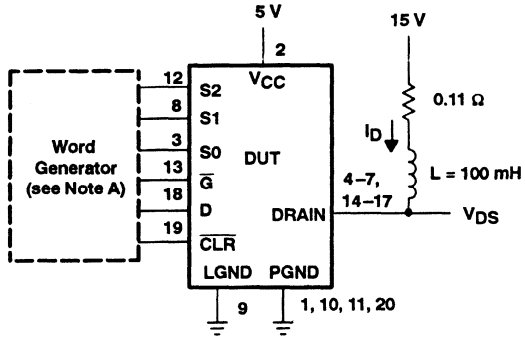


CURRENT WAVEFORM

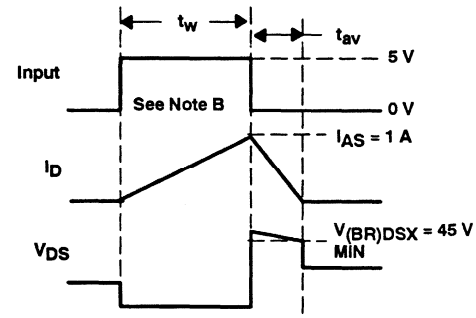
NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.

B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

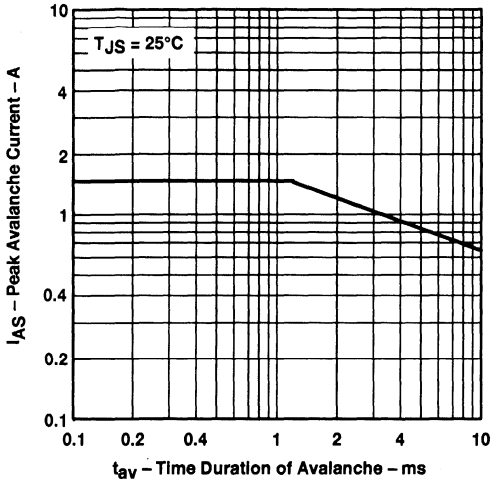


Figure 5

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

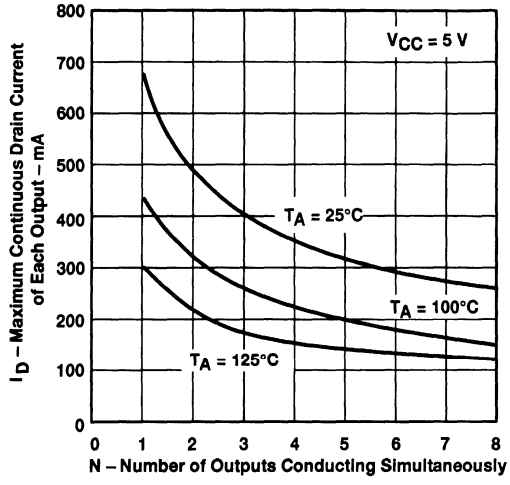


Figure 6

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

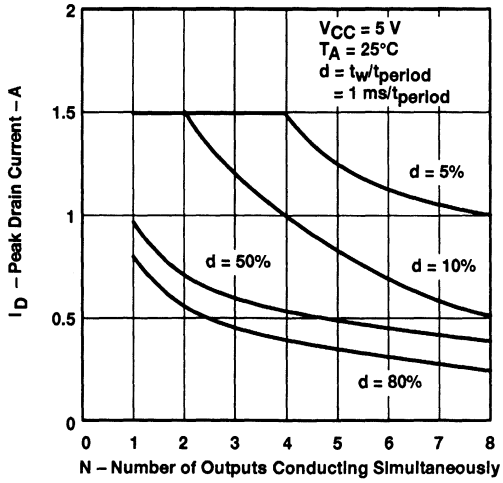


Figure 7

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

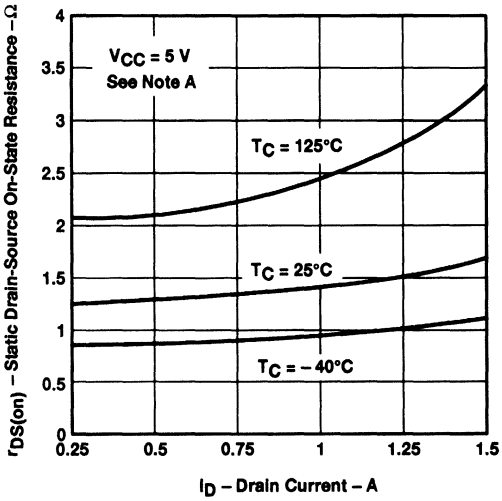


Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

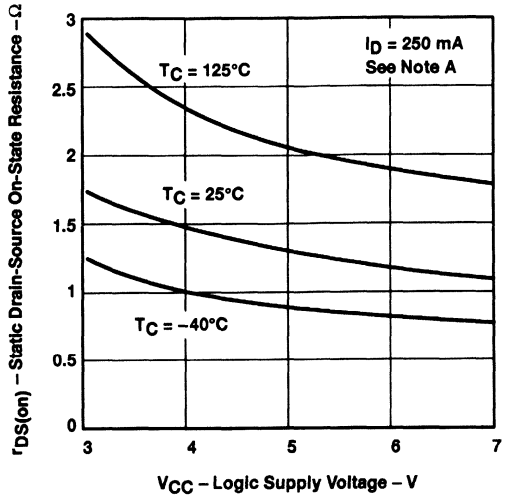


Figure 9

SWITCHING TIME vs FREE-AIR TEMPERATURE

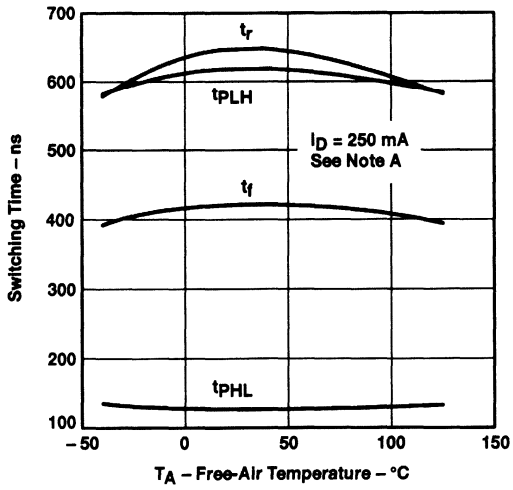
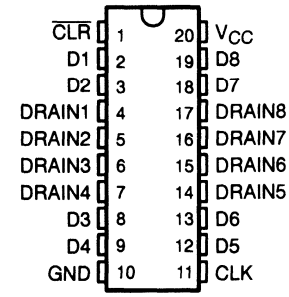


Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

- **Low $r_{DS(on)}$ . . . 1.3 Ω Typical**
- **Avalanche Energy . . . 75 mJ**
- **Eight Power DMOS Transistor Outputs of 250-mA Continuous Current**
- **1.5-A Pulsed Current Per Output**
- **Output Clamp Voltage up to 45 V**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)



description

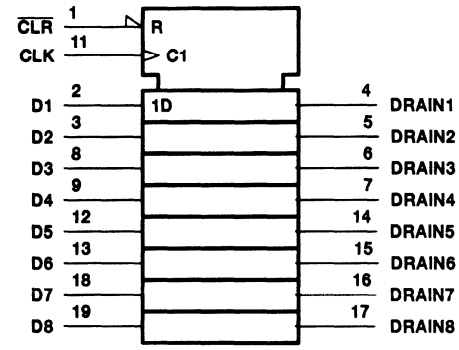
The TPIC6273 is a monolithic, high-voltage, high-current, power logic octal D-type latch with DMOS transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

The TPIC6273 contains eight positive-edge-triggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS transistor output.

When clear ($\overline{CLR}$) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous $\overline{CLR}$ is provided to turn all eight DMOS-transistor outputs off.

The TPIC6273 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic symbol†



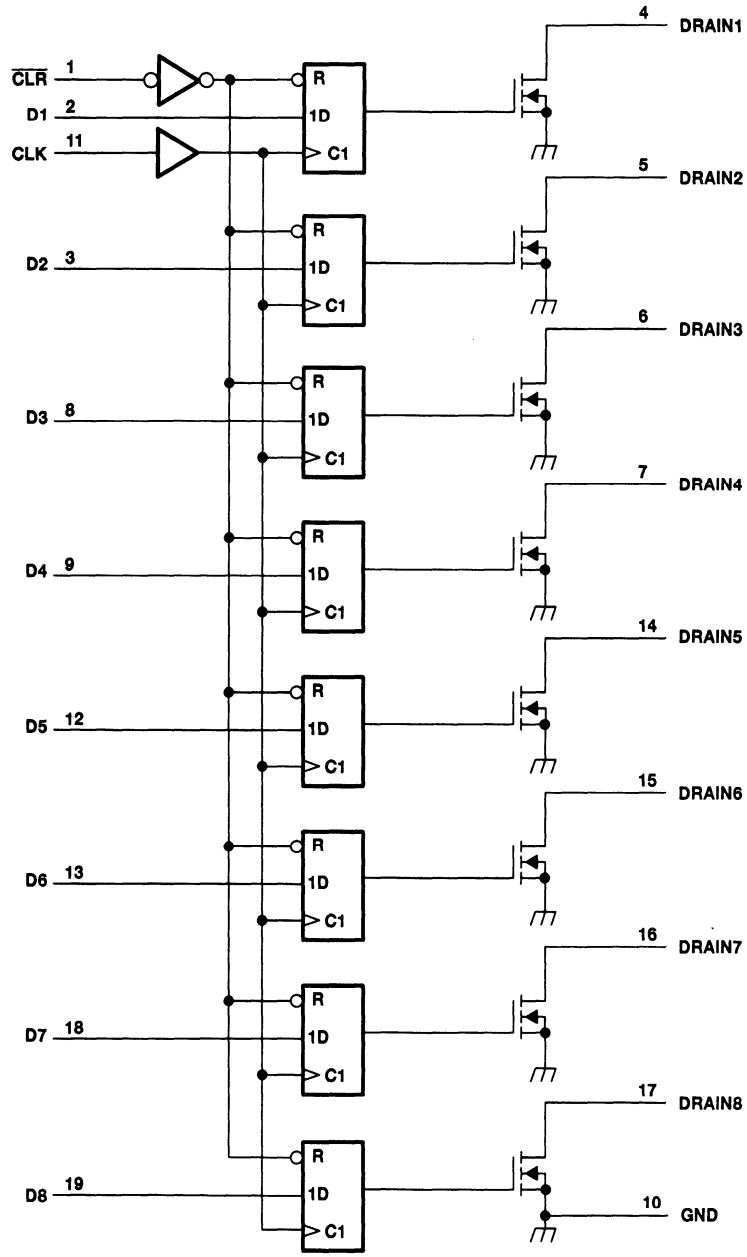
† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(each channel)

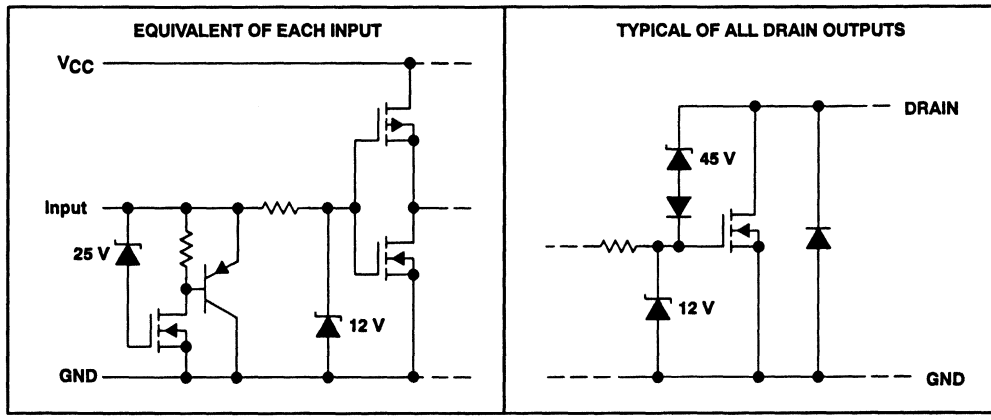
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	DRAIN
L	X	X	H
H	↑	H	L
H	↑	L	H
H	L	X	Latched

H = high level, L = low level, X = irrelevant

logic diagram, total device (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	250 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 μs, duty cycle ≤ 2%
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−1.8	1.5	A
Setup time, t_{su}, D high before CLK↑ (see Figure 2)	10		ns
Hold time, t_h, D high after CLK↑ (see Figure 2)	15		ns
Pulse duration, t_w (see Figure 2)	25		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				−1	µA
I_{CC}	Logic supply current	I_O = 0, All inputs low			15	100	µA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C	See Notes 5, 6, and 7		250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 8 and 9		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

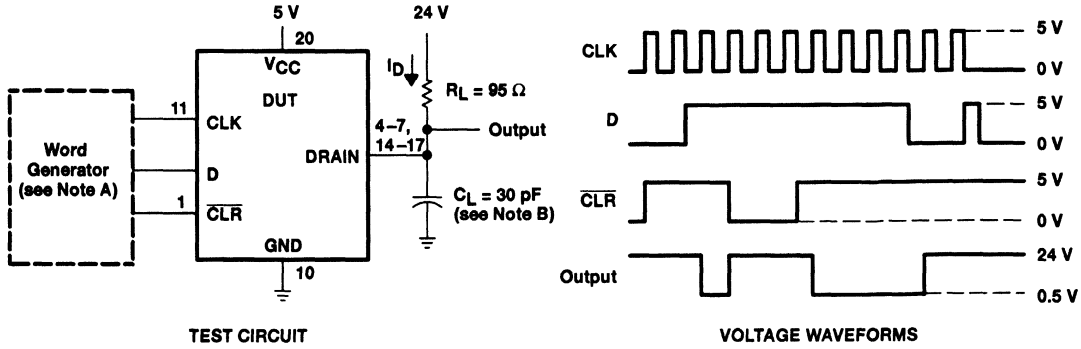
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from CLK	C_L = 30 pF, I_D = 250 mA, See Figures 1, 2, and 10		625		ns
t_{PHL}	Propagation delay time, high-to-low-level output from CLK			150		ns
t_r	Rise time, drain output			675		ns
t_f	Fall time, drain output			400		ns
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

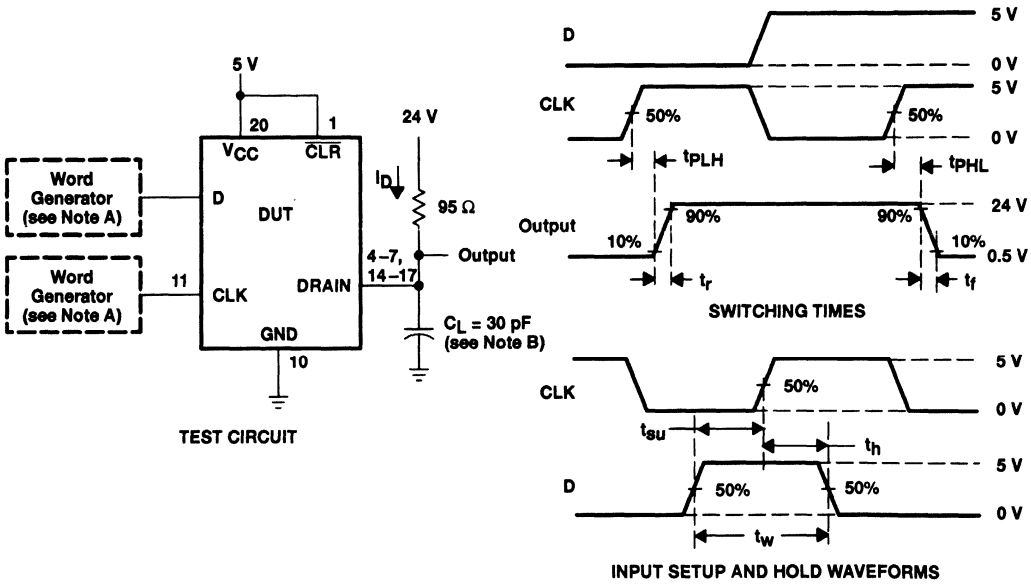
PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

Figure 1. Resistive Load Normal Operation



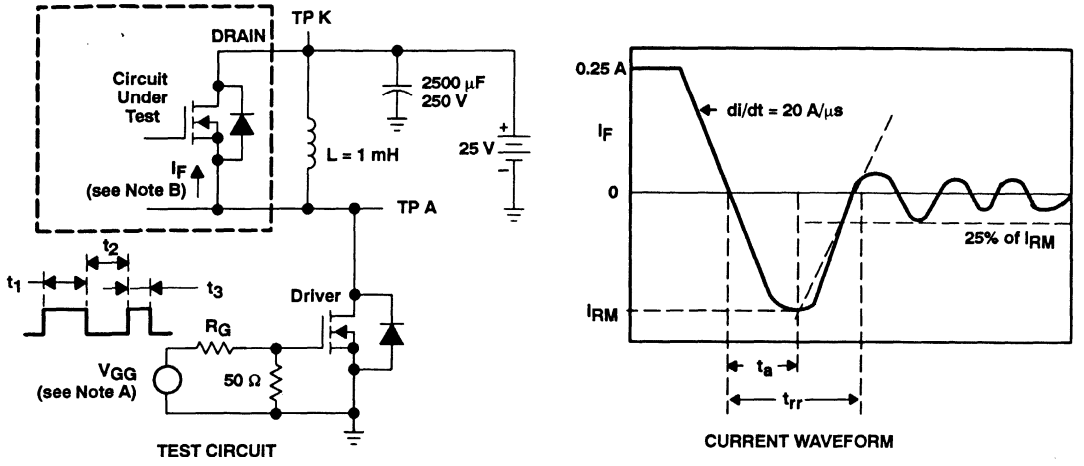
TEST CIRCUIT

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_W = 300$ ns, pulsed repetition rate (PRR) = 5 KHz, $Z_O = 50\ \Omega$.

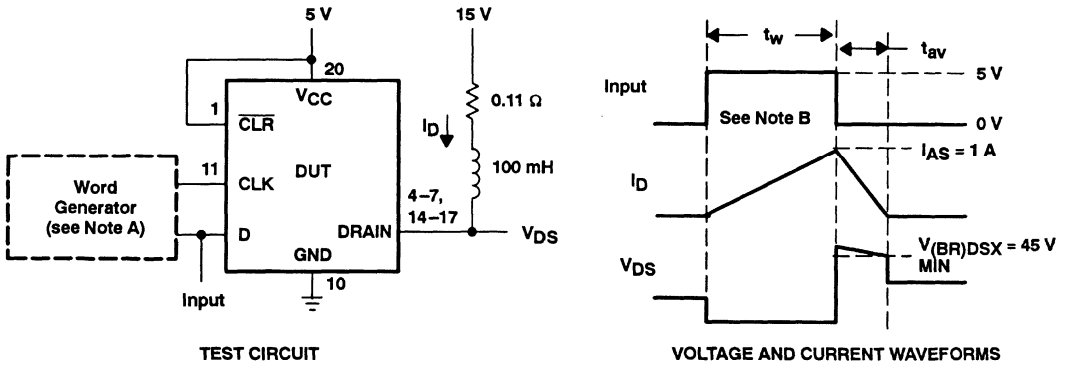
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 μs, t_2 = 7 μs, and t_3 = 3 μs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



NOTES: A. The word generator A has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, Z_O = 50 Ω.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

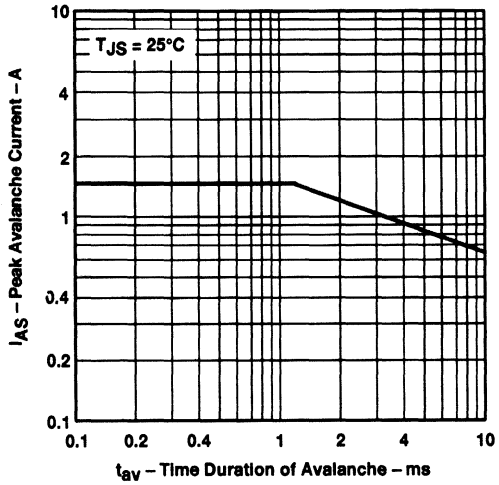


Figure 5

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

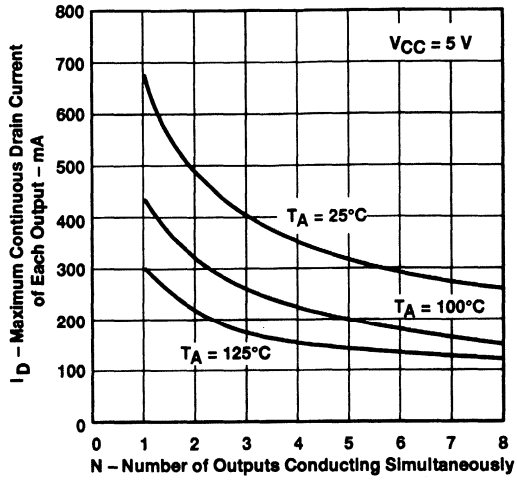


Figure 6

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

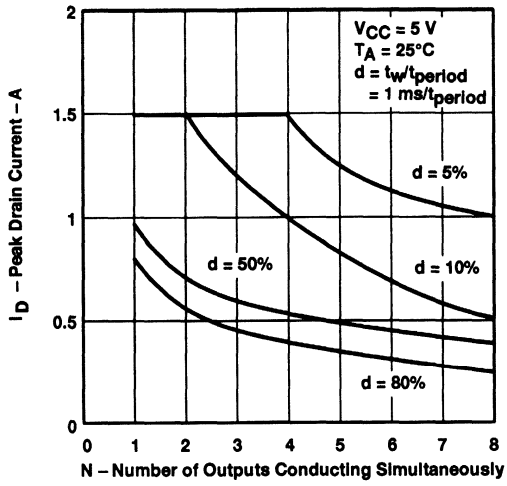


Figure 7

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

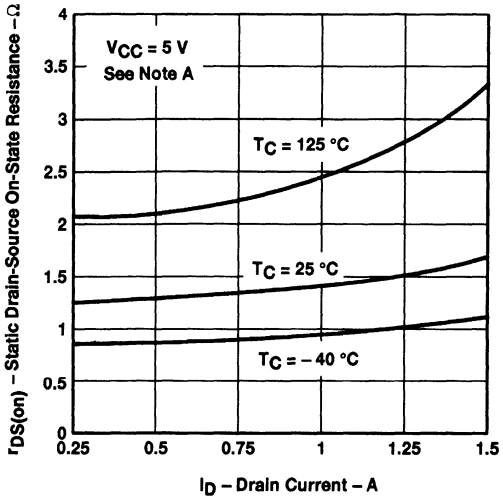


Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

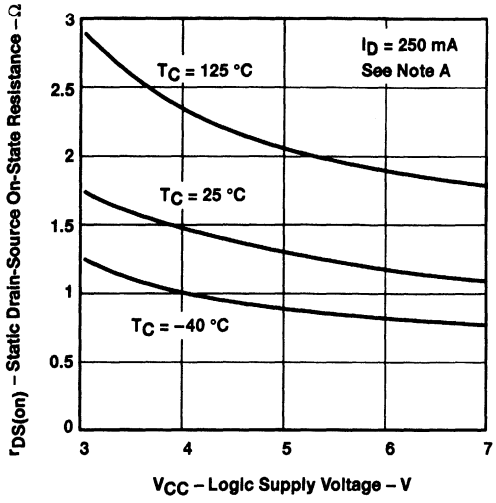


Figure 9

SWITCHING TIME vs FREE-AIR TEMPERATURE

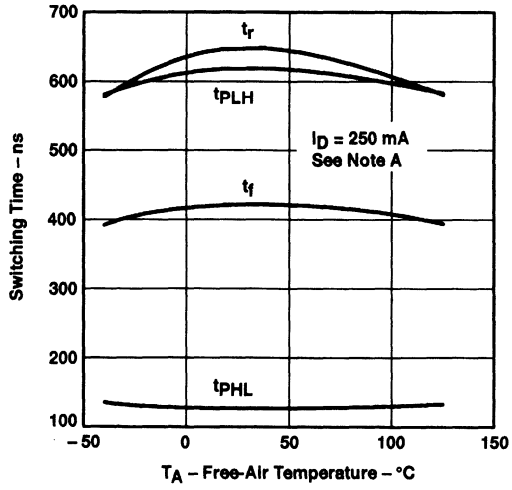


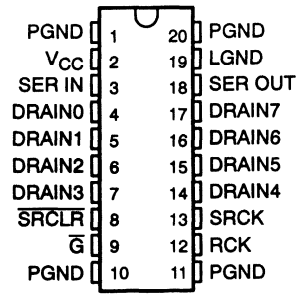
Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

SLIS010 – D4009, APRIL 1992 – REVISED FEBRUARY 1993

- **Low $r_{DS(on)}$ . . . 1.3 Ω Typical**
- **Avalanche Energy . . . 75 mJ**
- **Eight Power DMOS Transistor Outputs of 250-mA Continuous Current**
- **1.5-A Pulsed Current Per Output**
- **Output Clamp Voltage at 45 V**
- **Devices Are Cascadable**
- **Low Power Consumption**

DW OR N PACKAGE
(TOP VIEW)

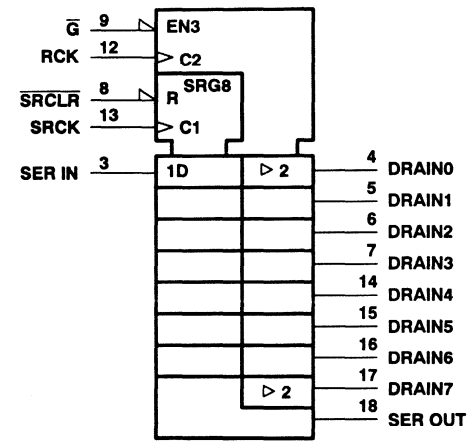


description

The TPIC6595 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear ($\overline{SRCLR}$) is high. When $\overline{SRCLR}$ is low, the input shift register is cleared. When output enable ($\overline{G}$) is held high, all data in the output buffers is held low and all drain outputs are off. When $\overline{G}$ is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

logic symbol†



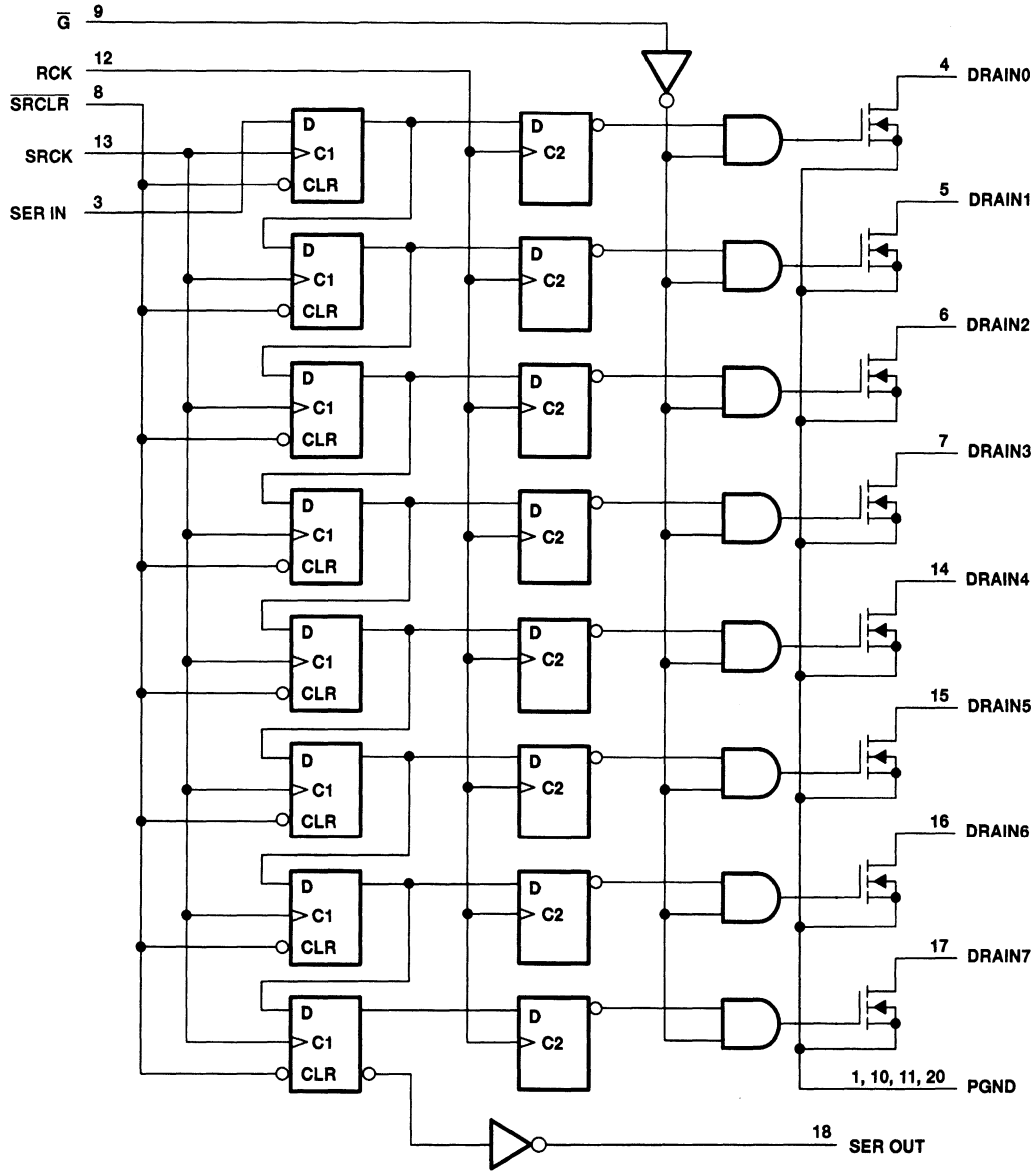
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Outputs are low-side, open-drain DMOS transistors with output ratings of 45 V and 250-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

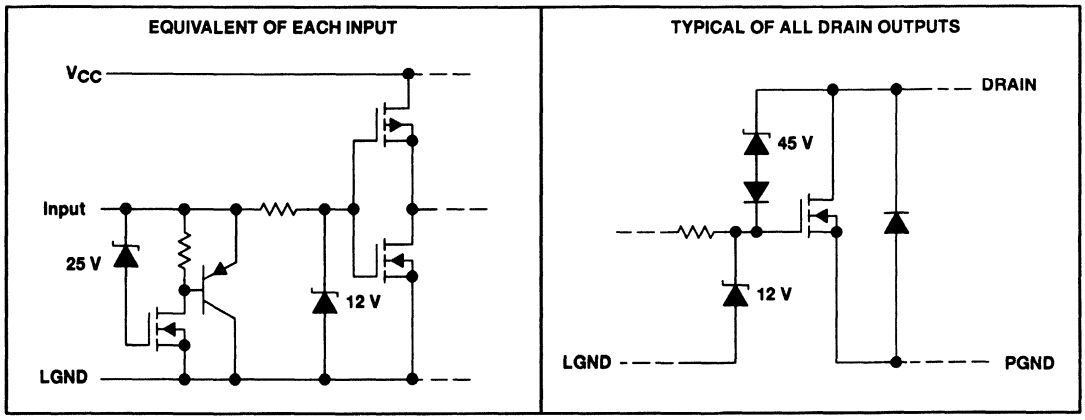
Separate power and logic level ground pins are provided to facilitate maximum system flexibility. Pins 1,10,11, and 20 are internally connected, and each pin must be externally connected to the power system ground in order to minimize parasitic inductance. A single-point connection between pin 19, logic ground (LGND) and pins 1, 10, 11, and 20, power ground (PGND) must be externally made in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	45 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	750 mA
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	250 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	2 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	75 mJ
Avalanche current, I_{AS} (see Note 4)	1 A
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2 %
4. DRAIN supply voltage = 15 V, starting junction temperature, (T_{JS}) = 25°C, L = 100 mH, I_{AS} = 1 A (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 125°C POWER RATING
DW	1125 mW	9.0 mW/°C	225 mW
N	1150 mW	9.2 mW/°C	230 mW

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}		V
Low-level input voltage, V_{IL}		0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C, V_{CC} = 5 V (see Notes 3 and 5)	−1.8	1.5	A
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	10		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	10		ns
Pulse duration, t_w (see Figure 2)	20		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250 mA, See Note 3			0.85	1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = −20 mA, V_{CC} = 4.5 V		4.4	4.49		V
		I_{OH} = −4 mA, V_{CC} = 4.5 V		4.1	4.3		
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20 mA, V_{CC} = 4.5 V			0.002	0.1	V
		I_{OH} = 4 mA, V_{CC} = 4.5 V			0.2	0.4	
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0				−1	µA
I_{CC}	Logic supply current	I_O = 0, All inputs low			15	100	µA
$I_{CC(FRQ)}$	Logic supply current frequency	f_{SRCK} = 5 MHz, I_O = 0, C_L = 30 pF, See Figures 1, 2, and 6			0.6	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, I_N = I_D, T_C = 85°C	See Notes 5, 6, and 7		250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V			0.05	1	µA
		V_{DS} = 40 V, T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250 mA, V_{CC} = 4.5 V	See Notes 5 and 6 and Figures 9 and 10		1.3	2	Ω
		I_D = 250 mA, T_C = 125°C, V_{CC} = 4.5 V			2	3.2	
		I_D = 500 mA, V_{CC} = 4.5 V			1.3	2	

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 250 mA, See Figures 1, 2, and 11		650		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			150		ns
t_r	Rise time, drain output			750		ns
t_f	Fall time, drain output			425		ns
t_a	Reverse-recovery-current rise time	I_F = 250 mA, di/dt = 20 A/µs, See Notes 5 and 6 and Figure 3		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
5. Technique should limit $T_J - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package	All 8 outputs with equal power		111	°C/W
		N package			108	

PARAMETER MEASUREMENT INFORMATION

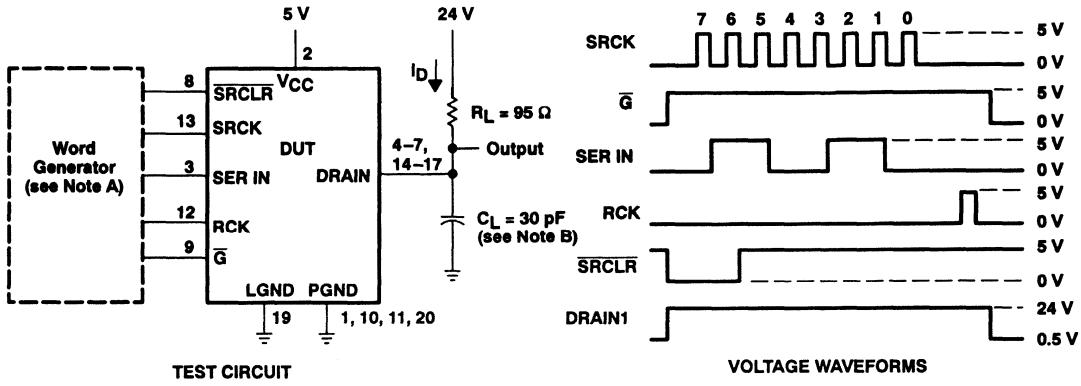


Figure 1. Resistive Load Operation

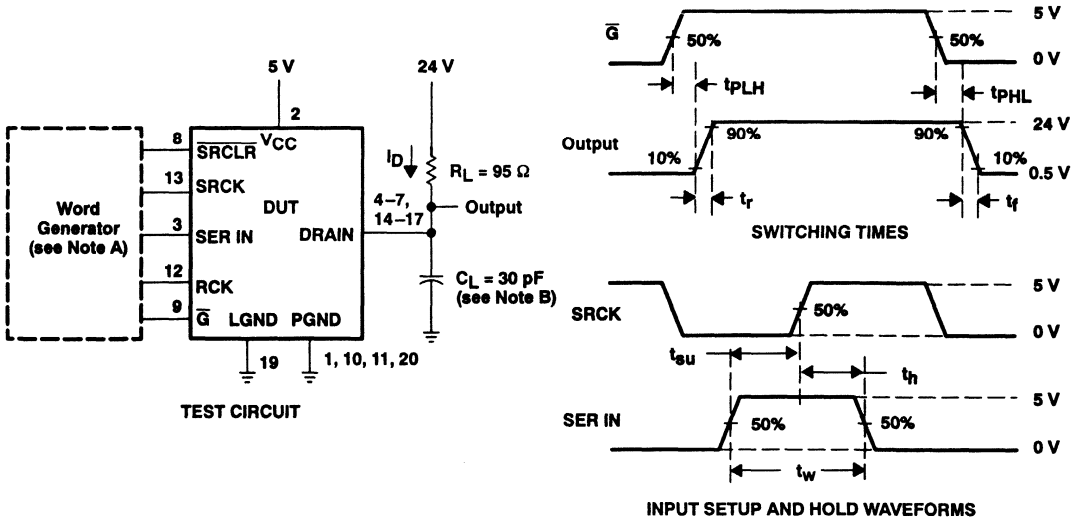
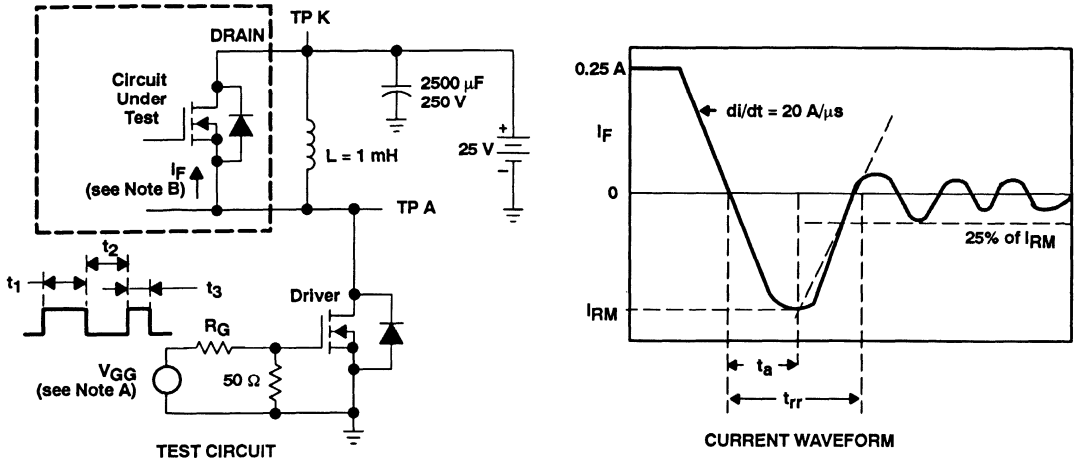


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

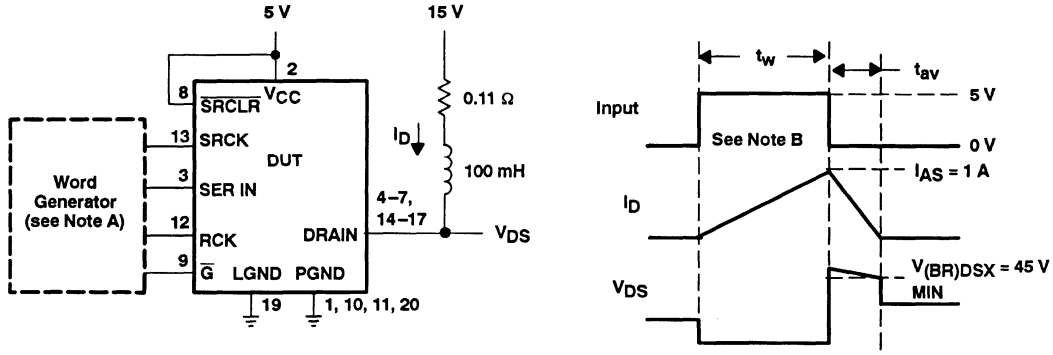
NOTES: A. Outputs DRAIN 1, 2, 5, and 6 low (PGND), all other DRAIN outputs are at 24 V. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.25 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, Z_O = 50 Ω.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1 A.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT
vs
TIME DURATION OF AVALANCHE

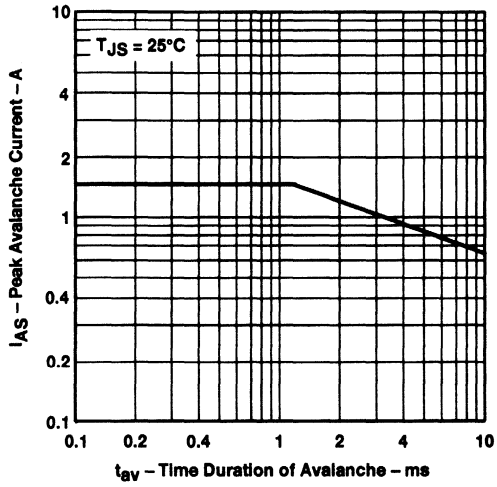


Figure 5

SUPPLY CURRENT
vs
FREQUENCY

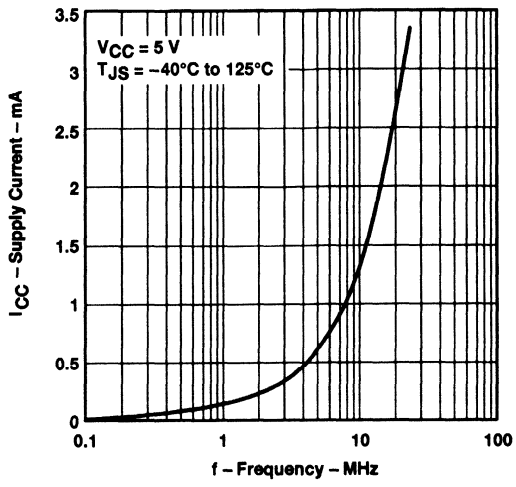


Figure 6

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

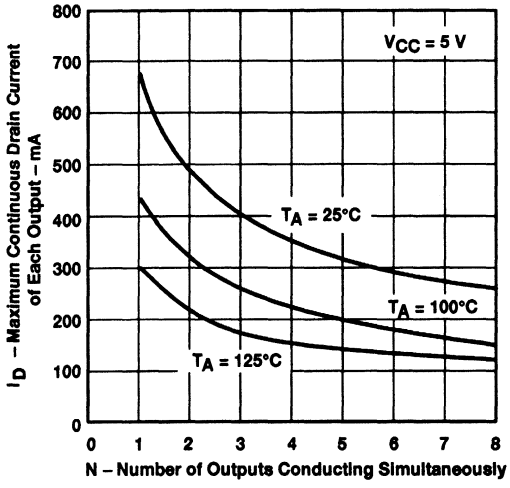


Figure 7

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

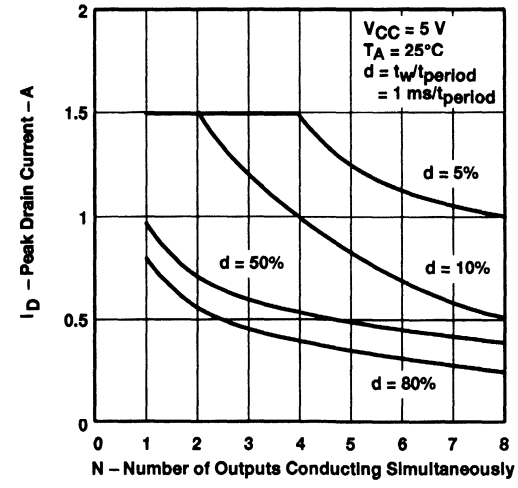


Figure 8

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

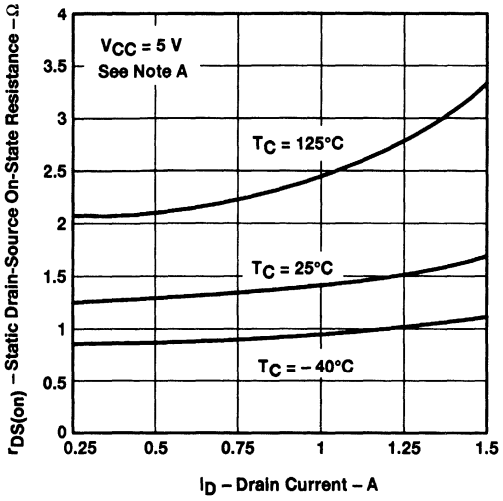


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

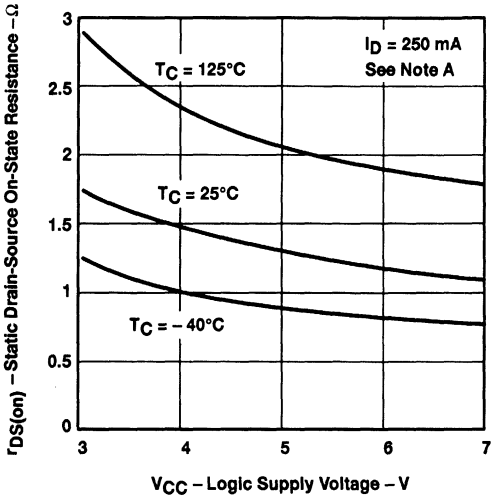


Figure 10

SWITCHING TIME vs FREE-AIR TEMPERATURE

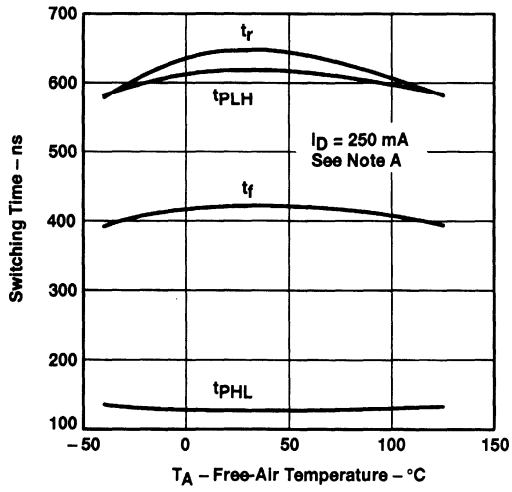


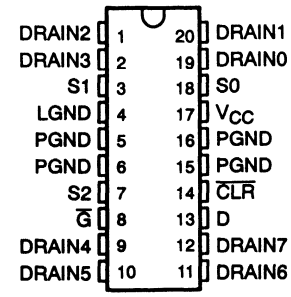
Figure 11

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

SLIS004 – D4074, APRIL 1993

- **Low $r_{DS(on)}$ . . . 1 Ω Typical**
- **Output Short-Circuit Protection**
- **Avalanche Energy . . . 75 mJ**
- **Eight 350-mA DMOS Outputs**
- **50-V Switching Capability**
- **Four Distinct Function Modes**
- **Low Power Consumption**

NE PACKAGE
(TOP VIEW)



description

This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multifunctional device capable of operating as eight addressable latches or an 8-line demultiplexer with active-low DMOS outputs. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

FUNCTION TABLE

INPUTS			OUTPUT OF ADDRESSED DRAIN	EACH OTHER DRAIN	FUNCTION
$\overline{CLR}$	$\overline{G}$	D			
H	L	H	L	Q_{io}	Addressable Latch
H	L	L	H	Q_{io}	
H	H	X	Q_{io}	Q_{io}	Memory
L	L	H	L	H	8-Line Demultiplexer
L	L	L	H	H	
L	H	X	H	H	Clear

LATCH SELECTION TABLE

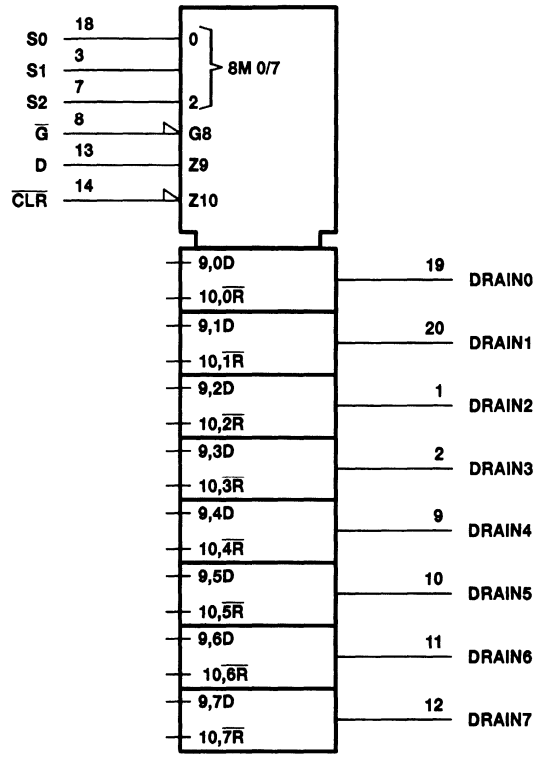
SELECT INPUTS			DRAIN ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

Four distinct modes of operation are selectable by controlling the clear ($\overline{CLR}$) and enable ($\overline{G}$) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable $\overline{G}$ should be held high (inactive) while the address lines are changing. In the 8-line demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are high. In the clear mode, all outputs are high and unaffected by the address and data inputs.

Separate power ground (PGND) and logic ground (LGND) pins are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

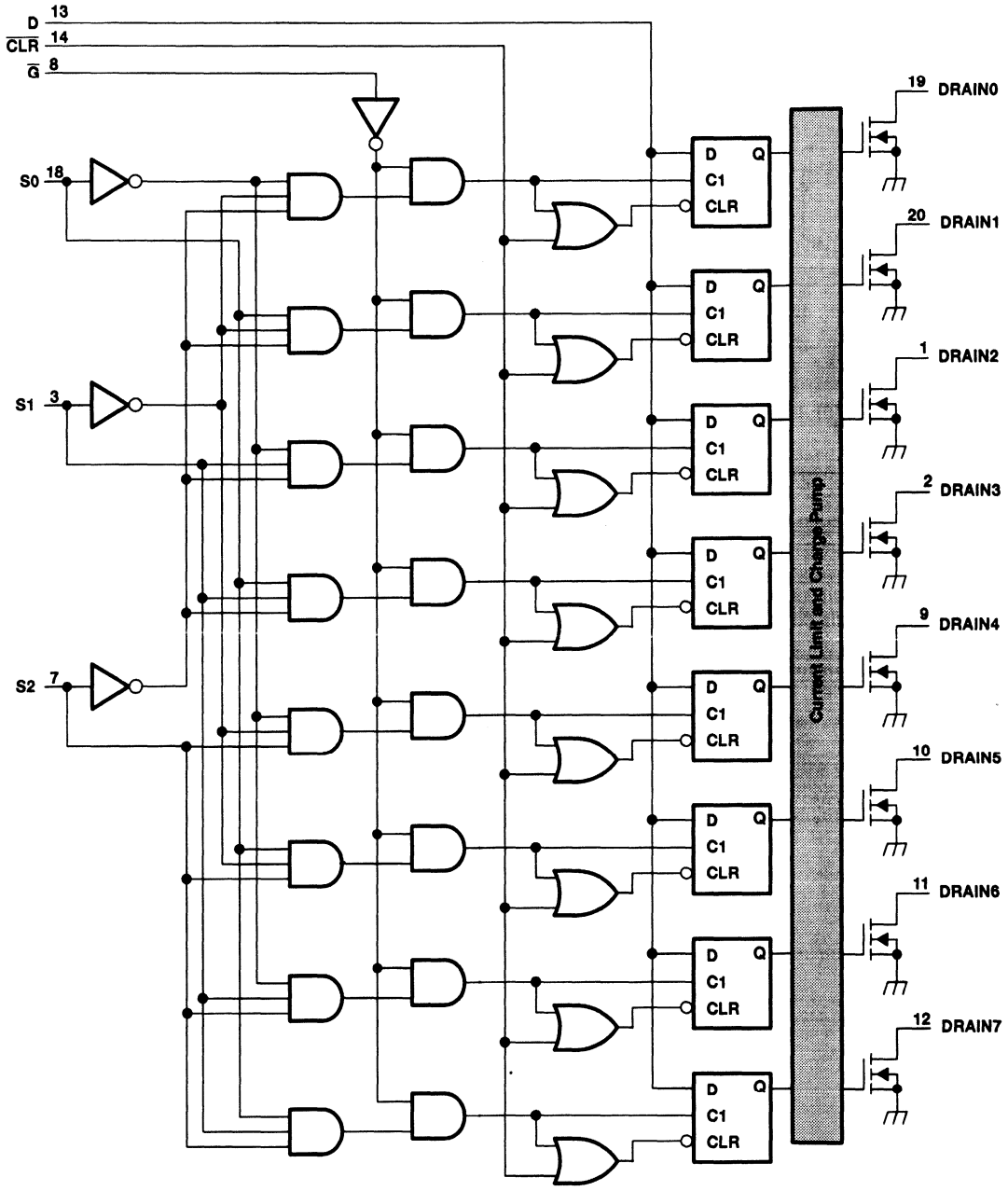
The TPIC6A259 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic symbol†

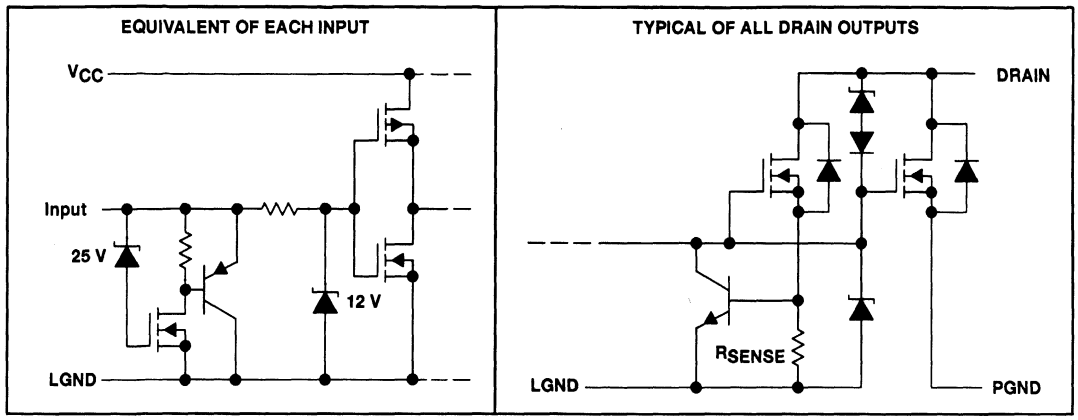


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current (see Note 3)	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	1.1 A
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	350 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	1.1 A
Single-pulse avalanche energy, E_{AS} (see Figure 6)	75 mJ
Avalanche current, I_{AS} (see Note 4)	600 mA
Continuous total dissipation at (or below) T_A = 25°C (see Note 5)	2.5 W
Continuous total dissipation at (or below) T_C = 100°C (see Note 5)	6 W
Operating case temperature range, T_C	−40°C to 125°C
Operating virtual-junction temperature range, T_J	−40°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2%
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 210 mH, I_{AS} = 600 mA (see Figure 6).
5. For operation above T_A = 25°C free-air temperature, derate linearly at the rate of 20 mW/°C. For operation above 100°C case temperature, derate linearly at the rate of 120 mW/°C. To avoid exceeding the design maximum junction temperature, this rating should not be exceeded.

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C (see Notes 3 and 6)	−1.8	0.6	A
Setup time, D high before $\overline{G}\uparrow$, t_{su} (see Figure 2)	10		ns
Hold time, D high before $\overline{G}\uparrow$, t_h (see Figure 2)	5		ns
Pulse duration, t_w (see Figure 2)	15		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics over recommended ranges of supply voltage and operating temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA			50			V
V_{SD}	Source-drain diode forward voltage	I_F = 350 mA,	See Note 3			0.8	1.1	V
I_{IH}	High-level input current	$V_I = V_{CC}$					1	μA
I_{IL}	Low-level input current	V_I = 0					−1	μA
I_{CC}	Logic supply current	I_O = 0,	$V_I = V_{CC}$ or 0			0.5	5	mA
I_{OK}	Output current at which chopping starts	T_C = 25°C,	See Note 6 and Figures 3 and 4		0.6	0.8	1.1	A
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, V_{CC} = 5 V,	$I_N = I_D$, See Notes 6, 7, and 8	T_C = 85°C,		350		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V,	T_C = 25°C			0.1	1	μA
		V_{DS} = 40 V,	T_C = 125°C			0.2	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 350 mA,	T_C = 25°C	See Notes 6 and 7 and Figures 9 and 10		1	1.5	Ω
		I_D = 350 mA,	T_C = 125°C			1.7	2.5	

† All typical values are at V_{CC} = 5 V, T_C = 25°C.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from D	C_L = 30 pF, I_D = 350 mA, See Figures 1, 2, and 11		30		ns
t_{PLH}	Propagation delay time, low-to-high-level output from D			125		ns
t_r	Rise time, drain output			60		ns
t_f	Fall time, drain output			30		ns
t_a	Reverse-recovery-current rise time	I_F = 350 mA, di/dt = 20 A/μs, See Notes 6 and 7 and Figure 5		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 3. Pulse duration ≤ 100 μs, duty cycle ≤ 2%
6. Technique should limit $T_J - T_C$ to 10°C maximum.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
8. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	All eight outputs with equal power		8.3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	All eight outputs with equal power		50	°C/W

PARAMETER MEASUREMENT INFORMATION

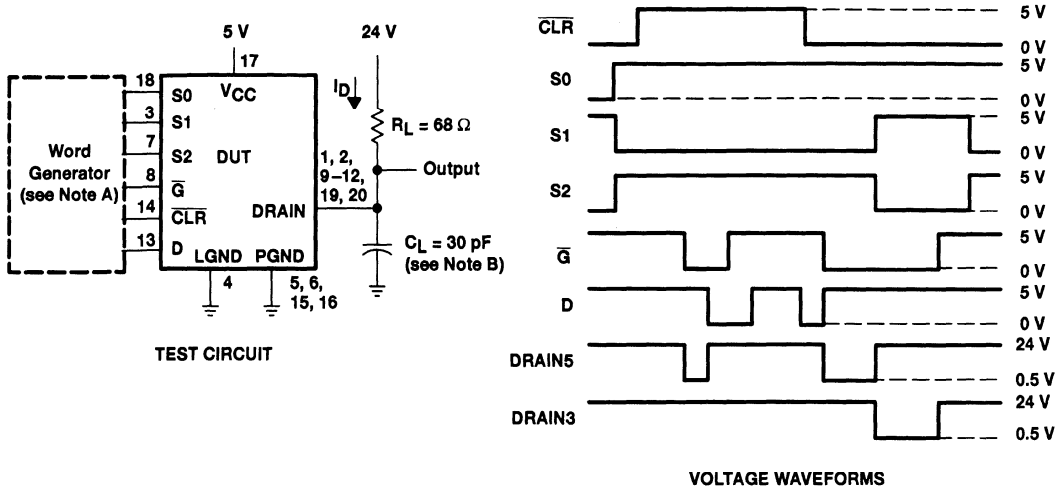


Figure 1. Typical Operation Mode

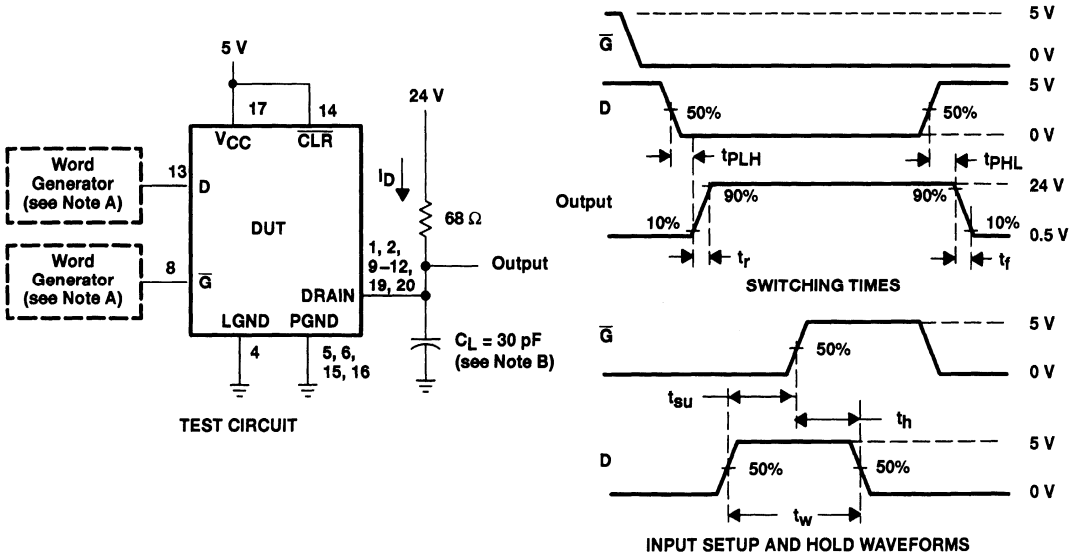
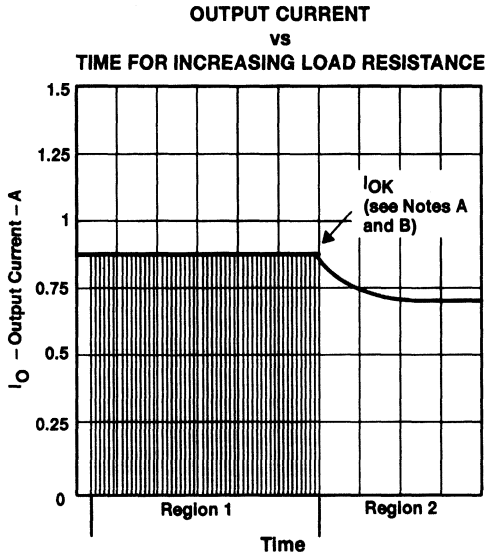
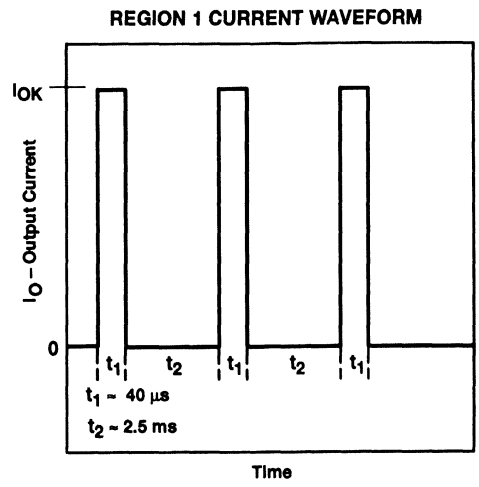


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION





First output current pulses after turn-on in chopping mode with resistive load.

NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.

B. Region 1 duty cycle is approximately 2%.

Figure 3. Chopping-Mode Characteristics

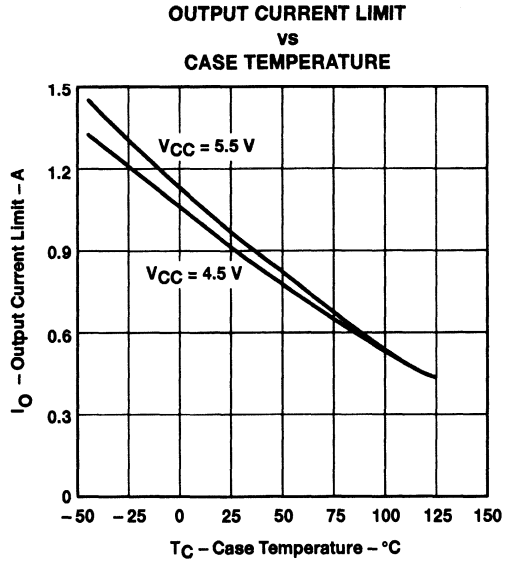
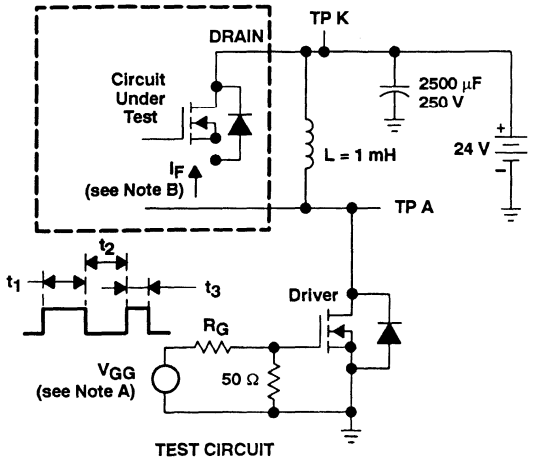
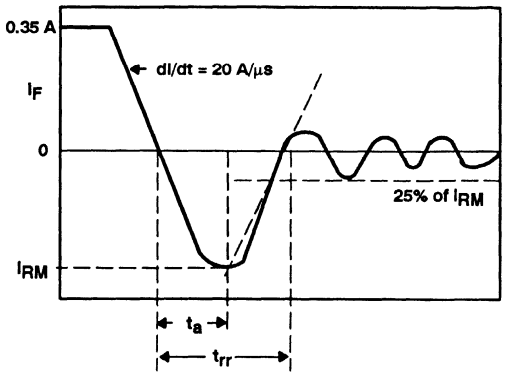


Figure 4

PARAMETER MEASUREMENT INFORMATION



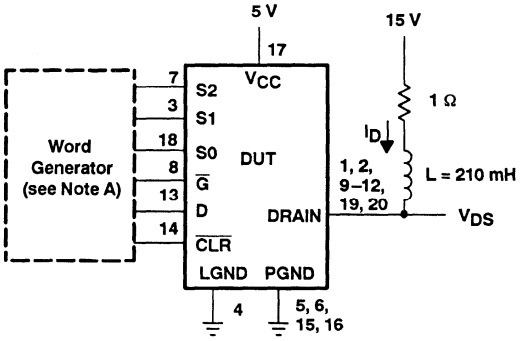
TEST CIRCUIT



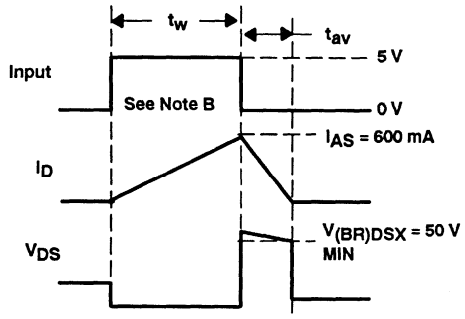
CURRENT WAVEFORM

NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/μs. A V_{GG} double-pulse train is used to set I_F = 0.35 A, where t_1 = 10 μs, t_2 = 7 μs, and t_3 = 3 μs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: C. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, Z_O = 50 Ω.
D. Input pulse duration, t_w, is increased until peak current I_{AS} = 600 mA.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ.

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

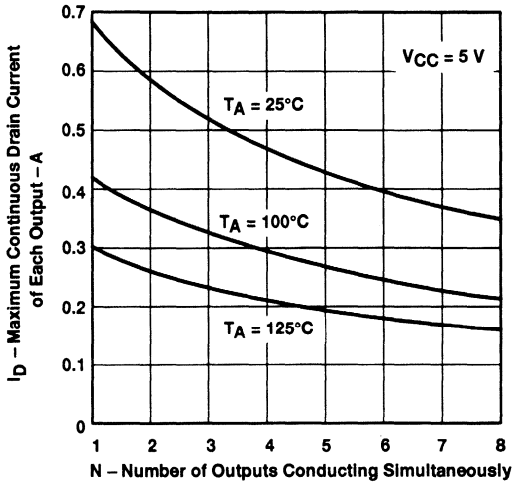


Figure 7

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

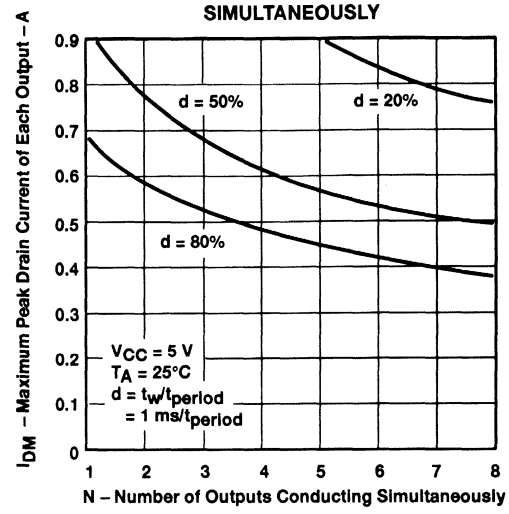


Figure 8

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT

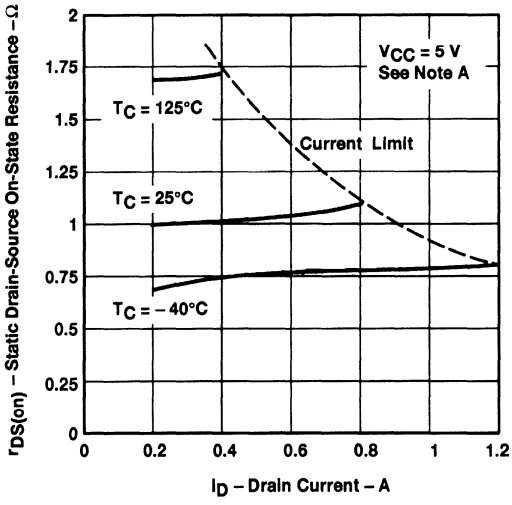


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

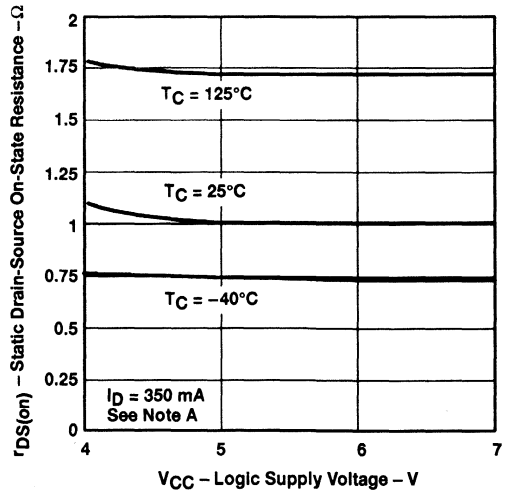
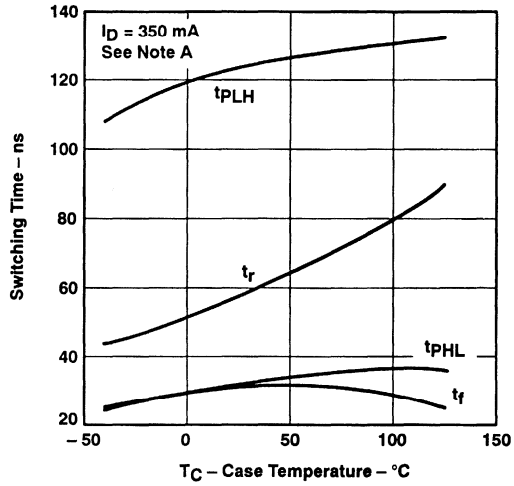


Figure 10

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

TYPICAL CHARACTERISTICS

SWITCHING TIME vs CASE TEMPERATURE

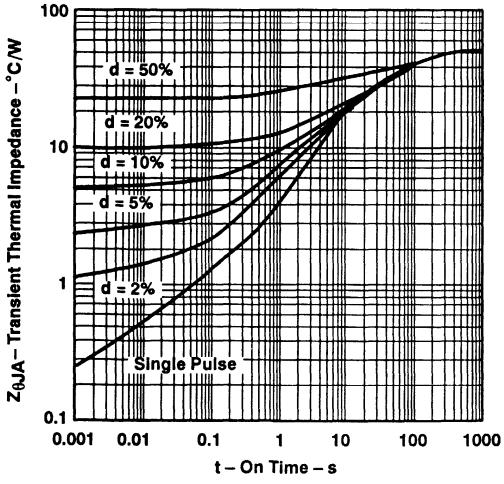


NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 11

THERMAL INFORMATION

TRANSIENT THERMAL IMPEDANCE vs ON TIME



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left|\frac{t_w}{t_c}\right| R_{\theta JA} + \left|1 - \frac{t_w}{t_c}\right| Z_{\theta(tw + tc)} + Z_{\theta(tw)} - Z_{\theta(tc)}$$

Where:

$Z_{\theta(t_w)}$ = the single-pulse thermal impedance for t = t_w seconds

$Z_{\theta(t_c)}$ = the single-pulse thermal impedance for t = t_c seconds

$Z_{\theta(t_w + t_c)}$ = the single-pulse thermal impedance for t = $t_w + t_c$ seconds

$d = t_w/t_c$

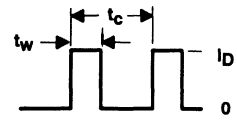
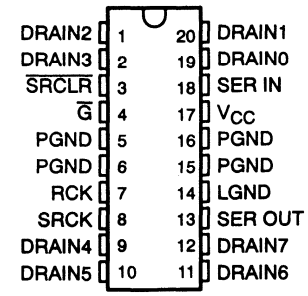


Figure 12

- Low $r_{DS(on)}$ . . . 1 Ω Typical
- Output Short-Circuit Protection
- Avalanche Energy . . . 75 mJ
- Eight 350-mA DMOS Outputs
- 50-V Switching Capability
- Devices Are Cascadable
- Low Power Consumption

NE PACKAGE
(TOP VIEW)

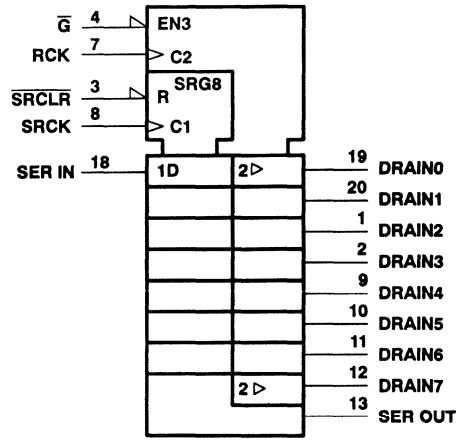


description

The TPIC6A595 is a monolithic, high-voltage, high-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads. Each open-drain DMOS transistor features an independent chopping current-limiting circuit to prevent damage in the case of a short circuit.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear (SRCLR) is high. When SRCLR is low, the input shift register is cleared. When output enable (G) is held high, all data in the output buffers is held low and all drain outputs are off. When G is held low, data from the storage register is transparent to the output buffers. The serial output (SER OUT) allows for cascading of the data from the shift register to additional devices.

logic symbol†



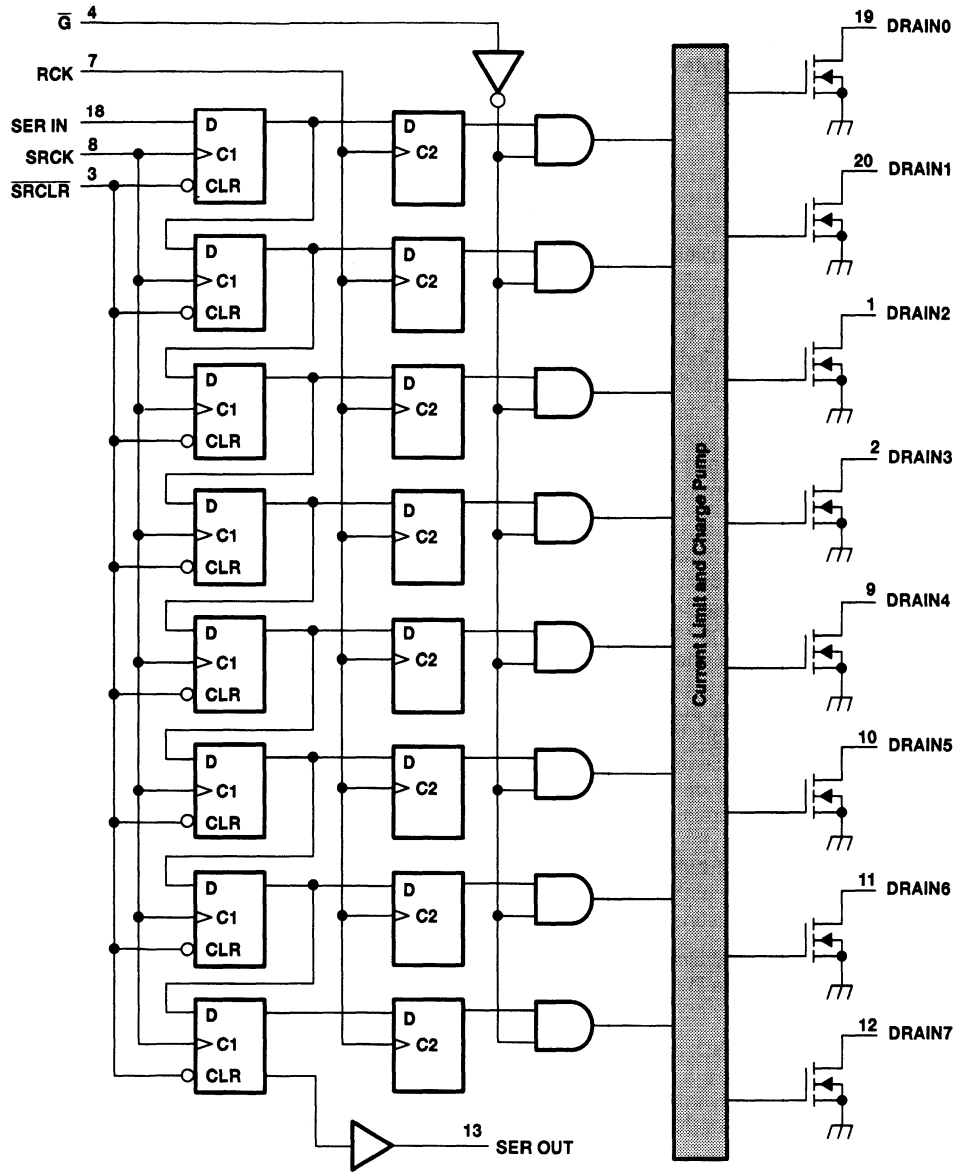
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50-V and 350-mA continuous sink current capability. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink current capability.

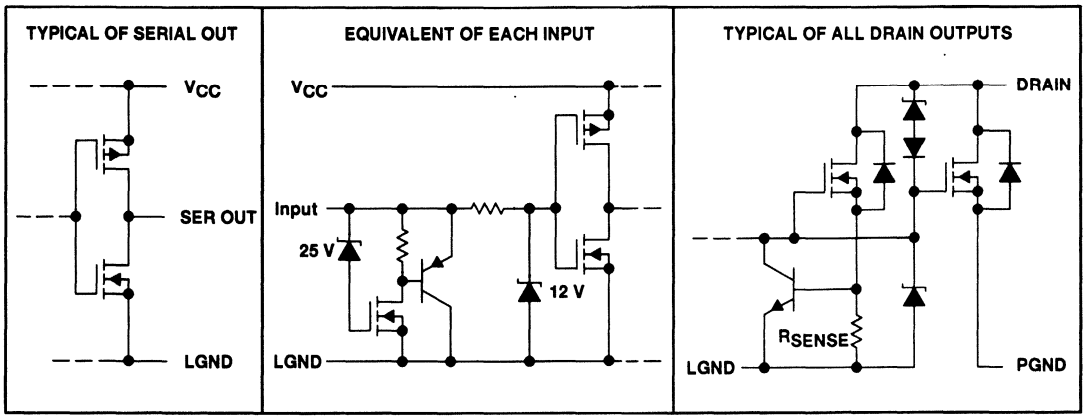
Separate power ground (PGND) and logic ground (LGND) terminals are provided to facilitate maximum system flexibility. All PGND terminals are internally connected, and each PGND terminal must be externally connected to the power system ground in order to minimize parasitic impedance. A single-point connection between LGND and PGND must be made externally in a manner that reduces crosstalk between the logic and load circuits.

The TPIC6A595 is characterized for operation over the operating case temperature range of −40°C to 125°C.

logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1)	7 V
Logic input voltage range, V_I	−0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2)	50 V
Continuous source-drain diode anode current	1 A
Pulsed source-drain diode anode current (see Note 3)	2 A
Pulsed drain current, each output, all outputs on, I_{Dn}, T_A = 25°C (see Note 3)	1.1 A
Continuous drain current, each output, all outputs on, I_{Dn}, T_A = 25°C	350 mA
Peak drain current single output, I_{DM}, T_A = 25°C (see Note 3)	1.1 A
Single-pulse avalanche energy, E_{AS} (see Figure 6)	75 mJ
Avalanche current, I_{AS} (see Note 4)	600 mA
Continuous total dissipation at (or below) T_A = 25°C (see Note 5)	2.5 W
Continuous total dissipation at (or below) T_C = 100°C (see Note 5)	6 W
Operating case temperature range, T_C	−40°C to 125°C
Operating virtual junction temperature range, T_J	−40°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to LGND and PGND.
2. Each power DMOS source is internally connected to PGND.
3. Pulse duration ≤ 100 µs, duty cycle ≤ 2 %
4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, L = 210 mH, I_{AS} = 600 mA (see Figure 6).
5. For operation above 25°C free-air temperature, derate linearly at the rate of 20 mW/°C. For operation above 100°C case temperature, derate linearly at the rate of 120 mW/°C. To avoid exceeding the design maximum junction temperature, this rating should not be exceeded.

recommended operating conditions over recommended operating temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	4.5	5.5	V
High-level input voltage, V_{IH}	0.85 V_{CC}	V_{CC}	V
Low-level input voltage, V_{IL}	0	0.15 V_{CC}	V
Pulsed drain output current, T_C = 25°C (see Notes 3 and 6)	−1.8	0.6	A
Setup time, SER IN high before SRCK↑, t_{su} (see Figure 2)	10		ns
Hold time, SER IN high after SRCK↑, t_h (see Figure 2)	10		ns
Pulse duration, t_w (see Figure 2)	20		ns
Operating case temperature, T_C	−40	125	°C

electrical characteristics over recommended ranges of supply voltage and operating temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA			50			V
V_{SD}	Source-drain diode forward voltage	I_F = 350 mA,	See Note 3			0.8	1.1	V
V_{OH}	High-level output voltage, SER OUT	I_{OH} = −20 μA			V_{CC}−0.1	V_{CC}		V
		I_{OH} = −4 mA			V_{CC}−0.5	V_{CC}−0.2		
V_{OL}	Low-level output voltage, SER OUT	I_{OL} = 20 μA				0	0.1	V
		I_{OL} = 4 mA				0.2	0.5	
I_{IH}	High-level input current	$V_I = V_{CC}$					1	μA
I_{IL}	Low-level input current	V_I = 0					−1	μA
I_{OK}	Output clamp current	T_C = 25°C, See Note 6 and Figures 3 and 4			0.6	0.8	1.1	A
I_{CC}	Logic supply current	I_O = 0,	$V_I = V_{CC}$ or 0			0.5	5	mA
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, $V_I = V_{CC}$ or 0,	I_O = 0, V_{CC} = 5 V,	C_L = 30 pF, See Figure 7		1.3		mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, V_{CC} = 5 V,	$I_N = I_D$, See Notes 6, 7, and 8	T_C = 85°C,		350		mA
I_{DSX}	Off-state drain current	V_{DS} = 40 V,	T_C = 25°C			0.1	1	μA
		V_{DS} = 40 V,	T_C = 125°C			0.2	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 350 mA,	T_C = 25°C	See Notes 6 and 7 and Figures 10 and 11		1	1.5	Ω
		I_D = 350 mA,	T_C = 125°C			1.7	2.5	

† All typical values are at V_{CC} = 5 V, T_C = 25°C

NOTES: 3. Pulse duration ≤ 100 μs, duty cycle ≤ 2%

6. Technique should limit $T_J - T_C$ to 10°C maximum.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
8. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at T_C = 85°C.

switching characteristics, V_{CC} = 5 V, T_C = 25°C

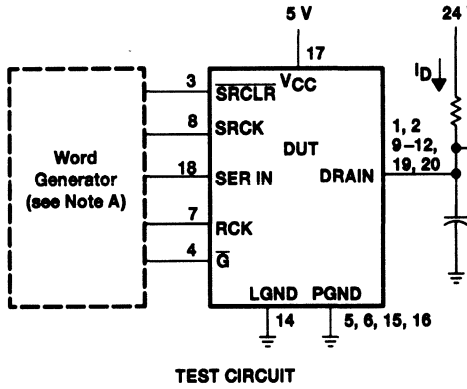
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$	C_L = 30 pF, I_D = 350 mA, See Figures 1, 2, and 12		30		ns
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$			125		ns
t_r	Rise time, drain output			60		ns
t_f	Fall time, drain output			30		ns
t_a	Reverse-recovery-current rise time	I_F = 350 mA, di/dt = 20 A/µs, See Notes 6 and 7 and Figure 5		100		ns
t_{rr}	Reverse-recovery time			300		

NOTES: 6. Technique should limit $T_J - T_C$ to 10°C maximum.
7. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

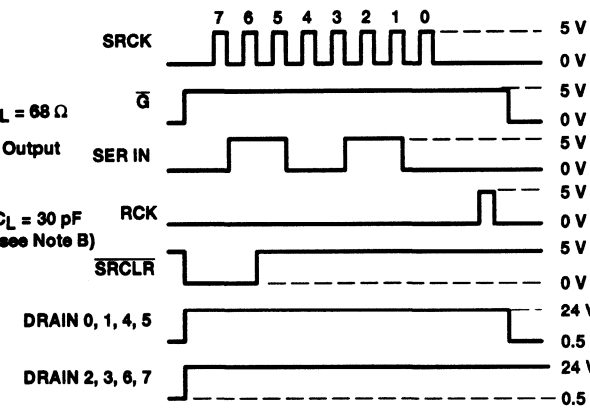
thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case	All eight outputs with equal power		8.3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	All eight outputs with equal power		50	°C/W

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, t_w = 300 ns, pulsed repetition rate (PRR) = 5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Resistive Load Operation

PARAMETER MEASUREMENT INFORMATION

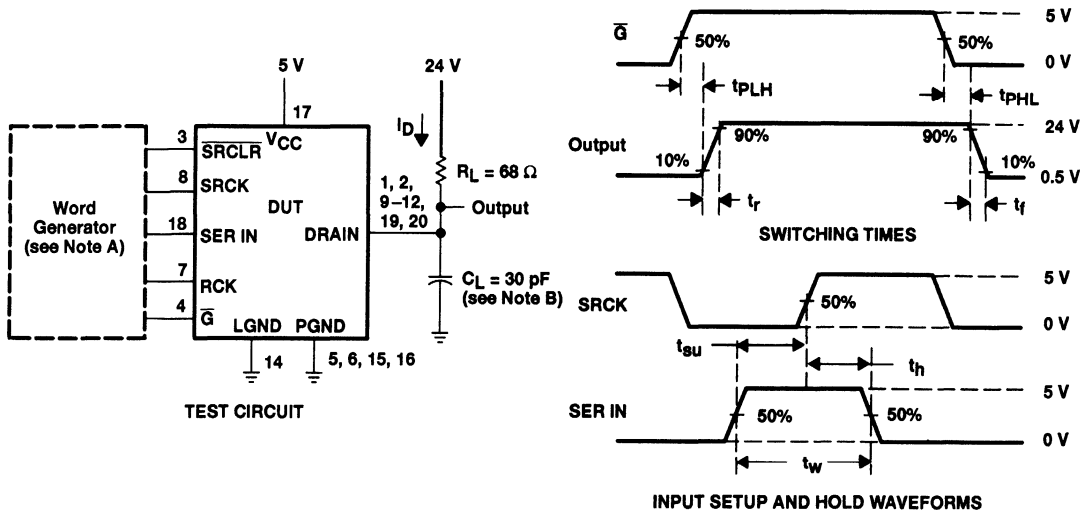
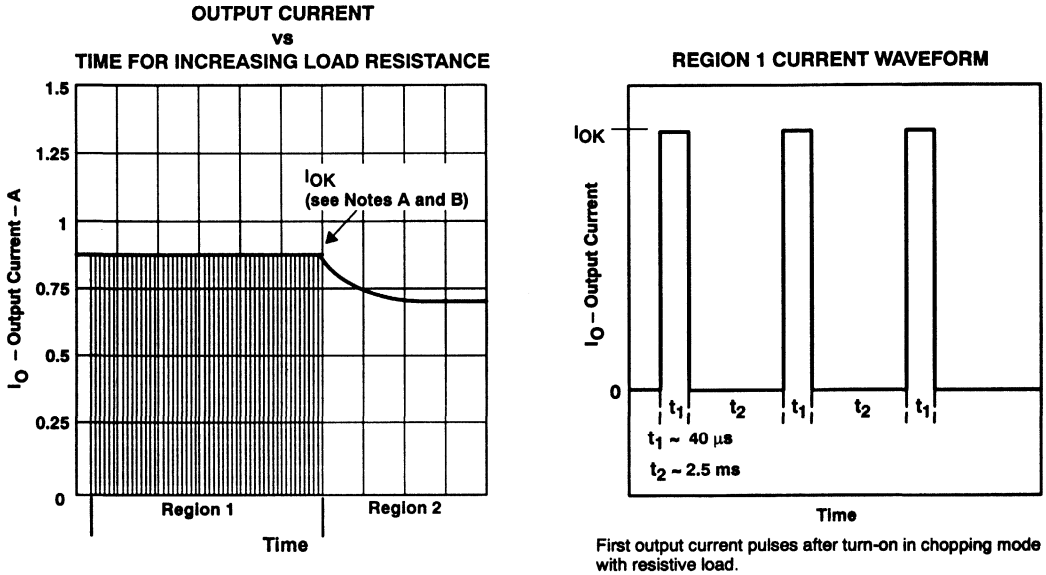


Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50\ \Omega$

B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



First output current pulses after turn-on in chopping mode with resistive load.

NOTES: A. Figure 3 illustrates the output current characteristics of the device energizing a load having initially low, increasing resistance, e.g., an incandescent lamp. In region 1, chopping occurs and the peak current is limited to I_{OK}. In region 2, output current is continuous. The same characteristics occur in reverse order when the device energizes a load having an initially high, decreasing resistance.
B. Region 1 duty cycle is approximately 2%.

Figure 3. Chopping-Mode Characteristics

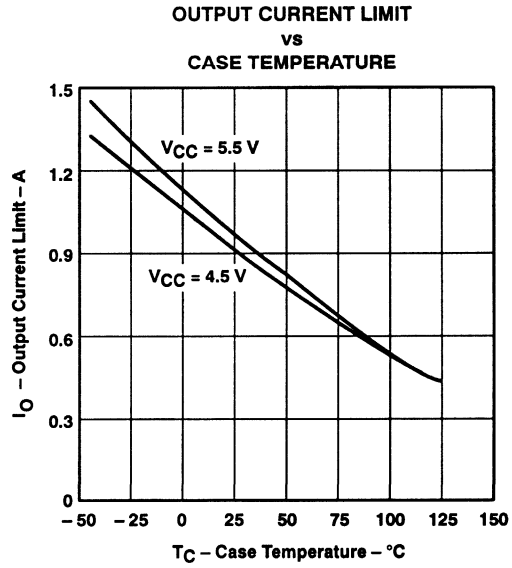
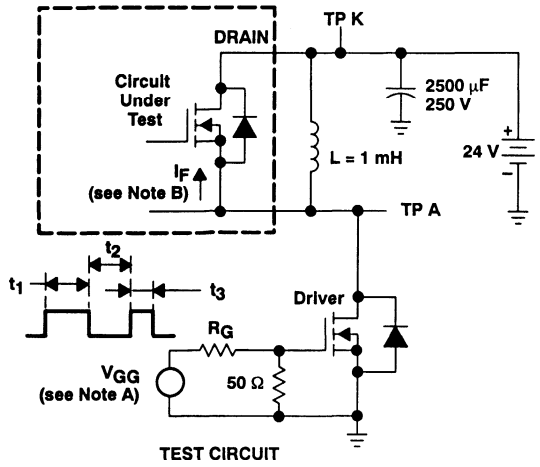
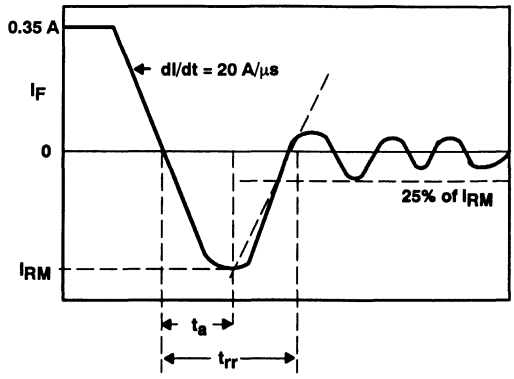


Figure 4

PARAMETER MEASUREMENT INFORMATION



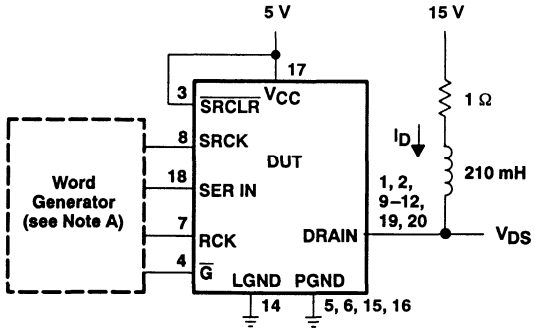
TEST CIRCUIT



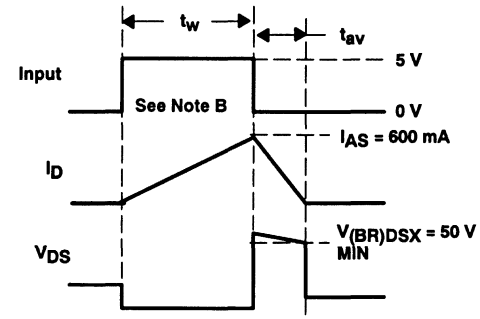
CURRENT WAVEFORM

NOTES: A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20 A/µs. A V_{GG} double-pulse train is used to set I_F = 0.35 A, where t_1 = 10 µs, t_2 = 7 µs, and t_3 = 3 µs.
B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

Figure 5. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The word generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, Z_O = 50 Ω.
B. Input pulse duration, t_w, is increased until peak current I_{AS} = 600 mA.
Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75 mJ.

Figure 6. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

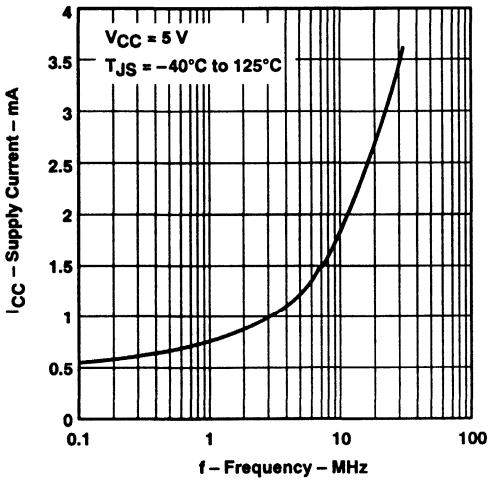


Figure 7

MAXIMUM CONTINUOUS DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

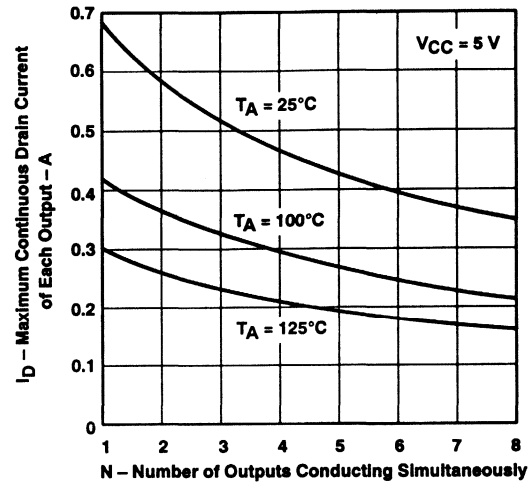


Figure 8

MAXIMUM PEAK DRAIN CURRENT OF EACH OUTPUT vs NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY

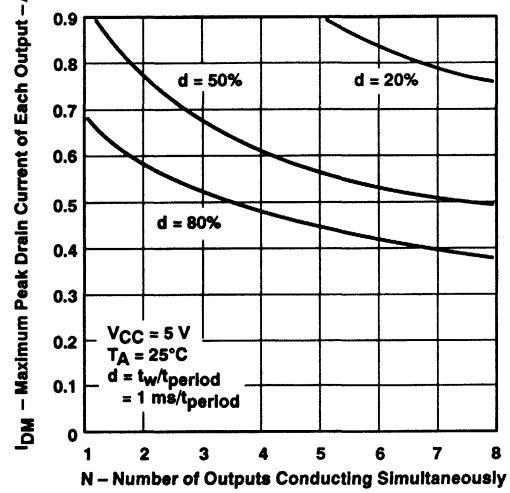
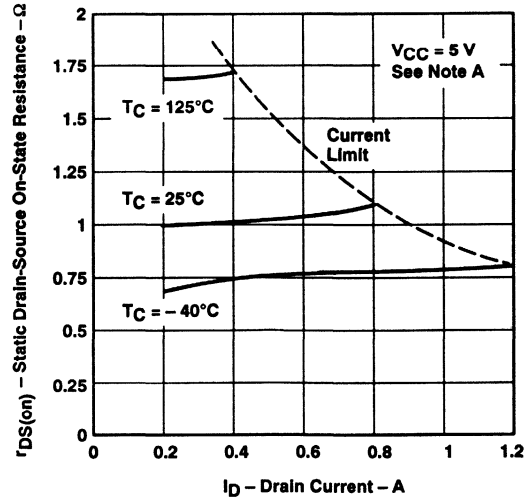


Figure 9

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs DRAIN CURRENT



NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 10

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs LOGIC SUPPLY VOLTAGE

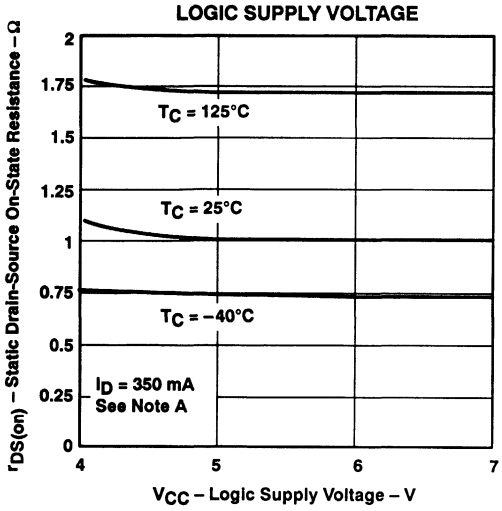


Figure 11

SWITCHING TIME vs CASE TEMPERATURE

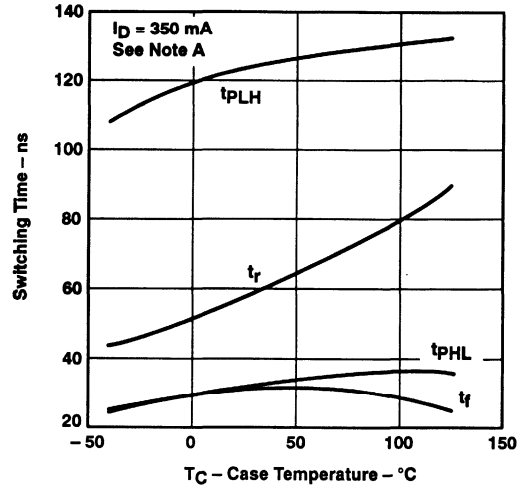
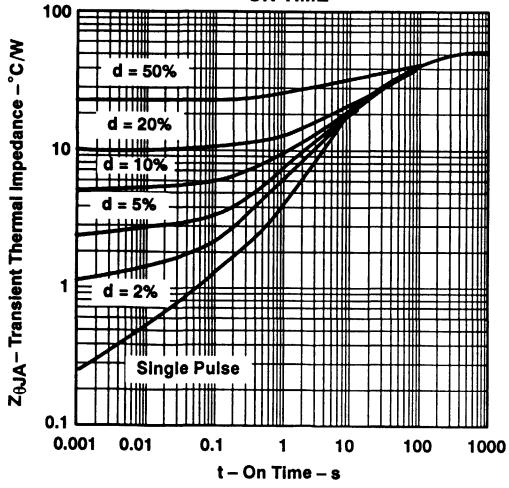


Figure 12

NOTE A: Technique should limit $T_J - T_C$ to 10°C maximum.

THERMAL INFORMATION

TRANSIENT THERMAL IMPEDANCE vs ON TIME



The single-pulse curve represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left|\frac{t_w}{t_c}\right| R_{\theta JA} + \left|1 - \frac{t_w}{t_c}\right| Z_{\theta(t_w + t_c)} + Z_{\theta(t_w)} - Z_{\theta(t_c)}$$

Where:

$Z_{\theta(t_w)}$ = the single-pulse thermal impedance for $t = t_w$ seconds

$Z_{\theta(t_c)}$ = the single-pulse thermal impedance for $t = t_c$ seconds

$Z_{\theta(t_w + t_c)}$ = the single-pulse thermal impedance for $t = t_w + t_c$ seconds

$d = t_w/t_c$

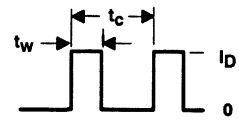


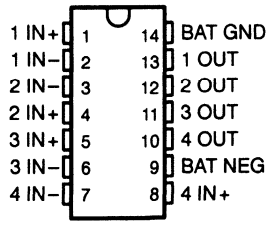
Figure 13

3 Peripheral Drivers/Actuators

SLRS014B – D2758, MARCH 1986 – REVISED APRIL 1993

- **Designed for –52-V Battery Operation**
- **50-mA Output Current Capability**
- **Input Compatible With TTL and CMOS**
- **High Common-Mode Input Voltage Range**
- **Very Low Input Current**
- **Fail-Safe Disconnect Feature**
- **Built-In Output Clamp Diode**
- **Direct Replacement for National DS3680 and Fairchild μA3680**

D OR N PACKAGE
(TOP VIEW)

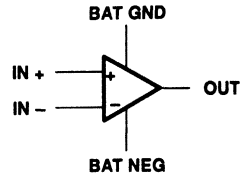


description

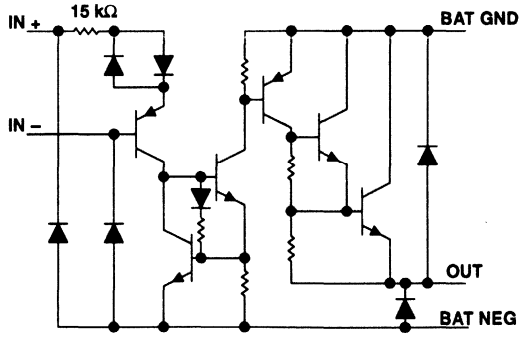
The DS3680I telephone relay driver is a monolithic integrated circuit designed to interface –48-V relay systems to TTL or other systems in telephone applications. It is capable of sourcing up to 50 mA from standard –52-V battery power. To reduce the effects of noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a common-mode input range of ±20 V referenced to battery ground. The common-mode input voltages for the four drivers can be different, so a wide range of input elements can be accommodated. The high-impedance inputs are compatible with positive TTL and CMOS levels or negative logic levels. A clamp network is included in the driver outputs to limit high-voltage transients generated by the relay coil during switching. The complementary inputs ensure that the driver output is off as a fail-safe condition when either output is open.

The DS3680I is characterized for operation from –25°C to 85°C.

symbol (each driver)



schematic diagram (each driver)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range at BAT NEG, V_{BAT-} (see Note 1) ..... −70 V to 0.5 V
Input voltage range with respect to BAT GND ..... −70 V to 20 V
Input voltage range with respect to BAT NEG ..... −0.5 V to 70 V
Differential input voltage, V_{ID} (see Note 2) ..... ±20 V
Output current: Resistive load ..... −100 mA
Inductive load ..... −50 mA
Inductive output load ..... 5 H
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds ..... 260°C

NOTES: 1. All voltages are with respect to BAT GND, unless otherwise specified.
2. Differential input voltages are at the noninverting input terminal IN+ with respect to the inverting input terminal IN–.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{BAT-}	−10	−60	V
Input voltage, either input	−20†	20	V
High-level differential input voltage, V_{IDH}	2	20	V
Low-level differential input voltage, V_{IDL}	−20†	0.8	V
Operating free-air temperature, T_A	−25	85	°C

† The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for input voltage levels.

electrical characteristics over recommended operating free-air temperature range, V_{BAT-} = −52 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_{IH}	High-level input current (into IN+)	V_{ID} = 2 V			40	100	µA
		V_{ID} = 7 V			375	1000	
I_{IL}	Low-level input current (into IN+)	V_{ID} = 0.4 V			0.01	5	µA
		V_{ID} = −7 V			−1	−100	
$V_{O(on)}$	On-stage output voltage	I_O = 50 mA	V_{ID} = 2 V		−1.6	−2.1	V
$I_{O(off)}$	Off-stage output current	$V_O = V_{BAT-}$	V_{ID} = 0.8 V		−2	−100	µA
			Inputs open		−2	−100	
I_R	Clamp diode reverse current	V_O = 0			2	100	µA
V_{OK}	Output clamp voltage	I_O = 50 mA			0.9	1.2	V
		I_O = −50 mA,	V_{BAT-} = 0		−0.9	−1.2	
$I_{BAT(on)}$	On-state battery current	All drivers on			−2	−4.4	mA
$I_{BAT(off)}$	Off-state battery current	All drivers off			−1	−100	µA

‡ All typical values are at T_A = 25°C.

switching characteristics V_{BAT-} = −52 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	V_{ID} = 3-V pulse, R_L = 1 kΩ, L = 1 H, See Figure 2		1	10	μs
t_{off}	Turn-off time			1	10	μs

PARAMETER MEASUREMENT INFORMATION

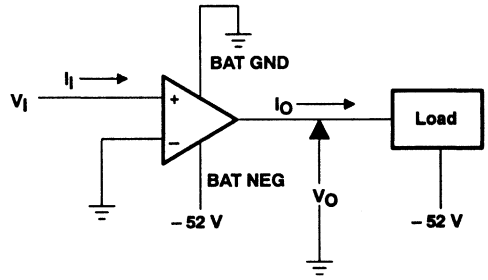


Figure 1. Generalized Test Circuit, Each Driver

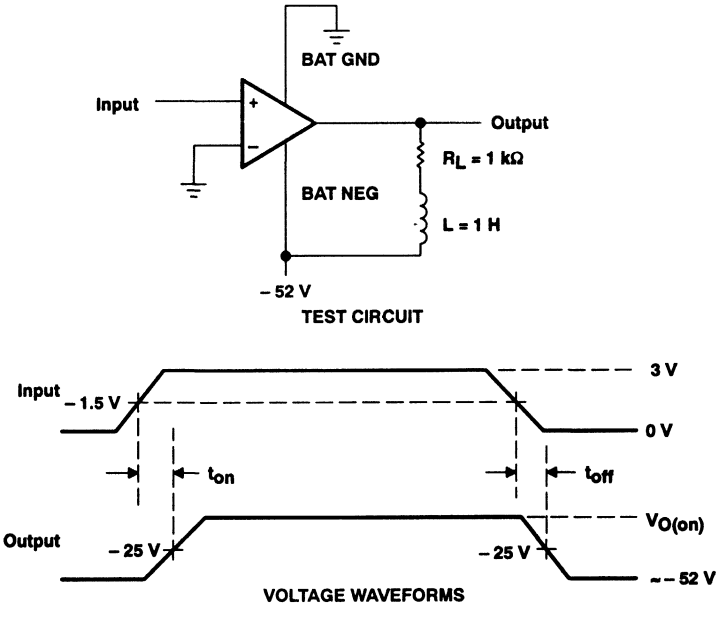


Figure 2. Test Circuit and Voltage Waveforms, Each Driver

APPLICATION INFORMATION

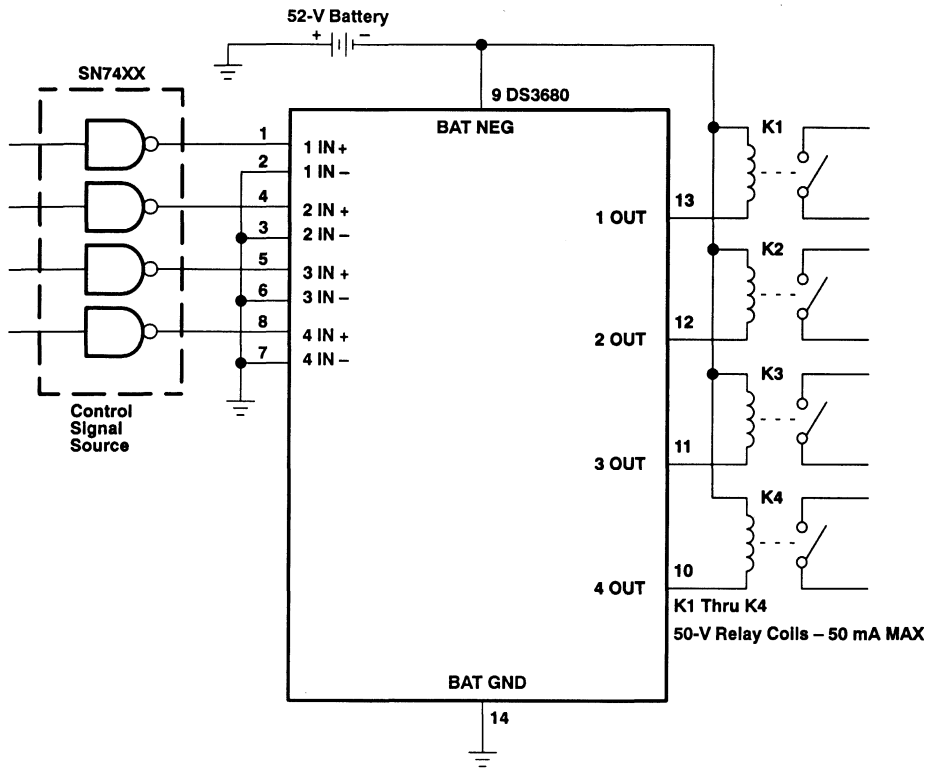
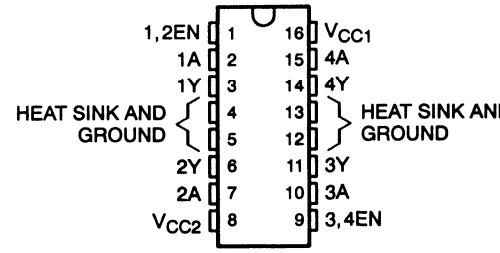


Figure 3. Relay Driver

SLRS005 – D2942, SEPTEMBER 1986 – REVISED MAY 1990

- **1-A Output Current Capability Per Driver**
- **Pulsed Current 2-A Driver**
- **Wide Supply Voltage Range: 4.5 V to 36 V**
- **Separate Input-Logic Supply**
- **NE Package Designed for Heat Sinking**
- **Thermal Shutdown**
- **Internal ESD Protection**
- **High-Noise-Immunity Inputs**
- **Functional Replacement for SGS L293**

NE PACKAGE
(TOP VIEW)



description

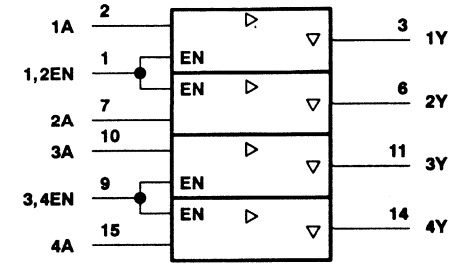
The L293 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to 1 A at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are TTL compatible. Each output is a complete totem-pole drive circuit with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

External high-speed output clamp diodes should be used for inductive transient suppression. A V_{CC1} terminal, separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation.

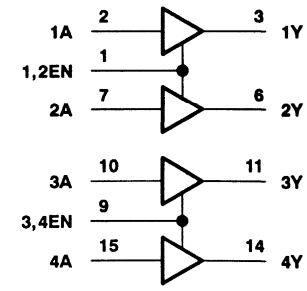
The L293 is designed for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagram

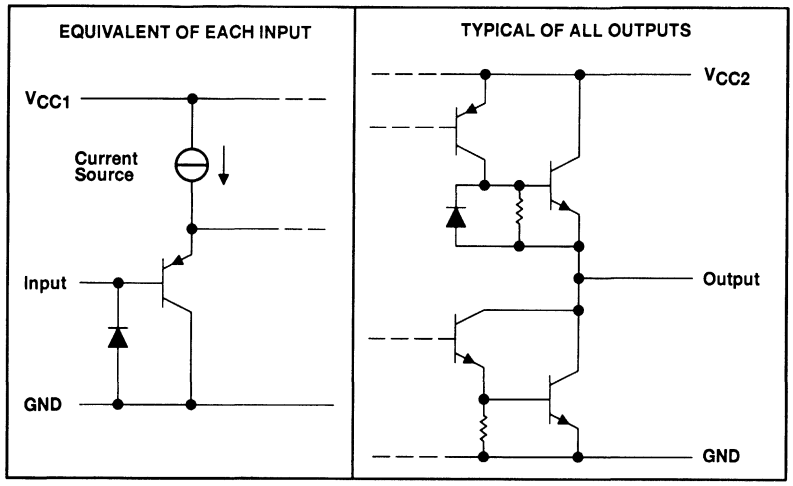


FUNCTION TABLE
(each driver)

INPUTS‡		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level, L = low-level,
X = irrelevant, Z = high-impedance (off)
‡ In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 36 V
Output supply voltage, V_{CC2} ..... 36 V
Input voltage, V_I ..... 7 V
Output voltage range ..... −3 V to V_{CC2} + 3 V
Peak output current (nonrepetitive, t ≤ 5 ms) ..... ±2 A
Continuous output current, I_O ..... ±1 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Notes 2 and 3) ..... 2075 mW
Continuous total dissipation at 80°C case temperature (see Note 3) ..... 5000 mW
Operating case or virtual junction temperature range ..... −40°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
3. For operation above 25°C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}			36	V
High-level input voltage, V_{IH}	$V_{CC1} \leq 7$ V	2.3		V
	$V_{CC1} \geq 7$ V	2.3	7	
Low-level output voltage, V_{IL}		−0.3†	1.5	V
Operating free-air temperature, T_A		0	70	°C

† The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

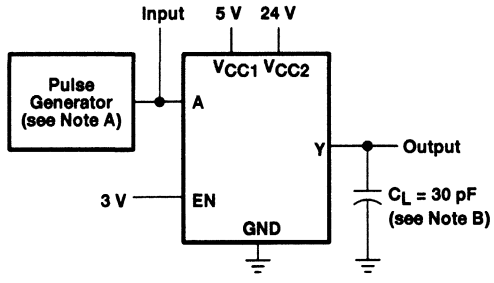
electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1 A		V_{CC2}−1.8	V_{CC2}−1.4		V
V_{OL}	Low-level output voltage		I_{OL} = 1 A			1.2	1.8	V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	μA
		EN				0.2	±10	
I_{IL}	Low-level input current	A	V_I = 0			−3	−10	μA
		EN				−2	−100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

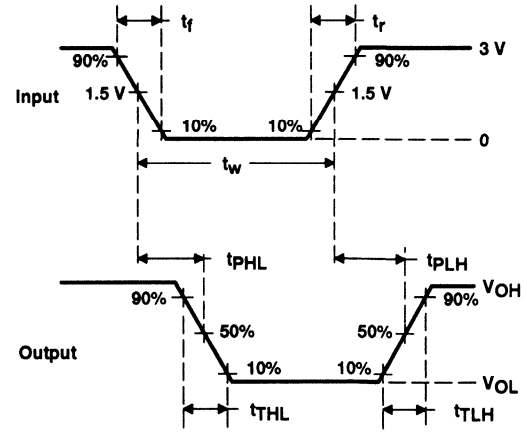
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, t_w = 10 μs, PRR = 5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

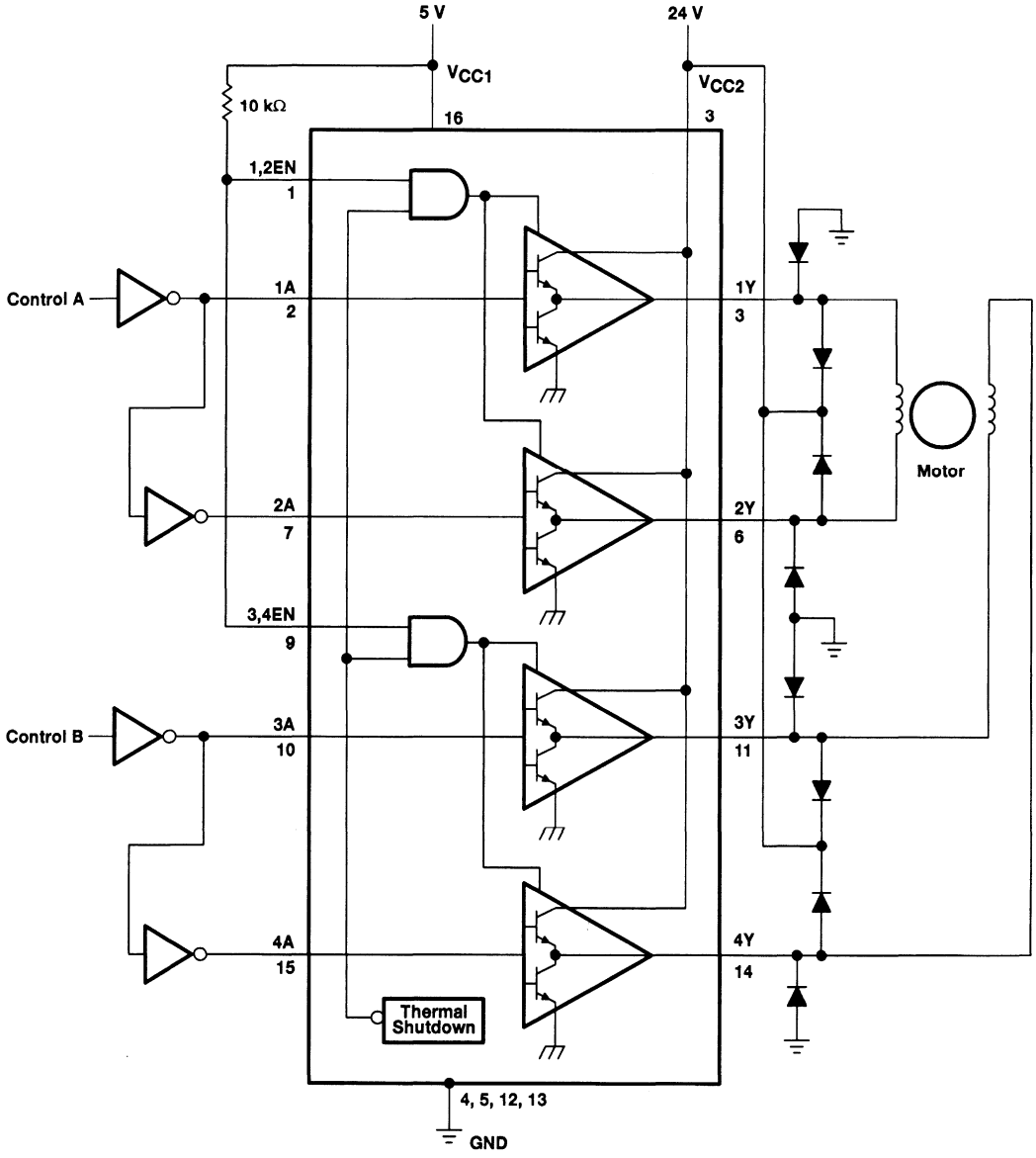
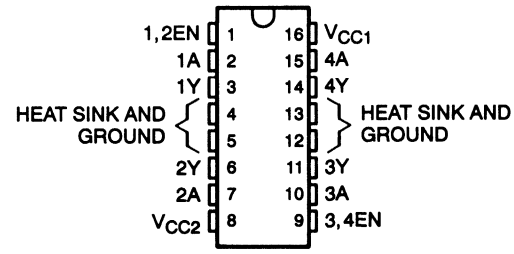


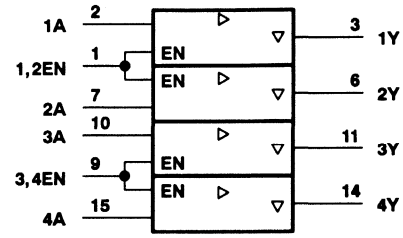
Figure 2. Two-Phase Motor Driver

- 600-mA Output Current Capability Per Driver
- Pulsed Current 1.2-A Per Driver
- Output Clamp Diodes for Inductive Transient Suppression
- Wide Supply Voltage Range 4.5 V to 36 V
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- High-Noise-Immunity Inputs
- Functional Replacement for SGS L293D

NE PACKAGE
(TOP VIEW)

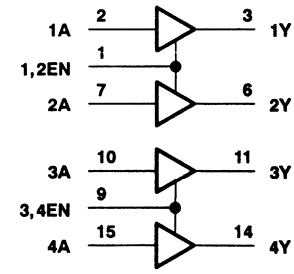


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



description

The L293D is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to 600-mA at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are TTL-compatible. Each output is a complete totem-pole drive circuit with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled, and their outputs are active and in phase with their inputs. External high-speed output clamp diodes should be used for inductive transient suppression. When the enable input is low, those drivers are disabled, and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A V_{CC1} terminal, separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation.

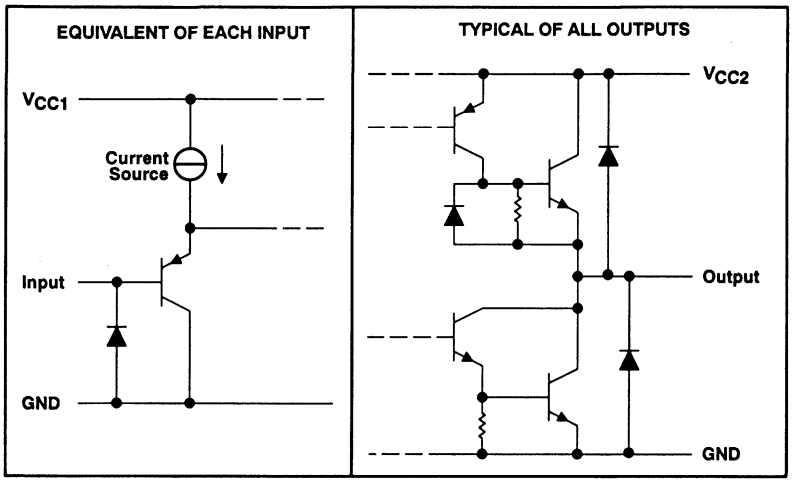
The L293D is designed for operation from 0°C to 70°C.

FUNCTION TABLE
(each driver)

INPUTS‡		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level, L = low level,
X = irrelevant, Z = high-impedance (off)
‡ In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1} (see Note 1) ..... 36 V
Output supply voltage, V_{CC2} ..... 36 V
Input voltage, V_I ..... 7 V
Output voltage range ..... −3 V to V_{CC2} + 3 V
Peak output current (nonrepetitive, t ≤ 100 μs) ..... ±1.2 A
Continuous output current, I_O ..... ±600 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Notes 2 and 3) ..... 2075 mW
Continuous total dissipation at 80°C case temperature (see Note 3) ..... 5000 mW
Operating case or virtual junction temperature range ..... −40°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
3. For operation above 25°C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		V_{CC1}	36	V
High-level input voltage, V_{IH}	$V_{CC1} \le 7$ V	2.3	V_{CC1}	V
	$V_{CC1} \ge 7$ V	2.3	7	
Low-level input voltage, V_{IL}		−0.3†	1.5	V
Operating free-air temperature, T_A		0	70	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.

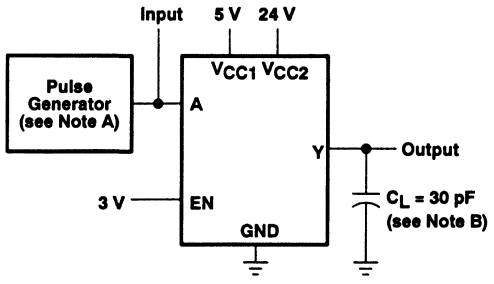
electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −0.6 A		V_{CC2}−1.8	V_{CC2}−1.4		V
V_{OL}	Low-level output voltage		I_{OL} = 0.6 A			1.2	1.8	V
V_{OKH}	High-level output clamp voltage		I_{OK} = −0.6 A			V_{CC2}+1.3		V
V_{OKL}	Low-level output clamp voltage		I_{OK} = −0.6 A			1.3		V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	μA
		EN				0.2	±10	
I_{IL}	Low-level input current	A	V_I = 0			−3	−10	μA
		EN				−2	−100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

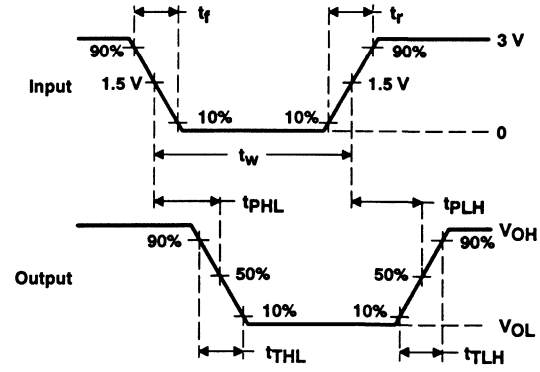
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, t_w = 10 μs, PRR = 5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

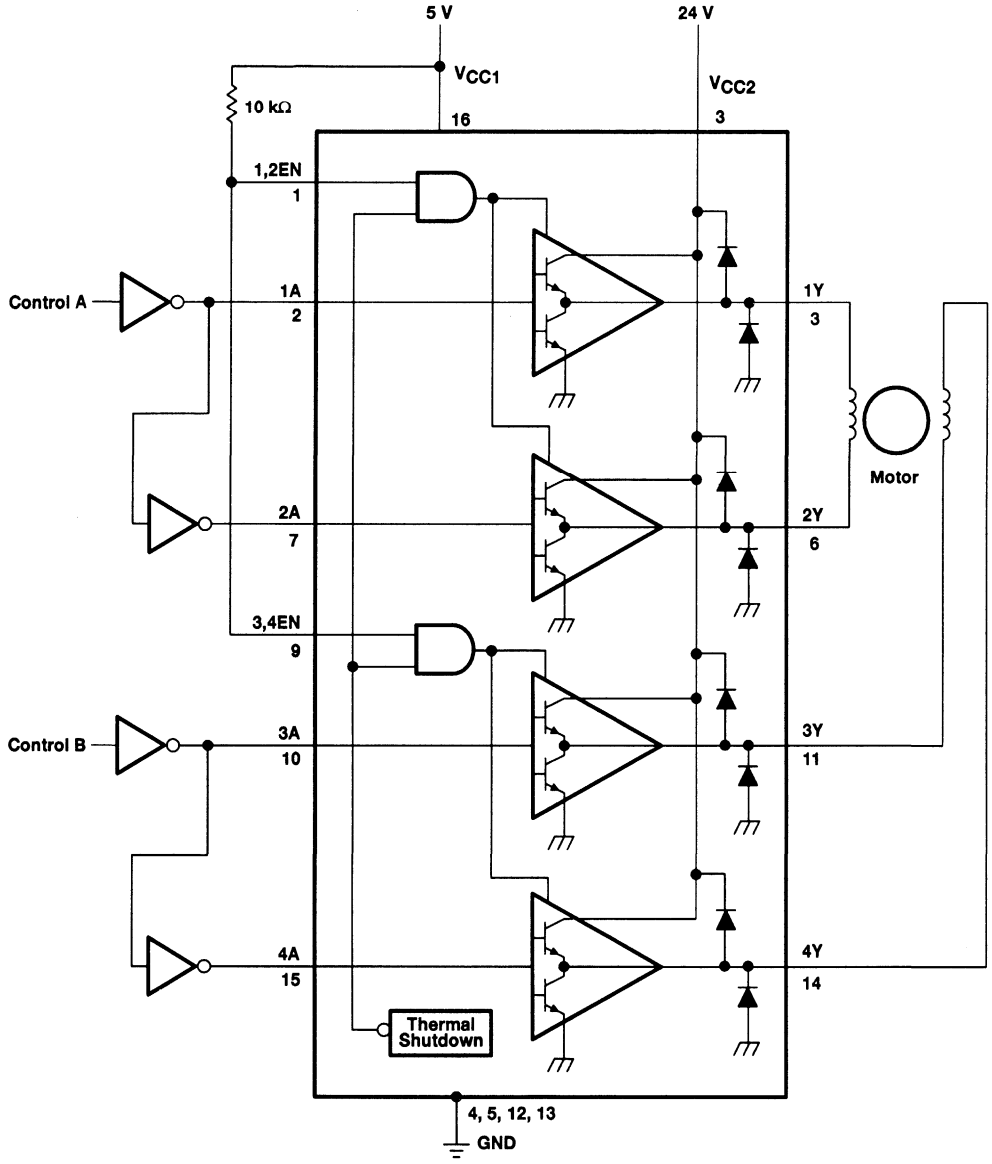


Figure 2. Two-Phase Motor Driver

SLRS011 – D2942, OCTOBER 1986 – REVISED JUNE 1990

- **2-A Output Current Capability Per Full-H Driver**
- **Wide Range of Output Supply Voltage . . . 5 V to 46 V**
- **Separate Input-Logic Supply Voltage**
- **Thermal Shutdown**
- **Internal Electrostatic Discharge Protection**
- **High Noise Immunity**
- **Functional Replacement for SGS L298**

description

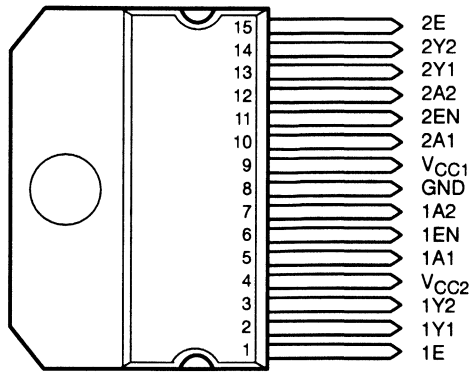
The L298 is a dual high-current full-H (bridge) driver designed to provide bidirectional drive currents of up to 2 A at voltages from 5 V to 46 V. It is designed to drive inductive loads such as relays, solenoids, dc motors, stepping motors, and other high-current or high-voltage loads in positive-supply applications. All inputs are TTL compatible. Each output (Y) is a complete totem-pole drive with a Darlington transistor sink and a pseudo-Darlington source. Each full-H driver is enabled separately. Outputs 1Y1 and 1Y2 are enabled by 1EN, and outputs 2Y1 and 2Y2 are enabled by 2EN. When an EN input is high, the associated channels are active. When an EN input is low, the associated channels are off (i.e., in the high-impedance state).

Each half of the device forms a full-H reversible driver suitable for solenoid or motor applications. The current in each full-H driver can be monitored by connecting a resistor between the sense output terminal 1E and GND and another resistor between sense output terminal 2E and GND.

External high-speed output-clamp diodes should be used for inductive transient suppression. To minimize device power dissipation, V_{CC1}, separate from V_{CC2}, is provided for the logic inputs.

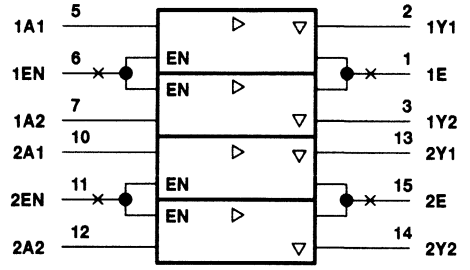
The L298 is designed for operation from 0°C to 70°C.

KV PACKAGE
(TOP VIEW)



The tab is electrically connected to GND.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

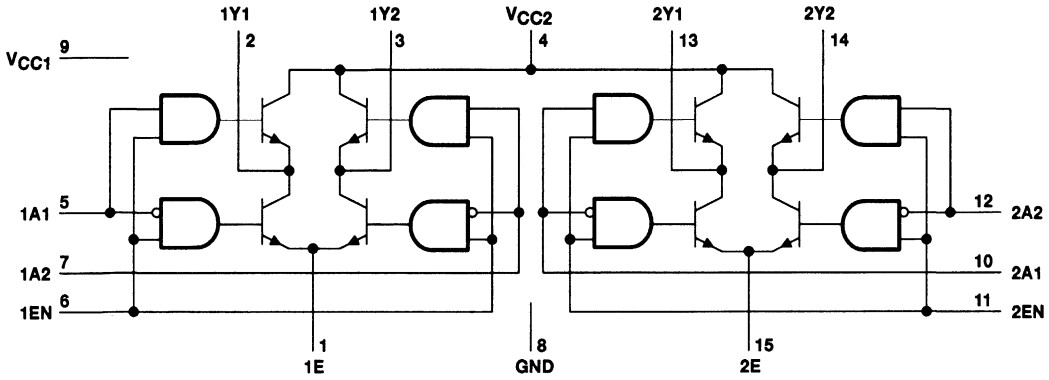
FUNCTION TABLE
(each channel)

INPUTS ‡		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

‡ In the thermal shutdown mode, the outputs are in the high-impedance state regardless of the input levels.

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1}, (see Note 1) ..... 7 V
Output supply voltage, V_{CC2} ..... 50 V
Input voltage range at A or EN, V_I ..... −0.3 V to 7 V
Output voltage range, V_O ..... −2 V to V_{CC2} + 2 V
Emitter terminal (1E and 2E) voltage range, V_E ..... −0.5 V to 2.3 V
Emitter terminal (1E and 2E) voltage (nonrepetitive, $t_w \leq 50$ µs) ..... −1 V
Peak output current, I_{OM} (nonrepetitive, $t_w \leq 0.1$ ms) ..... ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%)) ..... ±2.5 A
Continuous output current, I_O ..... ±2 A
Peak combined output current for each full-H driver (see Note 2)
(nonrepetitive, $t_w \leq 0.1$ ms) ..... ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) ..... ±2.5 A
Continuous combined output current for each full-H driver (see Note 2) ..... 3.575 W
Continuous dissipation at (or below) 25°C free-air temperature (see Note 3) ..... 3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 3) ..... 25 W
Operating free-air, case, or virtual junction temperature range ..... −40°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network GND, unless otherwise noted.
2. Combined output current applies to each of the two full-H drivers individually. This current is the sum of the currents at outputs 1Y1 and 1Y2 for full-H driver 1 and the sum of the currents at outputs 2Y1 and 2Y2 for full-H driver 2. The full-H drivers can carry the rated combined current simultaneously.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		5	46	V
Emitter terminal (1E or 2E) voltage, V_E (see Note 4)		−0.5†	2	V
			V_{CC1} −3.5	
			V_{CC2} −4	
High-level input voltage, V_{IH} (see Note 4)	A	2.3	V_{CC1}	V
			V_{CC2} −2.5	
	EN	2.3	7	
			V_{CC1}	
Low-level input voltage at A or EN, V_{IL}		−0.3†	1.5	V
Output current, I_O			±2	A
Commutation frequency			40	kHz
Operating free-air temperature, T_A		0	70	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for emitter terminal voltage and logic voltage levels.

NOTE 4: For optimum device performance, the maximum recommended voltage at any A input is 2.5 V lower than V_{CC2}, the maximum recommended voltage at any EN input is V_{CC1}, and the maximum recommended voltage at any emitter terminal is 3.5 V lower than V_{CC1} and 4 V lower than V_{CC2}.

electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_J = 25°C (unless otherwise noted)

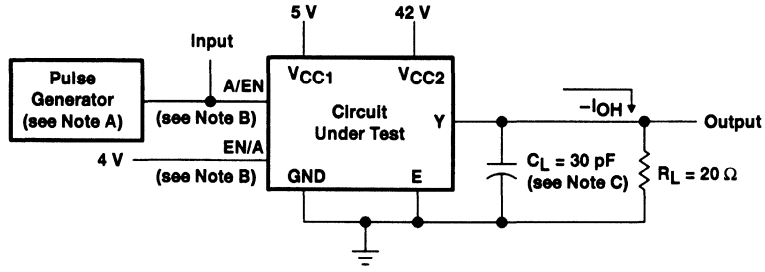
PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1 A			V_{CC2}−1.8	V_{CC2}−1.2		V
			I_{OH} = −2 A			V_{CC2}−2.8	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		I_{OL} = 1 A				V_E +1.2	V_E +1.8	V
			I_{OL} = 2 A				V_E +1.7	V_E +2.6	
V_{drop}	Total source plus sink output voltage drop		I_{OH} = −1 A, I_{OL} = 1 A		See Note 5		2.4	3.4	V
			I_{OH} = −2 A, I_{OL} = 1 A				3.5	5.2	
I_{IH}	High-level input current	A	$V_I = V_{IH}$				30	100	µA
		EN	$V_I = V_{IH} \le V_{CC1}$ −0.6 V				30	100	
I_{IL}	Low-level input current		I_I = 0 to 1.5 V					−10	µA
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level			7	12	mA
				All outputs at low level			24	32	
				All outputs at high impedance			4	6	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level			38	50	mA
				All outputs at low level			13	20	
				All outputs at high impedance				2	

NOTE 5: The V_{drop} specification applies for I_{OH} and I_{OL} applied simultaneously to different output channels. $V_{drop} = V_{CC2} - V_{OH} + V_{OL} - V_E$.

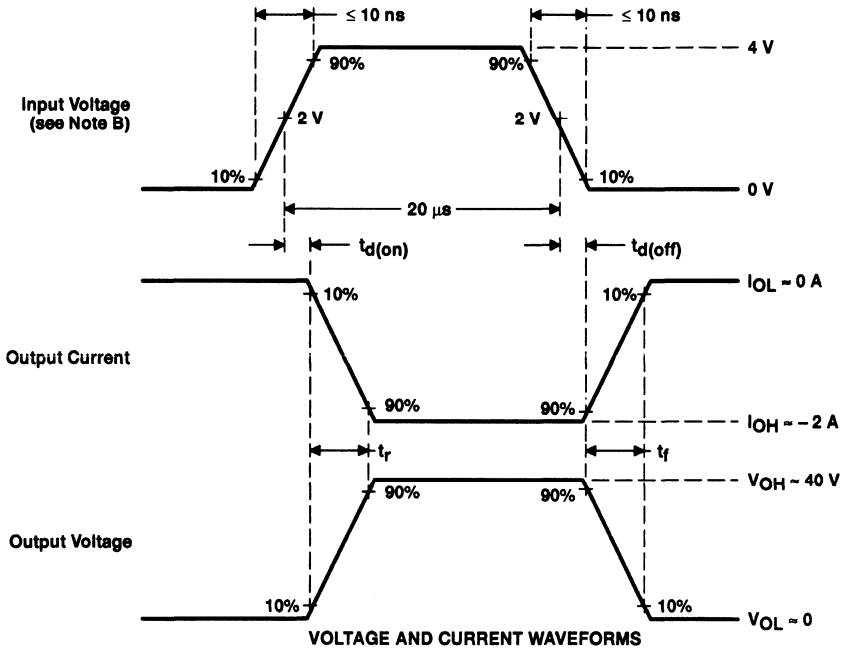
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time, source current from A input	C_L = 30 pF, See Figure 1		2.5		µs
$t_{d(off)}$	Turn-off delay time, source current from A input			1.7		µs
t_r	Rise time, source current (turning on)			0.4		µs
t_f	Fall time, source current (turning off)			0.2		µs
$t_{d(on)}$	Turn-on delay time, source current from EN input			2.5		µs
$t_{d(off)}$	Turn-off delay time, source current from EN input			1.7		µs
$t_{d(on)}$	Turn-on delay time, source current from A input	C_L = 30 pF, See Figure 2		1.5		µs
$t_{d(off)}$	Turn-off delay time, source current from A input			0.7		µs
t_r	Rise time, source current (turning on)			0.2		µs
t_f	Fall time, source current (turning off)			0.2		µs
$t_{d(on)}$	Turn-on delay time, sink current from EN input			1.5		µs
$t_{d(off)}$	Turn-off delay time, sink current from EN input			0.7		µs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

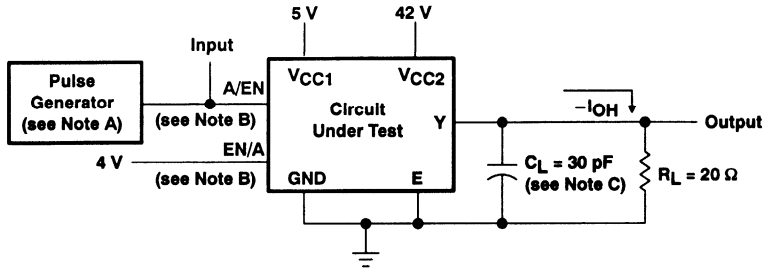


VOLTAGE AND CURRENT WAVEFORMS

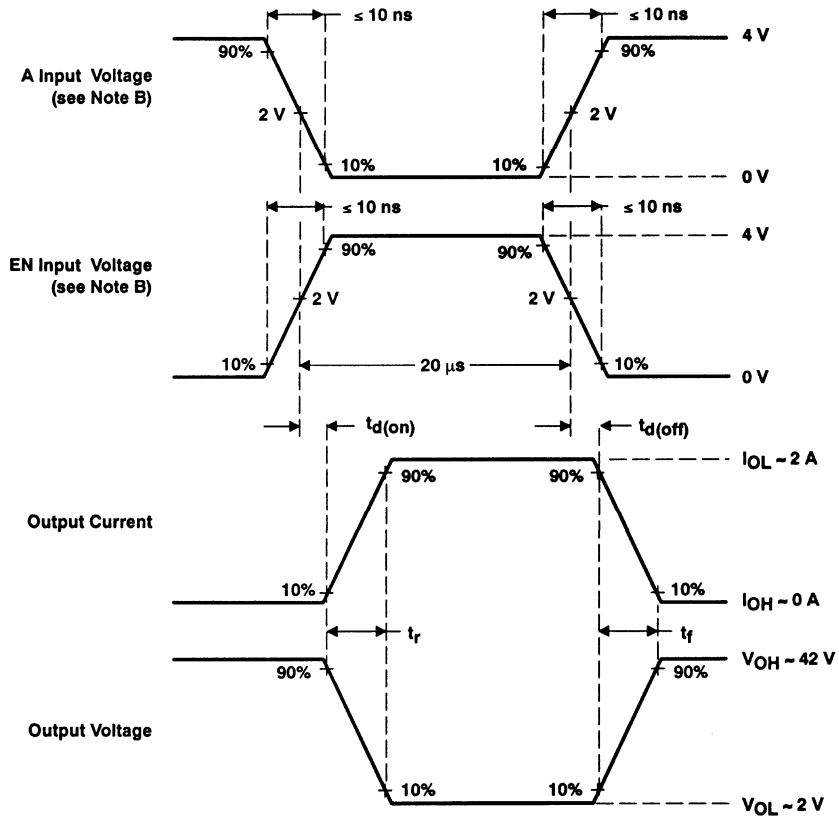
NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 0 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

Figure 1. Sink Current Test Circuit and Voltage and Current Waveforms From Data and Enable Inputs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 4 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Sink Current Switching Times From Data and Enable Inputs

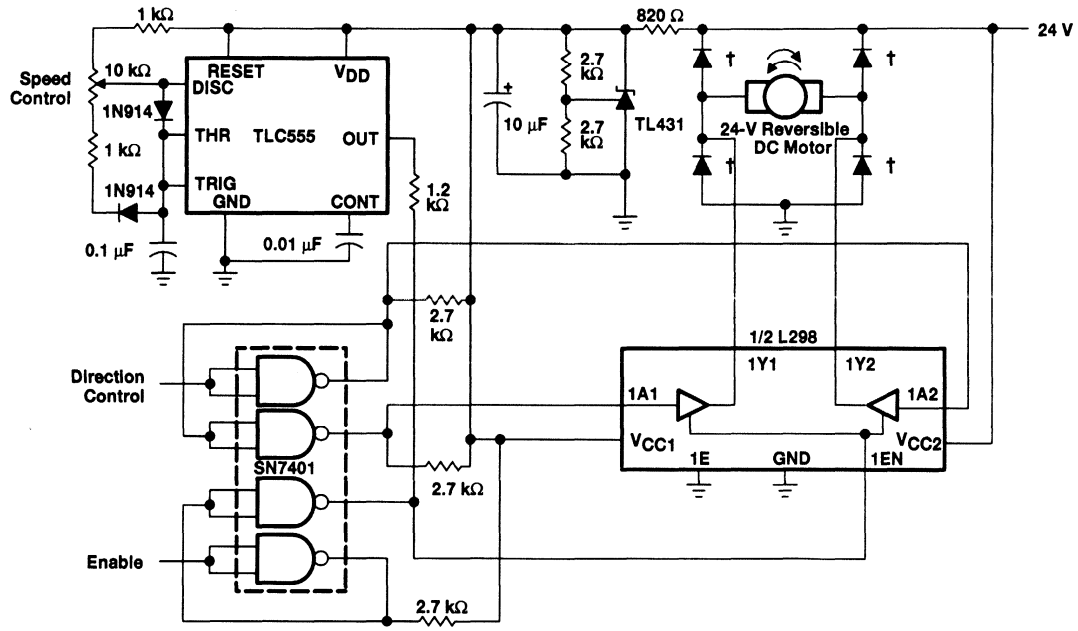
APPLICATION INFORMATION

This circuit shows one half of an L298 used to provide full-H bridge drive for a 24-V 2-A dc motor. Speed control is achieved with a TLC555 timer. This provides variable duty cycle pulses to the EN input of the L298. In this configuration, the operating frequency is approximately 1.2 kHz. The duty cycle is adjustable from 10% to 90% to provide a wide range of motor speeds. The motor direction is determined by the logic level at the direction control input. The circuit may be enabled or disabled by the logic level at the EN input. A 5-V supply for the logic and timer circuit is provided by a TL431 shunt regulator. For circuit operation, refer to the function table.

FUNCTION TABLE

ENABLE	DIRECTION CONTROL	1Y1	1Y2
H	H	source	sink
H	L	sink	source
L	X	disabled	disabled

X = don't care H = high level L = low level



† Diodes are 1N4934 or equivalent

Figure 3. L298 as Bidirectional DC Motor Driver

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT VERY HIGH SPEEDS

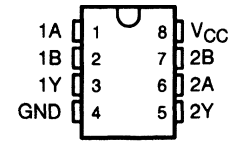
- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 20 V (After Conducting 300 mA)
- High-Speed Switching
- Circuit Flexibility for Varied Applications
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) With Copper Lead Frame Provides Cooler Operation and Improved Reliability
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SUMMARY OF DEVICES

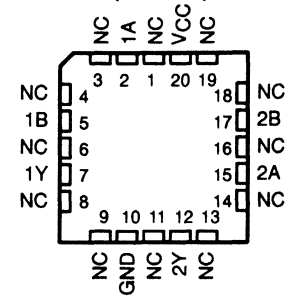
DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55451B	AND†	FK, JG
SN55452B	NAND	JG
SN55453B	OR	FK, JG
SN55454B	NOR	JG
SN75451B	AND	D, P
SN75452B	NAND	D, P
SN75453B	OR	D, P
SN75454B	NOR	D, P

† With output transistor base connected externally to output of gate

SN55451B, SN55452B,
SN55453B, SN55454B . . . JG PACKAGE
SN75451B, SN75452B,
SN75453B, SN75454B . . . D OR P PACKAGE
(TOP VIEW)



SN55451B, SN55452B
SN55453B, SN55454B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN55451B through SN55454B and SN75451B through SN75454B are dual peripheral drivers designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the SN75450 family and the SN75450A family devices manufactured previously. The speed of the devices is equal to that of the SN75450 family, and the parts are designed to ensure freedom from latch-up. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively (assuming positive logic), with the output of the logic gates internally connected to the bases of the npn output transistors.

The SN55' drivers are characterized for operation over the full military range of −55°C to 125°C. The SN75' drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55'	SN75'	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	V
Off-state output voltage		30	30	V
Continuous collector or output current (see Note 3)		400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)		500	500	mA
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. Voltage values are with respect to network GND, unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

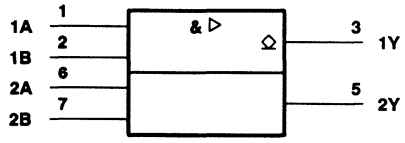
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

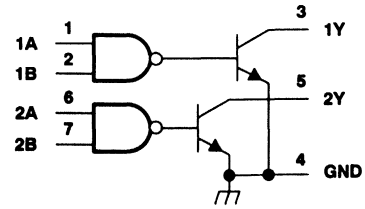
	SN55'			SN75'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.
Pin numbers shown are for the D, JG, and P packages.

logic diagram (positive logic)

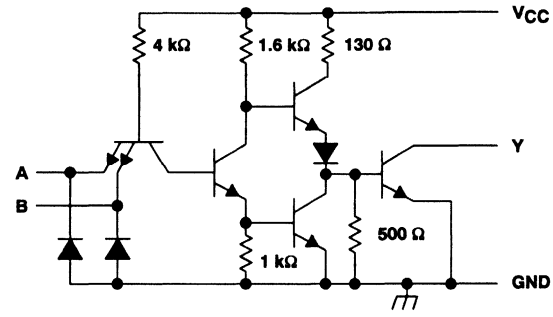


FUNCTION TABLE (each driver)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic: $Y = AB$ or $\overline{\overline{A}+\overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

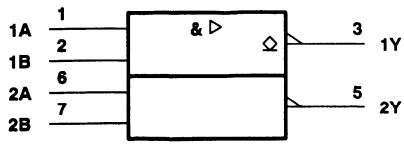
PARAMETER		TEST CONDITIONS‡	SN55451B			SN75451B			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 30 V			300			100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		52	65		52	65	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				18	25	
t_{TLH}	Transition time, low-to-high-level output				5	8	
t_{THL}	Transition time, high-to-low-level output				7	12	
V_{OH}	High-level output voltage after switching	SN55451B	V_S = 20 V, I_O ≈ 300 mA, See Figure 2		V_S−6.5		mV
		SN75451B		V_S−6.5			

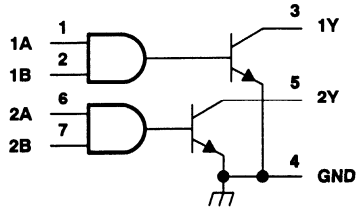
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

Pin numbers shown are for the D, JG, and P packages.

logic diagram (positive logic)

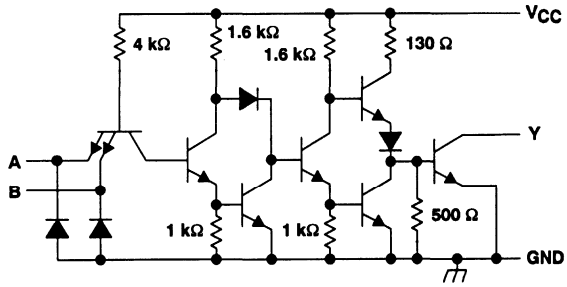


FUNCTION TABLE (each driver)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
$Y = \overline{AB}$ or $\overline{A}+\overline{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

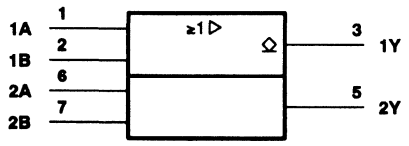
PARAMETER		TEST CONDITIONS‡	SN55452B			SN75452B			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 30 V			300			100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0		11	14		11	14	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		56	71		56	71	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

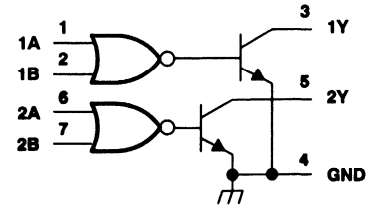
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				24	35	
t_{TLH}	Transition time, low-to-high-level output				5	8	
t_{THL}	Transition time, high-to-low-level output				7	12	
V_{OH}	High-level output voltage after switching	SN55452B	V_S = 20 V, I_O ≈ 300 mA, See Figure 2		V_S−6.5		mV
		SN75452B		V_S−6.5			

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.
Pin numbers shown are for the D, JG, and P packages.

logic diagram (positive logic)

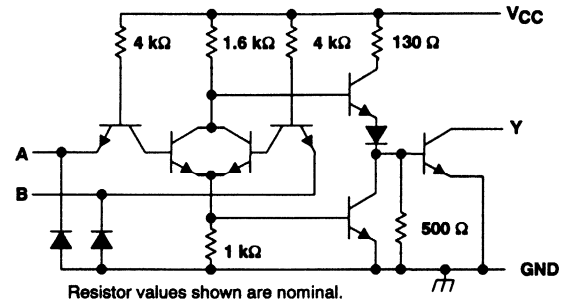


FUNCTION TABLE
(each driver)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic: $Y = A+B$ or $\overline{\overline{A}\,\overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS‡	SN55453B			SN75453B			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 30 V			300			100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		54	68		54	68	mA

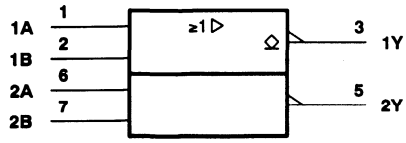
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				18	25	
t_{TLH}	Transition time, low-to-high-level output				5	8	
t_{THL}	Transition time, high-to-low-level output				7	12	
V_{OH}	High-level output voltage after switching	SN55453B	V_S = 20 V, I_O ≈ 300 mA, See Figure 2	V_S−6.5			mV
		SN75453B		V_S−6.5			

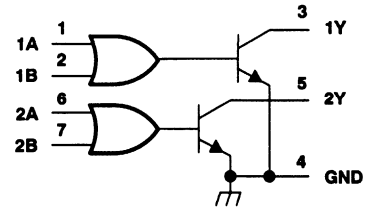
SLRS021A – D2217, DECEMBER 1976 – REVISED MAY 1993

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.
Pin numbers shown are for the D, JG, and P packages.

logic diagram (positive logic)

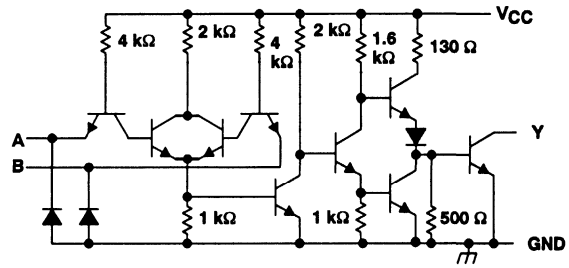


FUNCTION TABLE
(each driver)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

positive logic:
$Y = \overline{A+B}$ or $\overline{AB}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

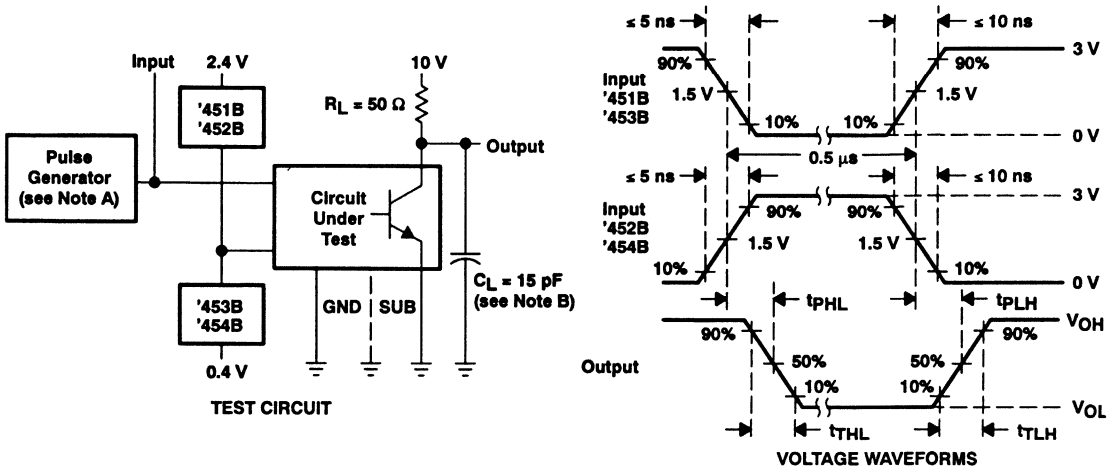
PARAMETER		TEST CONDITIONS‡	SN55454B			SN75454B			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 30 V			300			100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		61	79		61	79	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

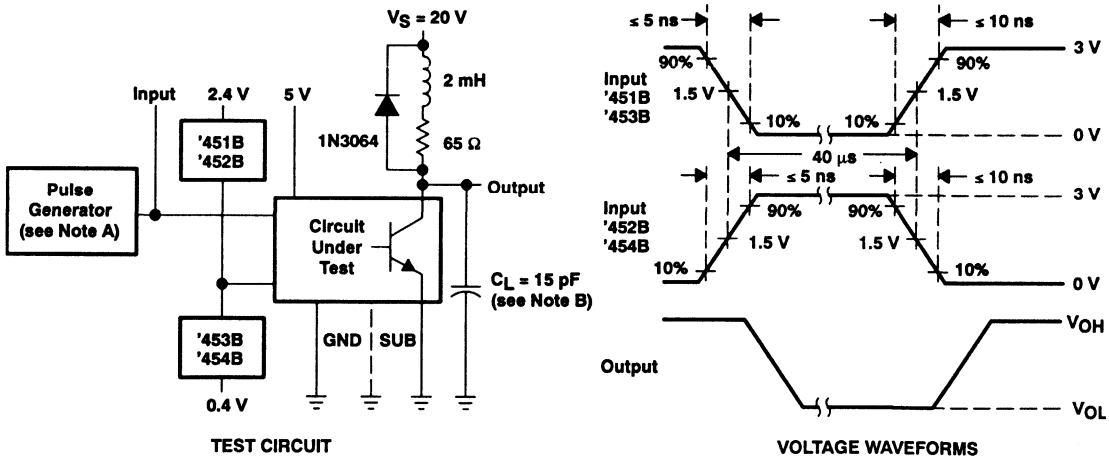
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		27	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				24	35	
t_{TLH}	Transition time, low-to-high-level output				5	8	
t_{THL}	Transition time, high-to-low-level output				7	12	
V_{OH}	High-level output voltage after switching	SN55454B	V_S = 20 V, I_O ≈ 300 mA, See Figure 2	V_S−6.5			mV
		SN75454B		V_S−6.5			

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

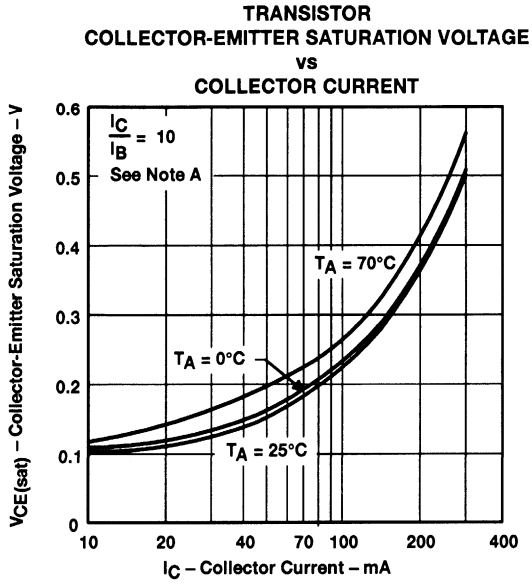
Figure 1. Test Circuit and Voltage Waveforms, Complete Drivers



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms for Latch-Up Test of Complete Drivers

TYPICAL CHARACTERISTICS



NOTE A: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤ 2%.

Figure 3

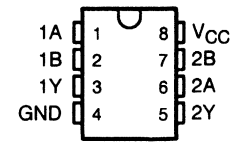
PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

- **Characterized for Use to 300 mA**
- **High-Voltage Outputs**
- **No Output Latch-Up at 30 V (After Conducting 300 mA)**
- **Medium-Speed Switching**
- **Circuit Flexibility for Varied Applications and Choice of Logic Function**
- **TTL-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltages**
- **Plastic DIP (P) With Copper Lead Frame for Cooler Operation and Improved Reliability**
- **Package Options Include Plastic Small Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

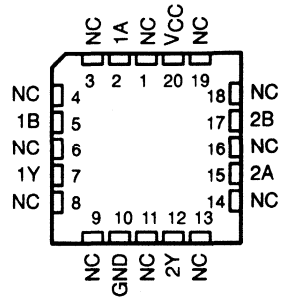
SUMMARY OF SERIES 55461/75461

DEVICE	LOGIC	PACKAGES
SN55461	AND	FK, JG
SN55462	NAND	FK, JG
SN55463	OR	FK, JG
SN55464	NOR	FK, JG
SN75461	AND	D, P
SN75462	NAND	D, P
SN75463	OR	D, P

SN55461, SN55462, SN55463, SN55464 . . . JG PACKAGE
SN75461, SN75462,SN75463 . . . D OR P PACKAGE
(TOP VIEW)



SN55461, SN55462, SN55463, SN55464 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These dual peripheral drivers are functionally interchangeable with SN55451B through SN55454B and SN75451B through SN75453B peripheral drivers, but are designed for use in systems that require higher breakdown voltages than those devices can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively (assuming positive logic), with the output of the gates internally connected to the bases of the npn output transistors.

Series SN55461 drivers are characterized for operation over the full military temperature range of −55°C to 125°C. Series SN75461 drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55'	SN75'	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	V
Off-state output voltage		35	35	V
Continuous collector or output current (see Note 3)		400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)		500	500	mA
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range, T_A		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. Voltage values are with respect to network GND unless otherwise specified.
2. This is the voltage between two emitters A and B.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

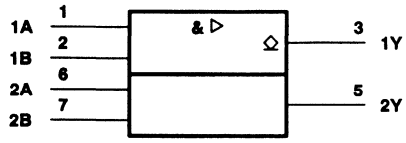
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	–

recommended operating conditions

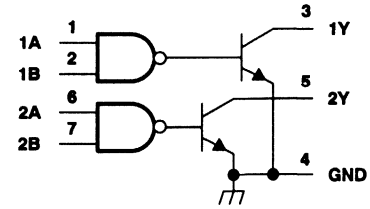
	SN55'			SN75'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

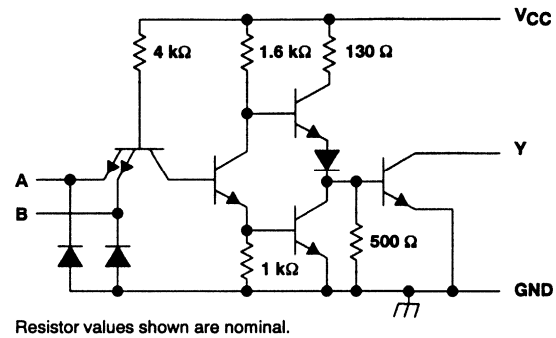


FUNCTION TABLE
(each driver)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic: $Y = AB$ or $\overline{\overline{A} + \overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

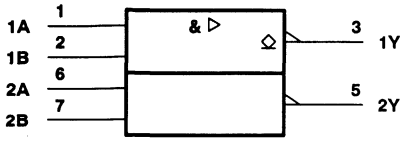
PARAMETER		TEST CONDITIONS†	SN55461			SN75461			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		56	76		56	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

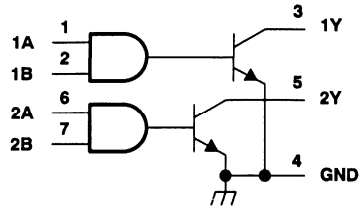
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output				25	40	
t_{TLH}	Transition time, low-to-high-level output				8	20	
t_{THL}	Transition time, high-to-low-level output				10	20	
V_{OH}	High-level output voltage after switching	SN55461	V_S = 30 V, I_O ≈ 300 mA, See Figure 2		V_S−10		mV
		SN75461			V_S−10		

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

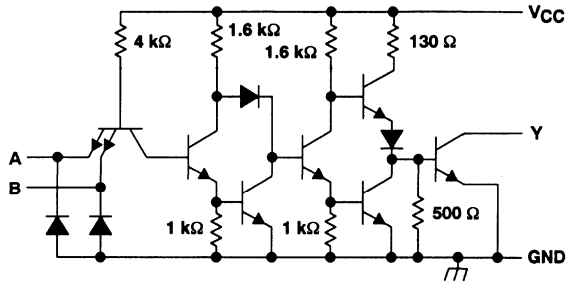


FUNCTION TABLE (each driver)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

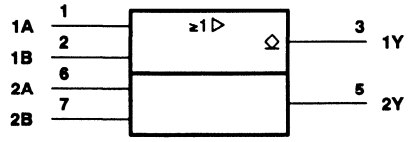
PARAMETER		TEST CONDITIONS†	SN55462			SN75462			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		61	76		61	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

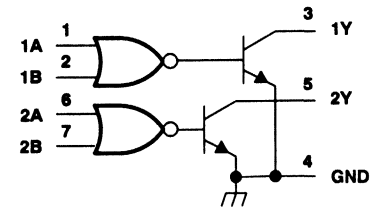
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	50	
t_{TLH}	Transition time, low-to-high-level output				13	25	
t_{THL}	Transition time, high-to-low-level output				10	20	
V_{OH}	High-level output voltage after switching	SN55462	V_S = 30 V, I_O ≈ 300 mA, See Figure 2	V_S−10			mV
		SN75462		V_S−10			

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

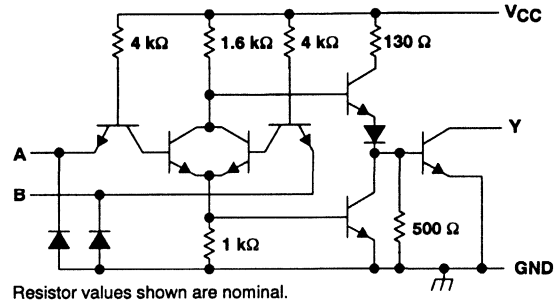


FUNCTION TABLE
(each driver)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
$Y = A + B$ or $\overline{\overline{A}\,\overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

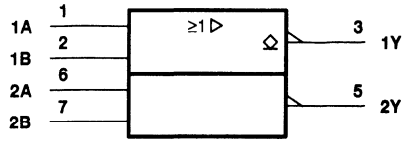
PARAMETER		TEST CONDITIONS†	SN55463			SN75463			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		58	76		58	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

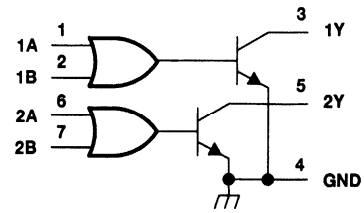
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output				25	40	
t_{TLH}	Transition time, low-to-high-level output				8	25	
t_{THL}	Transition time, high-to-low-level output				10	25	
V_{OH}	High-level output voltage after switching	SN55463	V_S = 30 V, I_O ≈ 300 mA, See Figure 2		V_S−10		mV
		SN75463			V_S−10		

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JG package.

logic diagram (positive logic)

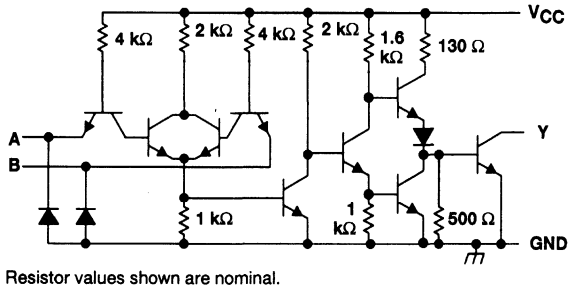


FUNCTION TABLE
(each driver)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

positive logic:
$Y = \overline{A} + \overline{B}$ or $\overline{A}\,\overline{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

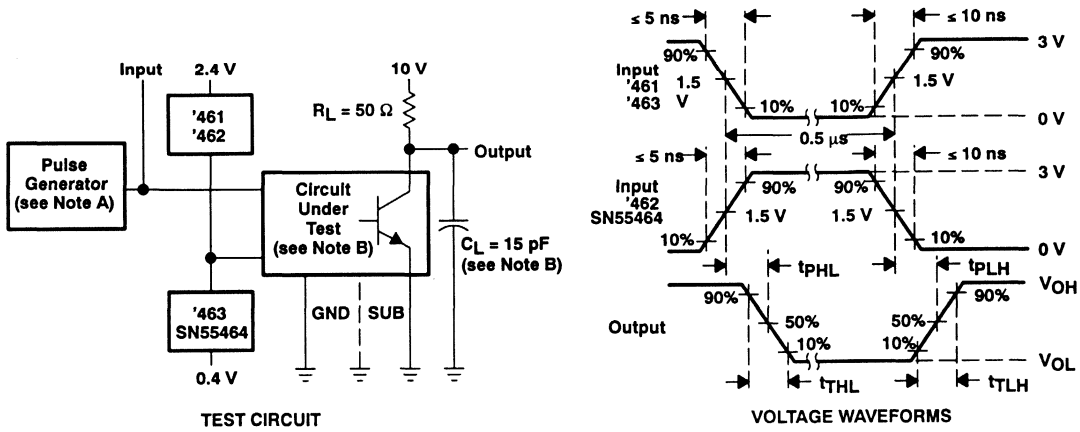
PARAMETER		TEST CONDITIONS‡			SN55464 MIN	SN55464 TYP‡	SN55464 MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN,	V_{IL} = 0.8 V,	V_{OH} = 35 V			300	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN,	V_{IH} = MIN,	I_{OL} = 100 mA		0.25	0.5	V
		V_{CC} = MIN,	V_{IH} = MIN,	I_{OL} = 300 mA		0.5	0.8	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	V_I = 0			14	19	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	V_I = 5 V			67	85	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

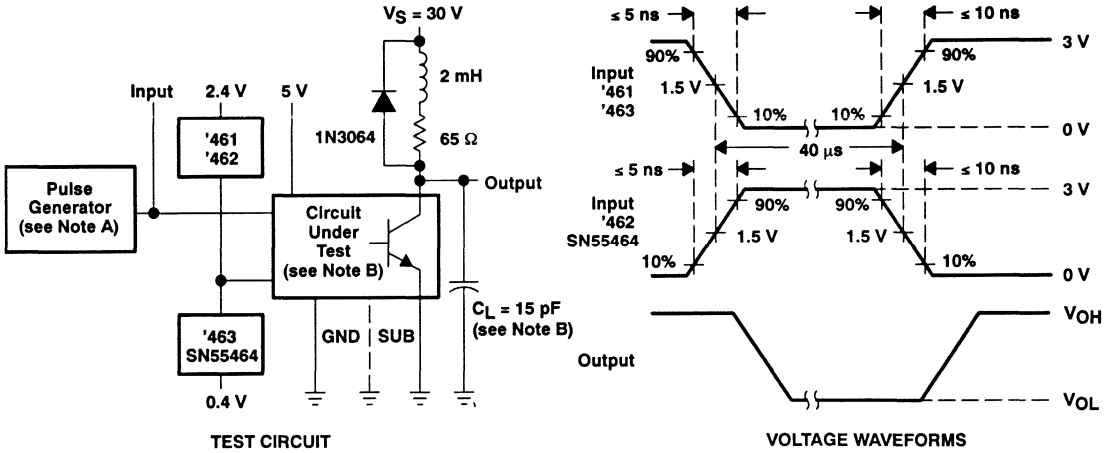
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, R_L = 50 Ω,	C_L = 15 pF, See Figure 1			40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output					30	50	
t_{TLH}	Transition time, low-to-high-level output					8	20	
t_{THL}	Transition time, high-to-low-level output					10	20	
V_{OH}	High-level output voltage after switching	V_S = 30 V, See Figure 2	I_O ≈ 300 mA,		V_S−10			mV

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Switching Times



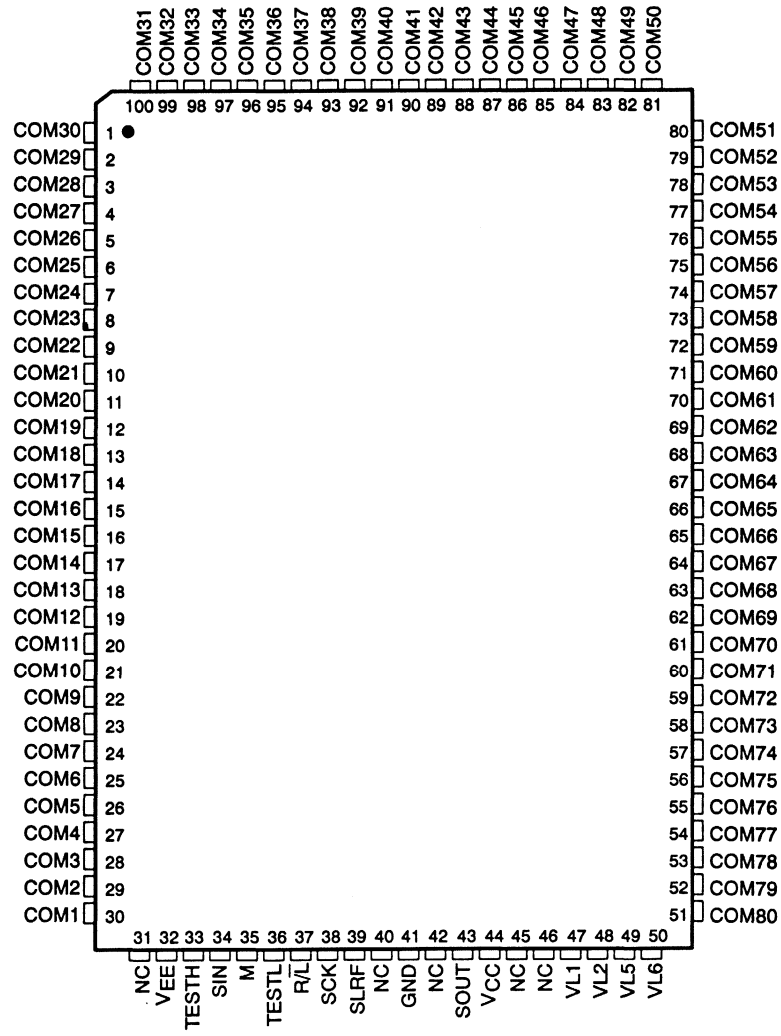
NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms for Latch-Up Test

SGLS042 – D4012, JANUARY 1992

- Duty Cycle for LCD Driver . . . 1/100 to 1/480
- V_{EE} Voltage for LCD Driver . . . 14 V to 26 V (40 V Max)
- 80 Channel Outputs
- 5-V Power Supply Voltage
- CMOS Si-Gate High-Voltage Technology
- 100-Terminal Ceramic Flat Package

HS PACKAGE
(TOP VIEW)



NC–No internal connection

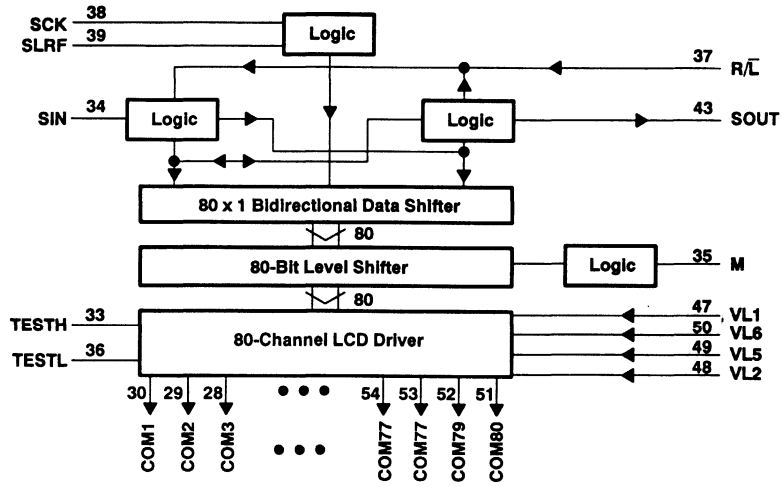
description

The SN553491 row driver is a monolithic silicon gate CMOS integrated circuit designed to drive the row electrodes of a liquid crystal flat panel display.

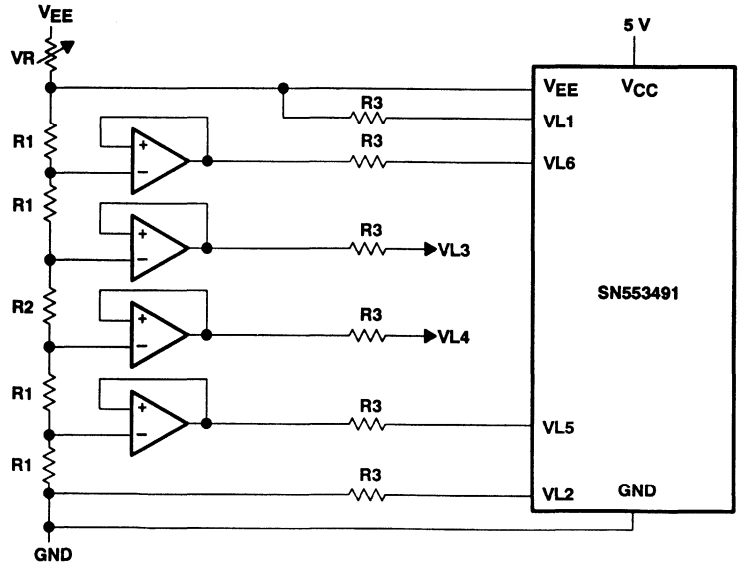
description (continued)

This device consists of an 80-bit shift register, an 80-bit level shifter, and an 80-channel output driver. Serial data is entered into the shift register on either the rising or falling edge of the shift clock. SOUT is used to cascade additional devices.

functional block diagram



power supply circuit



Resistors marked with same number have equal value.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
COM1–COM80	1–30, 51–100	O	Common (row) drive signal output, see Table 1.
GND	41		Ground
M	35	I	Frame signal input
NC	31, 40, 42, 45, and 46		No internal connection
R/$\overline{L}$	37	I	Select right or left shift of register V_{CC}: Right shift, SIN→ R1→ R2→ R3→ R80→ SOUT V_{SS}: Left shift, SIN→ R80→ R79→ R2→ R1→ SOUT R1 → COM1 output R2 → COM2 output I I I R80 → COM80 output
SCK	38	I	Shift clock
SIN	34	I	Serial input
SLRF	39	I	Select rise or fall edge of SCK for register and output shift V_{CC}: Rise edge of SCK GND: Fall edge of SCK
SOUT	43	O	Serial output
TESTH	33	I	Output test for on level of LCD (= V_{CC}). See Table 2 for output test levels.
TESTL	36	I	Output test for off level of LCD (= V_{CC}). See Table 2 for output test levels.
V_{CC}	44		Voltage supply
V_{EE}	32		Output bias voltage for LCD
VL1, VL2, VL5, VL6	47–50		Output supplies for LCD VL1 and VL2 are on level of LCD, VL5 and VL6 are off level of LCD.

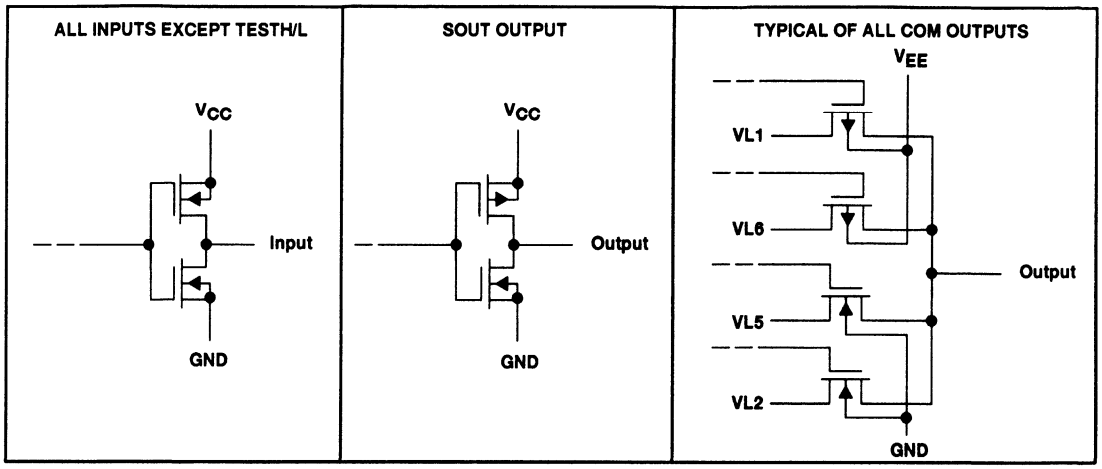
Table 1. Level for LCD Driving Signal

OUTPUT LEVEL	VL1	VL2	VL5	VL6
M	0	1	0	1
Data	1	1	0	0

Table 2. Output Test Levels

OUTPUT TEST	TESTH = V_{CC}		TESTL = V_{CC}		TESTH/L = V_{CC}	
M	1	0	1	0	1	0
Output Level	VL2	VL1	VL6	VL5	VL6	VL5

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Output bias voltage range, V_{EE} ..... −0.3 V to 40 V
Input voltage range at SCK, SIN, M, SLRF, R/$\overline{L}$,V_I ..... −0.3 V to V_{CC} + 0.3 V
Output voltage range at SOUT, V_O ..... −0.3 V to V_{CC} + 0.3 V
Output supply voltage range, VLn for LCD (see Note 2) ..... −0.3 V to V_{EE} + 0.3 V
Input current, I_I ..... ± 10 mA
Output current, I_O: SOUT ..... 10 mA
COM1 to COM80 ..... 5 mA
Operating free-air temperature range, T_A ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to GND.
2. VLn voltage range should be under the following conditions: $V_{EE} \geq VL1 \geq VL6 \geq V_{EE} - 7$ V, and $7 \geq VL5 \geq VL2 \geq GND$.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Notes 1, 2, 3, and 4)			4.5	5	5.5	V
Supply voltage for LCD output	V_{EE}, VL1, VL6, VL5, VL2		14		26	V
High-level input voltage, V_{IH}	SCK, SIN, M, SLRF, R/$\overline{L}$, TESTH, TESTL		0.8 V_{CC}		V_{CC}	V
Low-level input voltage, V_{IL}	SCK, SIN, M, SLRF, R/$\overline{L}$, TESTH, TESTL		GND		0.2 V_{CC}	V
Operating free-air temperature, T_A			−55		125	°C
Pulse duration, clock high, $t_{w(SCKH)}$	At SCK,	SLRF = GND	125			ns
Pulse duration, clock low, $t_{w(SCKL)}$			5			µs
Pulse duration, clock high, $t_{w(SCKH)}$	At SCK,	SLRF = V_{CC}	5			µs
Pulse duration, clock low, $t_{w(SCKL)}$			125			ns
Setup time, SIN high or low, t_{su}			100			ns
Hold time, SIN high or low, t_h			100			ns
Output hold time, SOUT high or low, $t_{h(SO}$	C_L = 30 pF		100			ns
Clock frequency, f_{clock}	SCK				100	kHz

NOTES: 1. Voltage values are with respect to GND.
2. VLn voltage range should be under the following conditions: $V_{EE} \geq VL1 \geq VL6 \geq V_{EE} - 7$ V, and $7 \geq VL5 \geq VL2 \geq$ GND.
3. Turn on and off sequence of power must be as follows:
   Turn on sequence: V_{CC} → Input → V_{EE}
   Turn off sequence: V_{EE} → Input → V_{CC}.
4. VLn voltage range should be within Δ V (see Figure 1).

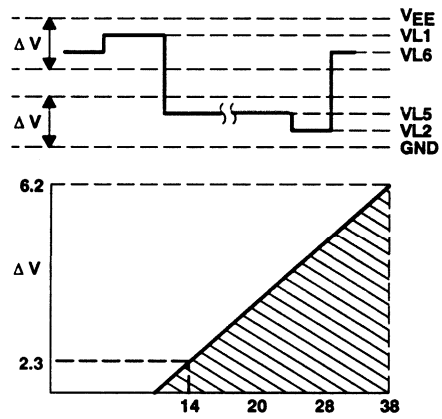


Figure 1

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

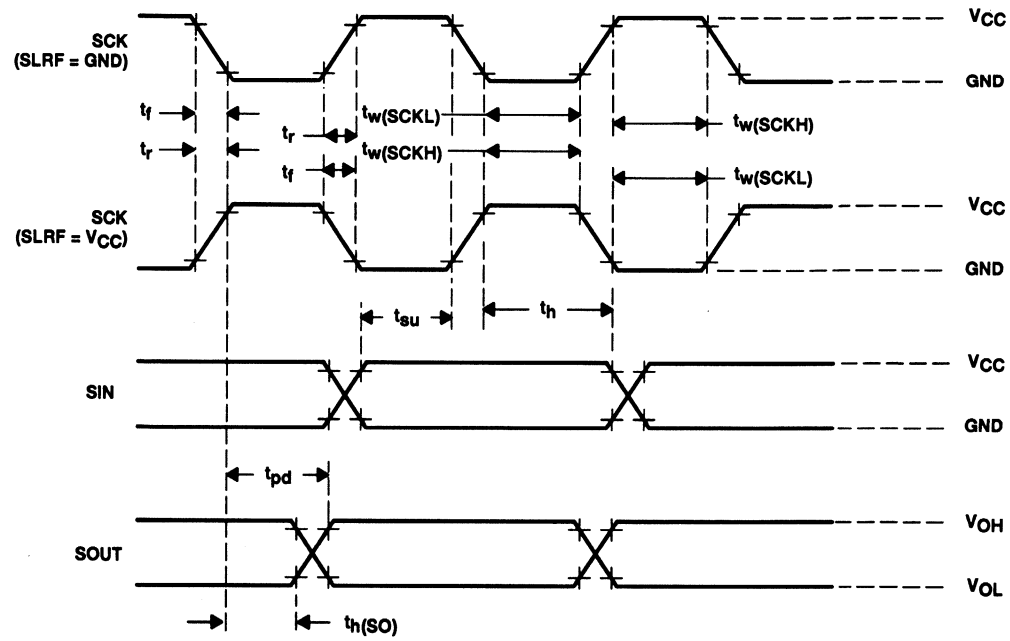
PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	SOUT	I_{OH} = −0.4 mA	V_{CC} −0.4			V
V_{OL}	Low-level output voltage	SOUT	I_{OL} = 0.4 mA			0.4	V
I_{IH}	High-level input current	SCK, SIN, M, SLRF, R/$\overline{L}$	V_{CC} = MAX, V_I = V_{CC}			5	µA
		TESTH, TESTL				500	µA
I_{IL}	Low-level input current	SCK, SIN, M, SLRF, R/$\overline{L}$	V_{CC} = MAX, V_I = GND			−5	µA
		TESTH, TESTL				−5	µA
Z_O	Output impedance	COM1 to COM80	I_O = 100 µA		3	8	kΩ
I_I	Input current	VLn	VL1 = VL6 = V_{EE}, GND, VL2 = VL5 = 7 V, GND			±50	µA
I_{CC}	Supply current	V_{CC}	V_{CC} = MAX, V_{EE} = MAX, V_I = V_{CC}, GND			200	µA
I_{EE}	Supply current	V_{EE}				2.5	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C, V_{CC} = 5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	Propagation delay time	SCK	SOUT	C_L = 30 pF		3	µs

PARAMETER MEASUREMENT INFORMATION



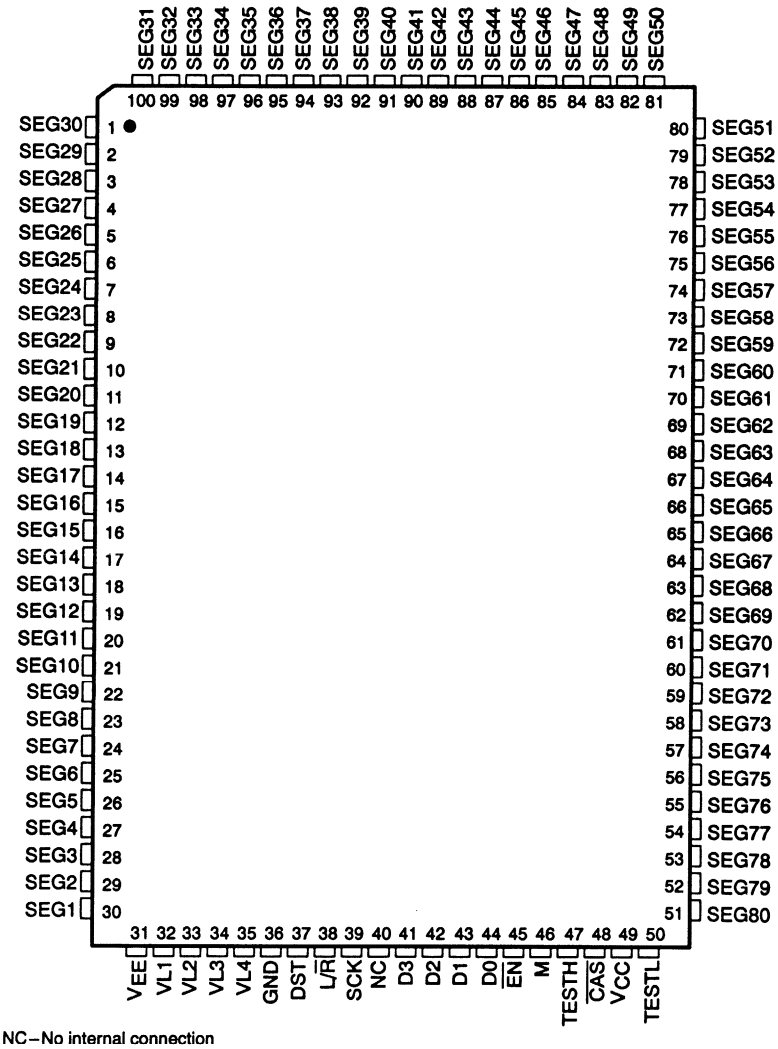
NOTE: $t_r \leq 30$ ns, $t_f \leq 30$ ns

Figure 2. Serial Clock Timing Diagram

SGLS043 – D4008, JANUARY 1992

- Duty Cycle for LCD Driver . . . 1/100 to 1/480
- V_{EE} Voltage for LCD Driver . . . 14 V to 26 V (40 V Max)
- 80 Channel Outputs
- 5-V Power Supply Voltage
- 4-Bit Data Bus
- CMOS Si-Gate High-Voltage Technology
- 100-Terminal Ceramic Flat Package

HS PACKAGE
(TOP VIEW)



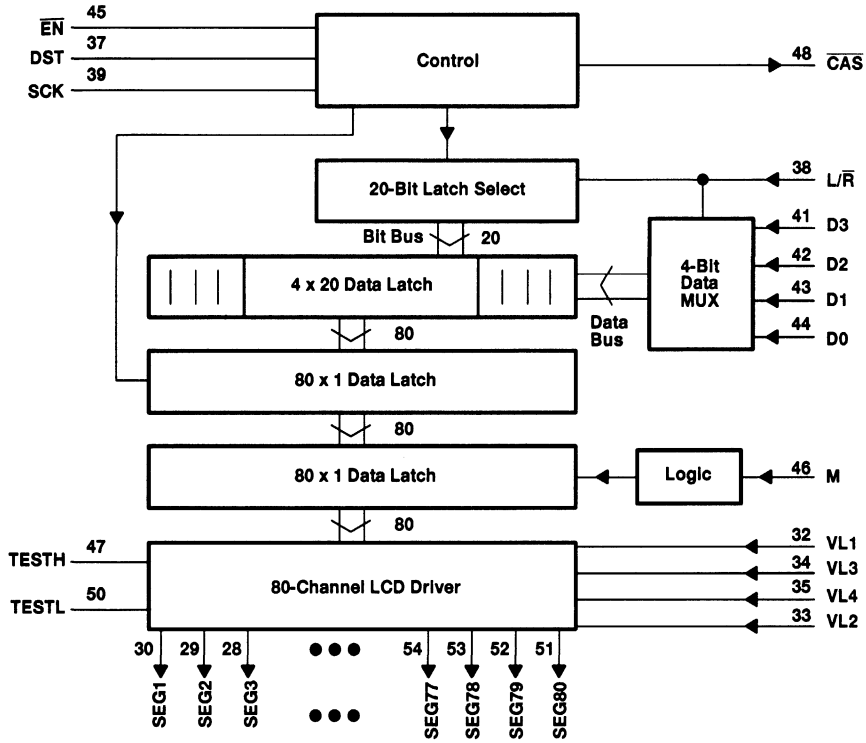
NC – No internal connection

description

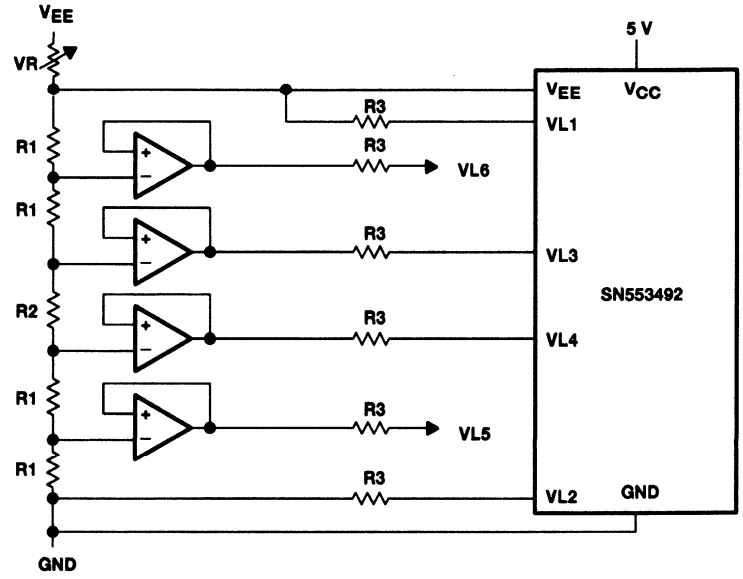
The SN553492 column driver is a monolithic silicon gate CMOS integrated circuit designed to drive the column electrodes of a liquid crystal flat panel display.

This device consists of a 4 x 20-bit data latch, an 80 x 1-bit data latch, an 80-bit level shifter, and an 80-channel output driver. Four-bit data is entered into the 4 x 20-bit data latch on the falling edge of the shift clock. $\overline{CAS}$ is used to cascade additional devices.

functional block diagram



power supply circuit



Resistors marked with same number have equal value.

Terminal Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
$\overline{CAS}$	48	O	Cascade output
D0–D3	41–44	I	Four bits of data input Data: 0 = On level of LCD; 1 = Off level of LCD
DST	37	I	Data strobe – data latched to 80 x 1 data latch and sets SEG output.
GND	36		Ground
$\overline{EN}$	45	I	Enable
L/$\overline{R}$	38	I	Select left or right shift of 4 x 20 data latch, see Table 1.
M	46	I	Frame signal Input
NC	40		No internal connection
SCK	39	I	Shift clock of 4 x 20 data latch (falling edge)
SEG 1–SEG 80	1–30, 51–100	O	Segment (column) drive signal output, see Table 2.
TESTH	47	I	Output test for on level of LCD (= V_{CC}). See Table 3 for output test levels.
TESTL	50	I	Output test for off level of LCD (= V_{CC}). See Table 3 for output test levels.
V_{CC}	49		Voltage supply
V_{EE}	31		Output bias voltage for LCD
VL1, VL2, VL3, VL4	32 – 35		Output supplies for LCD VL1 and VL2 are on level of LCD, VL3 and VL4 are off level of LCD.

Table 1. Left or Right Shift of 4 x 20 Data Latch

L/$\overline{R}$	SCK	1	2	3	4	...	19	20
GND	D3	1	5	9	13	...	73	77
	D2	2	6	10	14	...	74	78
	D1	3	7	11	15	...	75	79
	D0	4	8	12	16	...	76	80
V_{CC}	D3	80	76	72	68	...	8	4
	D2	79	75	71	67	...	7	3
	D1	78	74	70	66	...	6	2
	D0	77	73	69	65	...	5	1

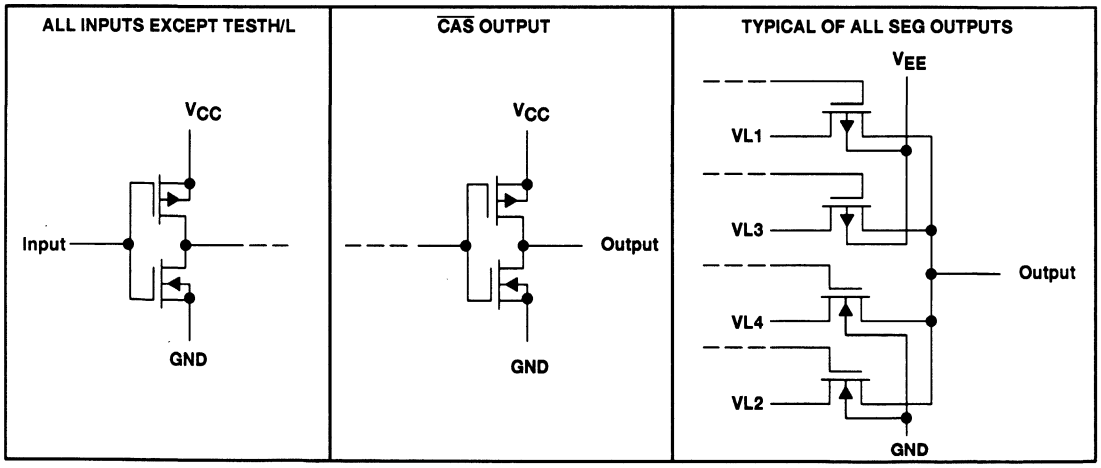
Table 2. LCD Driving Signal Level

OUTPUT LEVEL	VL1	VL2	VL3	VL4
M	1	0	1	0
Data	1	1	0	0

Table 3. On- and Off-Level LCD Tests

M	TESTH	TESTL	SEG1–SEG80
1	1	0	VL1
0	1	0	VL2
1	1	1	VL3
0	1	1	VL4
1	0	1	VL3
1	0	1	VL4

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Output bias voltage range, V_{EE}	−0.3 V to 40 V
Input voltage range at DST, SCK, M, L/$\overline{R}$, $\overline{EN}$, D0–D3, TESTH/L, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage range at $\overline{CAS}$, V_O	−0.3 V to V_{CC} + 0.3 V
Output supply voltage range, VLn for LCD (see Note 2)	−0.3 V to V_{EE} + 0.3 V
Input current, I_I	± 10 mA
Output current, I_O: $\overline{CAS}$	10 mA
SEG1 to SEG80	5 mA
Operating free-air temperature range, T_A	−55°C to 125°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to GND.
2. VLn voltage range should be under the following conditions: $V_{EE} \geq VL1 \geq VL3 \geq V_{EE} - 7$ V, and $7 \geq VL4 \geq VL2 \geq GND$.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Notes 2, 3, and 4)		4.5	5	5.5	V
Supply voltage for LCD output	V_{EE}, VL1 VL4	14		26	V
High-level input voltage, V_{IH}	DST, SCK, M, L/$\overline{R}$, D0 to D3, $\overline{EN}$, TESTH, TESTL	0.8 V_{CC}		V_{CC}	V
Low-level input voltage, V_{IL}	DST, SCK, M, L/$\overline{R}$, D0 to D3, $\overline{EN}$, TESTH, TESTL	V_{SS}		0.2 V_{CC}	V
Clock frequency, f_{clock}	SCK			6	MHz
Operating free-air temperature, T_A		–55		125	°C
Clock cycle time, $t_{c(SCK)}$	SCK	166			ns
Clock cycle time, $t_{c(DST)}$	DST	t_{SCK}x20			
Pulse duration, clock high, $t_{w(SCKH)}$	At SCK	83			ns
Pulse duration, clock low, $t_{w(SCKL)}$	At SCK	83			ns
Pulse duration, clock high, $t_{w(SCKH)}$	At DST	70		t_{SCK}x19	µs
Setup time, data strobe, DST low before SCK, $t_{su(DST)}$		80			ns
Hold time, data strobe, SCK low before DST, $t_{h(DST)}$		30			ns
Setup time, Dn high or low, t_{su}		30			ns
Hold time, Dn high or low, t_h		30			ns
Enable time, t_{en}	SCK – $\overline{EN}$	50			ns
Disable time, t_{dis}	$\overline{EN}$ – SCK	50			ns

NOTES: 2. VLn voltage range should be under the following conditions: $V_{EE} \geq VL1 \geq VL3 \geq V_{EE} - 7$ V, and $7 \geq VL4 \geq VL2 \geq GND$.

3. Turn on and off sequence of power must be as follows:
   Turn on sequence: V_{CC} → Input → V_{EE}
   Turn off sequence: V_{EE} → Input → V_{CC}.

4. VLn voltage range should be within ΔV (see Figure 1).

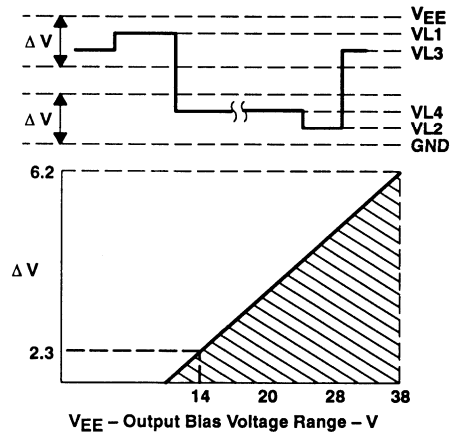


Figure 1

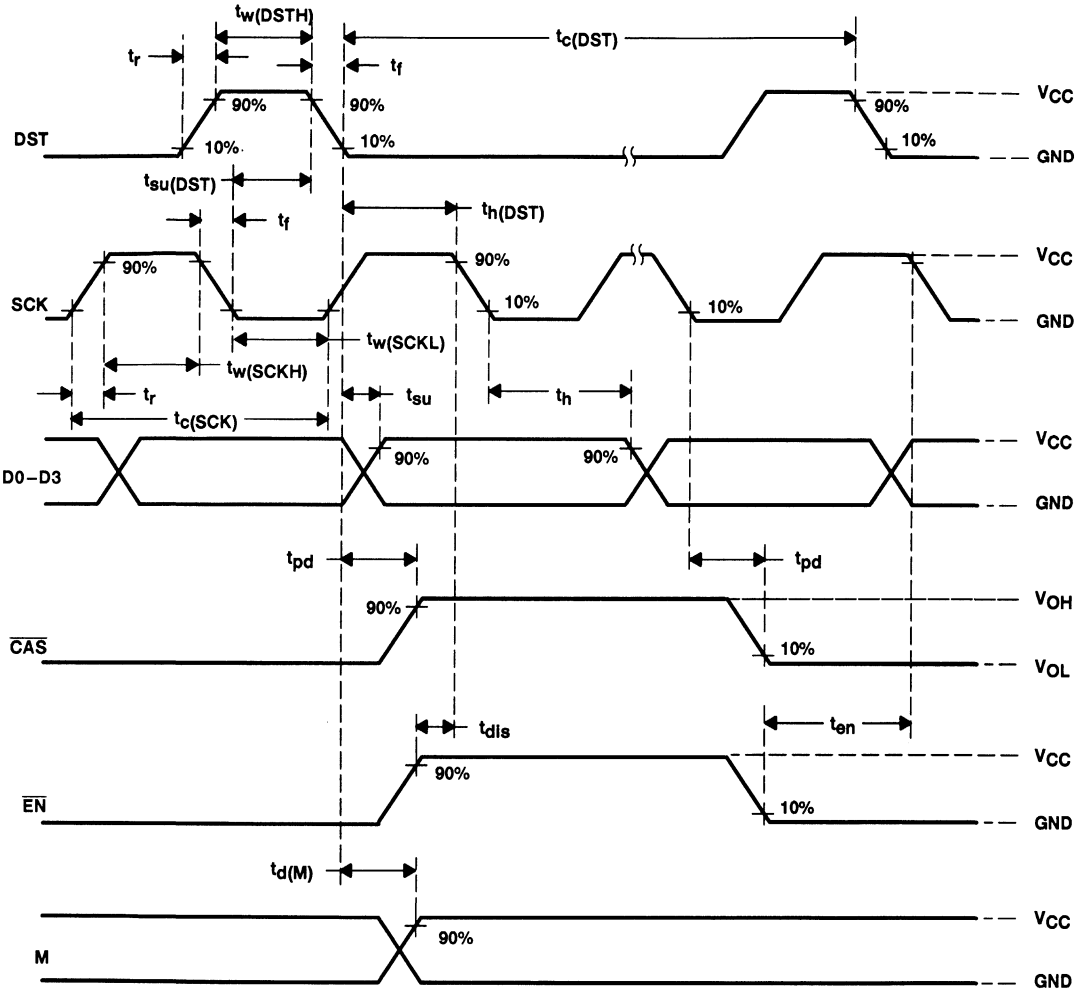
electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	$\overline{CAS}$	I_{OH} = −0.4 mA	V_{CC} −0.4			V
V_{OL}	Low-level output voltage	$\overline{CAS}$	I_{OL} = 0.4 mA			0.4	V
I_{IH}	High-level input current	DST, SCK, M, L/$\overline{R}$, $\overline{EN}$, D0 to D3	V_{CC} = MAX, V_I = V_{CC}			5	μA
		TESTH, TESTL				500	μA
I_{IL}	Low-level input current	DST, SCK, M, L/$\overline{R}$, $\overline{EN}$, D0 to D3	V_{CC} = MAX, V_I = GND			−5	μA
		TESTH, TESTL				−5	μA
Z_O	Output impedance	SEG1 to SEG80	I_O = 100 μA		2	4	kΩ
I_I	Input current	VLn	V_I = V_{EE}, GND			±50	μA
I_{CC}	Supply current	V_{CC}	See Note 5			3	mA
I_{EE}	Supply current	V_{EE}	See Note 5			2.5	mA
$I_{I(standby)}$	Input standby current	V_{CC}	See Note 6			200	μA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C, V_{CC} = 5 V.
NOTES: 5. Test conditions are at f_{DST} = V_{CC} = MAX, V_{EE} = MAX, V_I = V_{CC}, GND. Outputs are not loaded.
6. Test condition of standby current is added at $\overline{EN}$ input = V_{CC}.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	Propagation delay time	DST	CAS, SCK–$\overline{CAS}$	C_L = 30 pF		3	ns
t_d	Frame sync delay time		M			300	ns

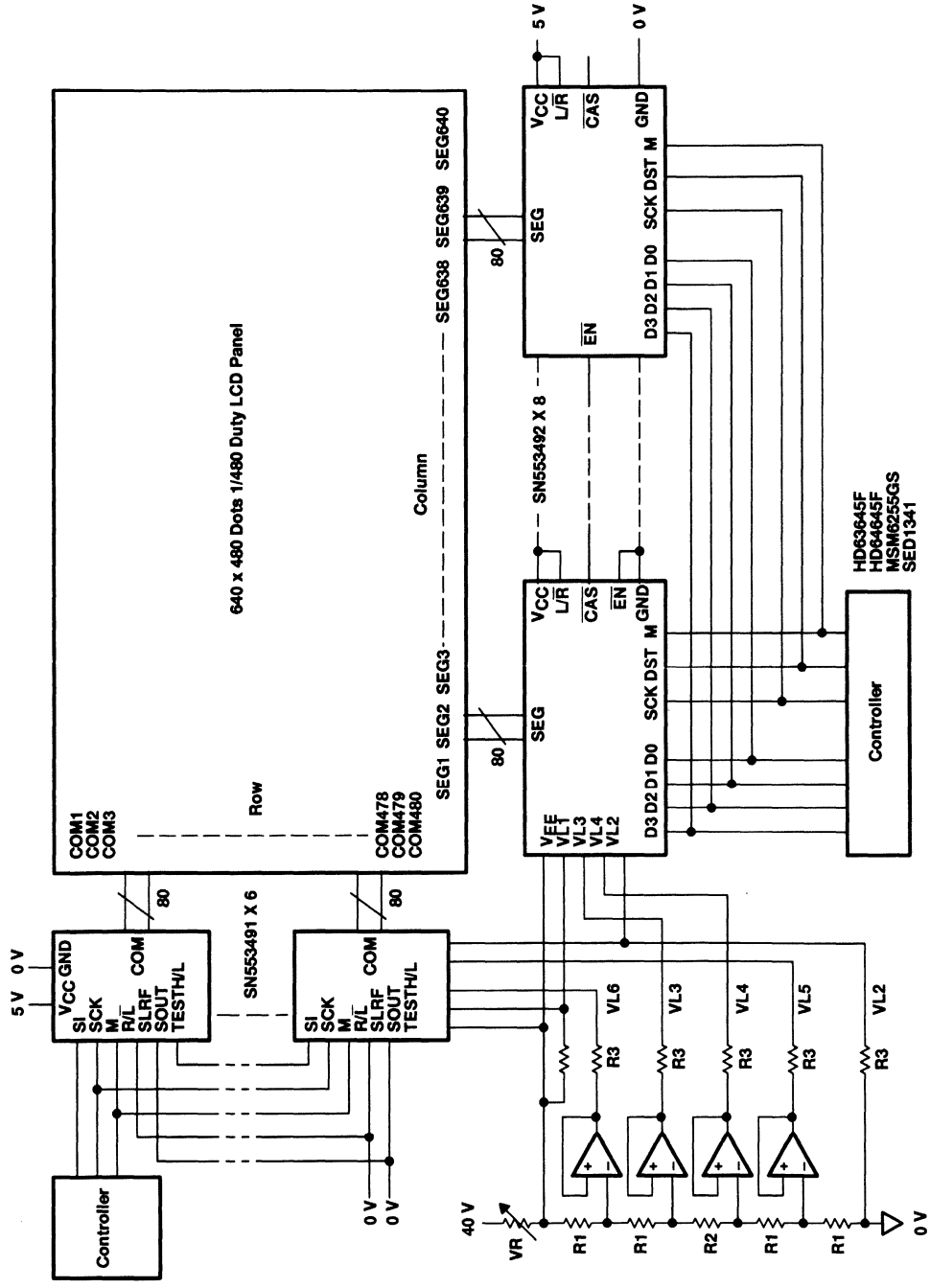


NOTE: $t_r \leq 30$ ns, $t_f \leq 30$ ns.

Figure 2. Timing Diagram

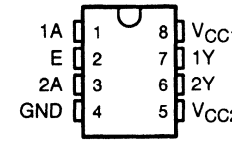
APPLICATION INFORMATION

application circuit



- **Dual Circuits Capable of Driving High-Capacitance Loads at High Speeds**
- **Output Supply Voltage Range up to 24 V**
- **Low Standby Power Dissipation**

D OR P PACKAGE
(TOP VIEW)

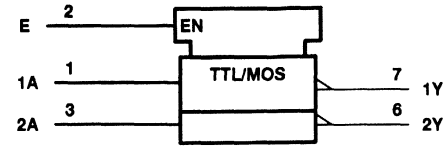


description

The SN75372 is a dual NAND gate interface circuit designed to drive power MOSFETs from TTL inputs. It provides high current and voltage levels necessary to drive large capacitive loads at high speeds. The device operates from a V_{CC1} of 5 V and a V_{CC2} of up to 24 V.

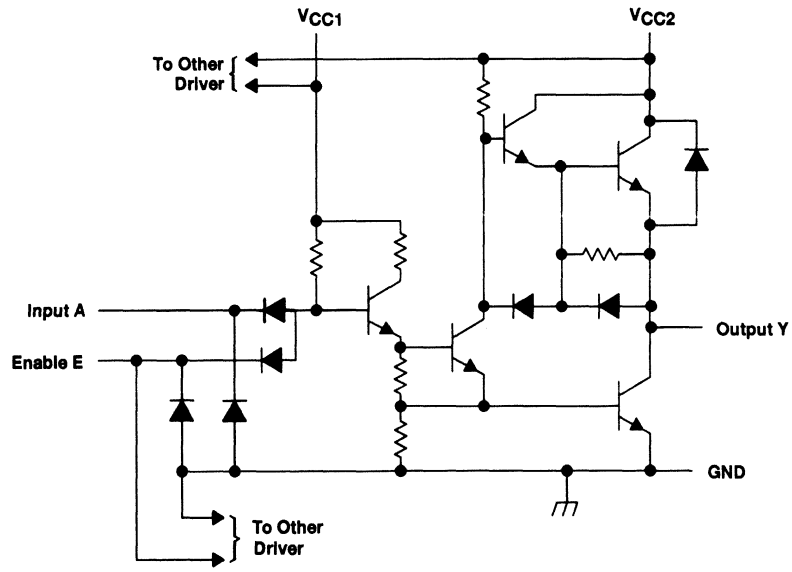
The SN75372 is characterized for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC1} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range, V_{CC2} ..... −0.5 V to 25 V
Input voltage ..... 5.5 V
Peak output current, (t_w < 10 ms, duty cycle < 50%) ..... 500 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−10	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

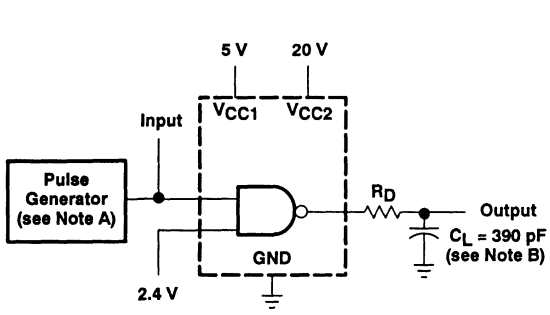
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -12$ mA				−1.5	V
V_{OH}	High-level output voltage		$V_{IL} = 0.8$ V,	$I_{OH} = -50$ μA	$V_{CC2}-1.3$	$V_{CC2}-0.8$		V
			$V_{IL} = 0.8$ V,	$I_{OH} = -10$ mA	$V_{CC2}-2.5$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage		$V_{IH} = 2$ V,	$I_{OL} = 10$ mA		0.15	0.3	V
			$V_{CC2} = 15$ V to 24 V, $I_{OL} = 40$ mA	$V_{IH} = 2$ V,		0.25	0.5	
V_F	Output clamp-diode forward voltage		$V_I = 0$,	$I_F = 20$ mA			1.5	V
I_I	Input current at maximum input voltage		$V_I = 5.5$ V				1	mA
I_{IH}	High-level input current	Any A	$V_I = 2.4$ V				40	μA
		Any E					80	
I_{IL}	Low-level input current	Any A	$V_I = 0.4$ V			−1	−1.6	mA
		Any E				−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high		$V_{CC1} = 5.25$ V, All inputs at 0 V,	$V_{CC2} = 24$ V, No load		2	4	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high						0.5	mA
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low		$V_{CC1} = 5.25$ V, All inputs at 5 V,	$V_{CC2} = 24$ V, No load		16	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low					7	13	mA
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition		$V_{CC1} = 0$, All inputs at 5 V,	$V_{CC2} = 24$ V, No load			0.5	mA

† All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, and $T_A = 25°C$.

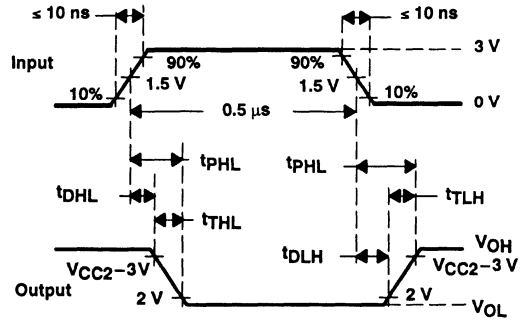
switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 20$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	$C_L = 390$ pF, $R_D = 10\ \Omega$, See Figure 1		20	35	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{TLH}	Transition time, low-to-high-level output			20	30	ns
t_{THL}	Transition time, high-to-low-level output			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	50	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_O ~ 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Each Driver

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

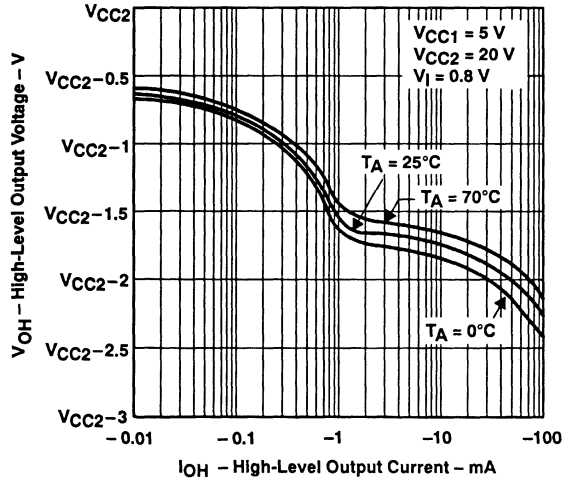


Figure 2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

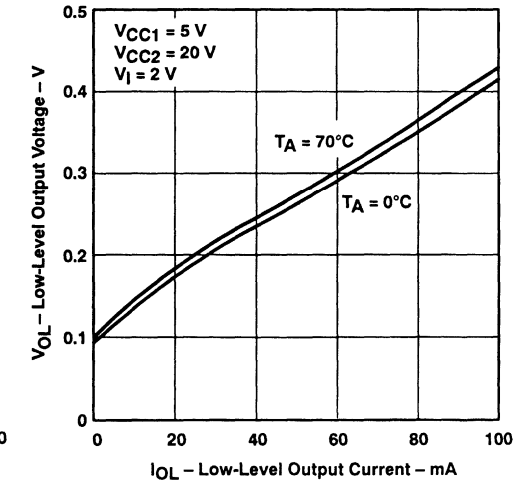


Figure 3

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

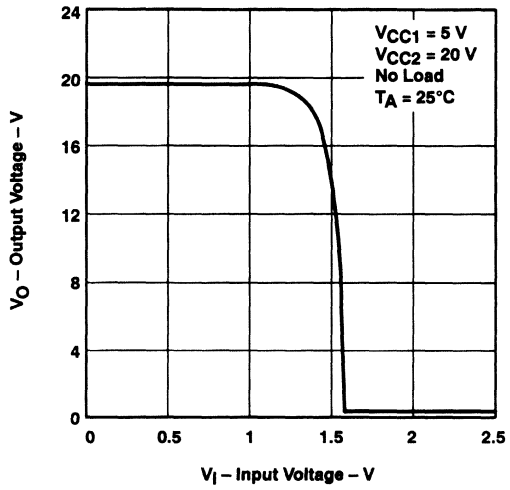


Figure 4

POWER DISSIPATION (BOTH DRIVERS)
vs
FREQUENCY

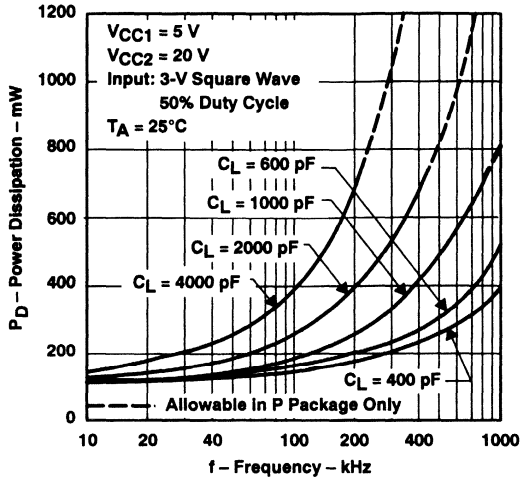


Figure 5

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

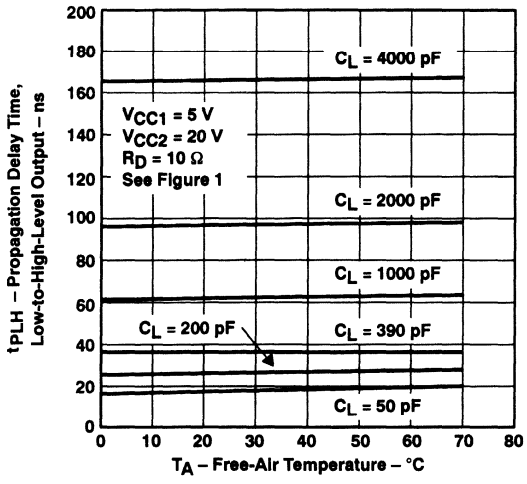


Figure 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

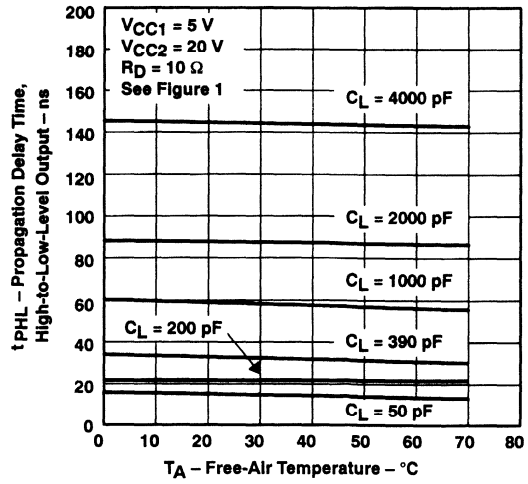


Figure 7

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

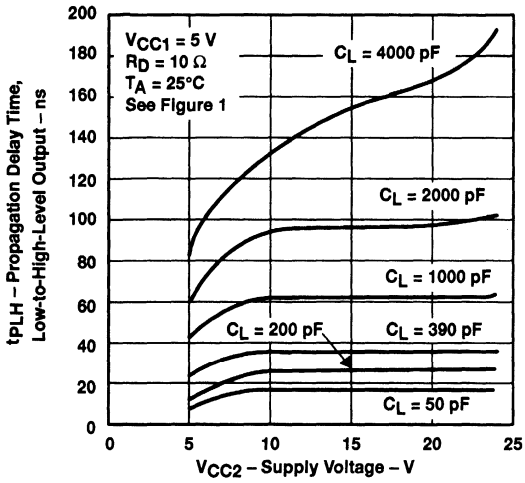


Figure 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

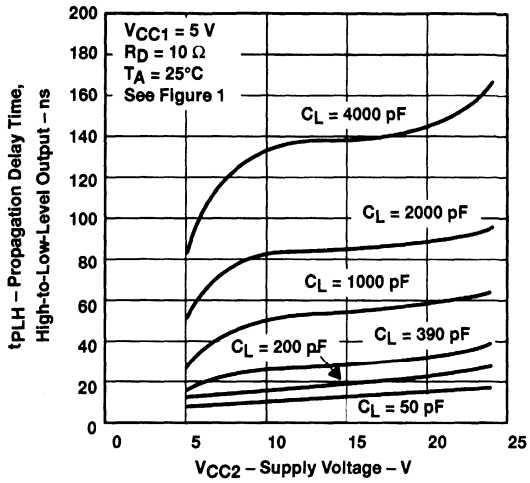


Figure 9

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

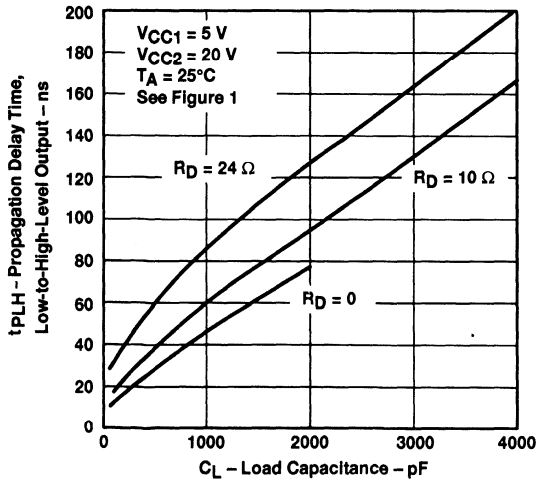


Figure 10

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

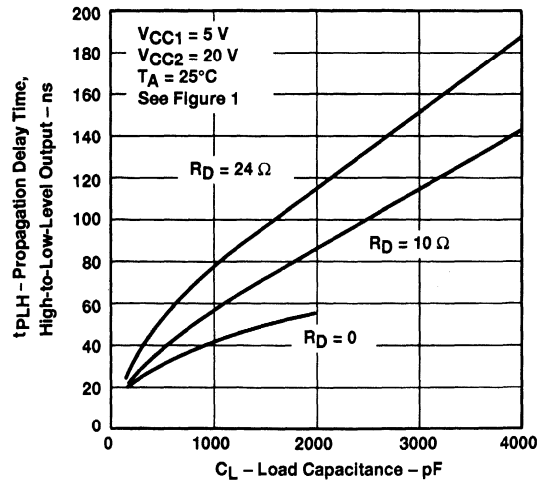


Figure 11

NOTE: For R_D = 0, operation with C_L > 2000 pF violates absolute maximum current rating.

APPLICATION INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pullup resistor is not satisfactory for high-speed applications. In Figure 12(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470-Ω pullup resistor. The input capacitance (C_{iss}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the combination of C_{iss} and the pullup resistor is shown in Figure 12(b).

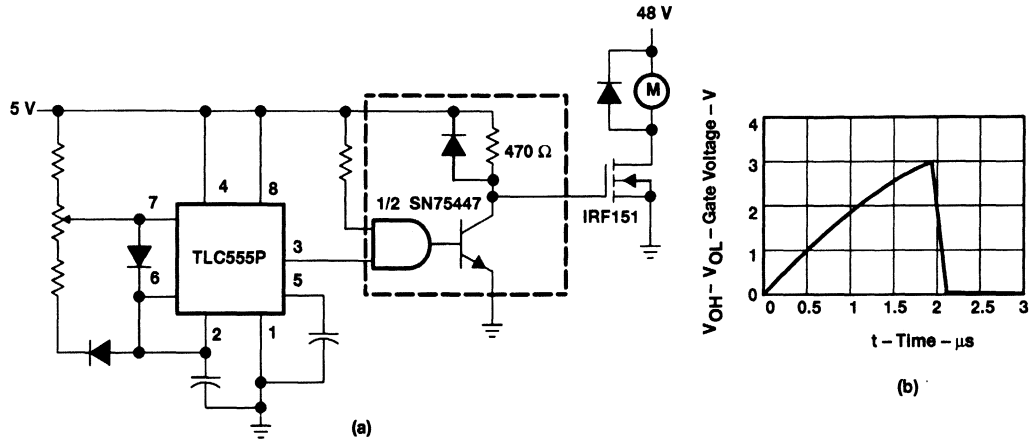


Figure 12. Power MOSFET Drive Using SN75447

APPLICATION INFORMATION

A faster, more efficient drive circuit uses an active pullup as well as an active pulldown output configuration, referred to as a totem-pole output. The SN75372 driver provides the high speed, totem-pole drive desired in an application of this type, see Figure 13(a). The resulting faster switching speeds are shown in Figure 13(b).

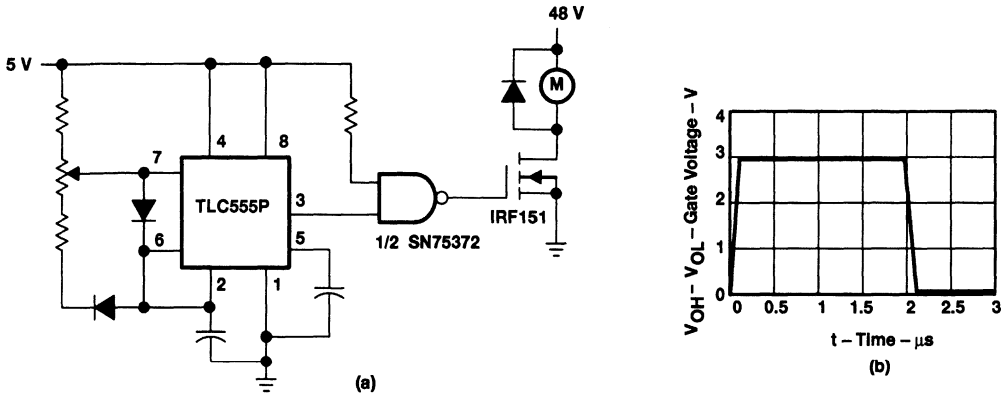


Figure 13. Power MOSFET Drive Using SN75372

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{pk} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired drive time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 13(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 13(a) is

$$I_{PK} = \frac{(3 - 0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V, and assuming worst-cast conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, the SN75374 quad MOSFET driver should be used.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75372 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical SN75372 as a function of load capacitance and frequency. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} = P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load, and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_H t_H + P_L t_L}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in Figure 14.

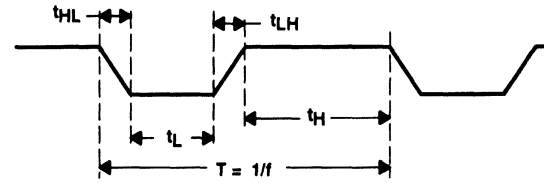


Figure 14. Output Voltage Waveform

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

THERMAL INFORMATION

power dissipation precautions (continued)

In the following power calculation, both channels are operating under identical conditions:
V_{OH} =19.2 V and V_{OL} = 0.15 V with V_{CC1} = 5 V, V_{CC2} = 20 V, V_C = 19.05 V, C = 1000 pF, and the duty cycle = 60%. At 0.5 MHz, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is high, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values,

$$P_{DC(AV)} = \left[(5\ V)\left(\frac{2\ mA}{2}\right) + (20\ V)\left(\frac{0\ mA}{2}\right)\right](0.6) + \left[(5\ V)\left(\frac{16\ mA}{2}\right) + (20\ V)\left(\frac{7\ mA}{2}\right)\right](0.4)$$

$P_{DC(AV)}$ = 47 mW per channel

Power during the charging time of the load capacitance is

$P_{C(AV)}$ = (1000 pF) (19.05 V)^2 (0.5 MHz) = 182 mW per channel

Total power for each driver is

$P_{T(AV)}$ = 47 mW + 182 mW = 229 mW

and total package power is

$P_{T(AV)}$ = (229) (2) = 458 mW.

SLLS025 – D3004, SEPTEMBER 1986

- **Quadruple Circuits Capable of Driving High-Capacitance Loads at High Speeds**
- **Output Supply Voltage Range From 5 V to 24 V**
- **Low Standby Power Dissipation**
- **V_{CC3} Supply Maximizes Output Source Voltage**

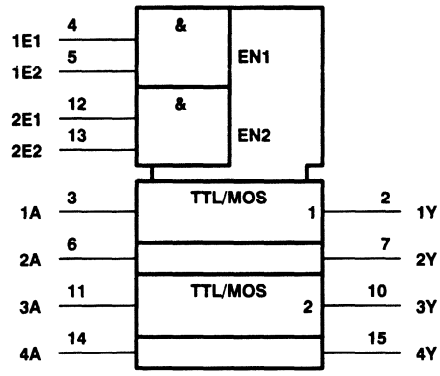
description

The SN75374 is a quadruple NAND interface circuit designed to drive power MOSFETs from TTL inputs. It provides the high current and voltage necessary to drive large capacitive loads at high speeds.

The outputs can be switched very close to the V_{CC2} supply rail when V_{CC3} is about 3 V higher than V_{CC2}. V_{CC3} can also be tied directly to V_{CC2} when the source voltage requirements are lower.

The SN75374 is characterized for operation from 0°C to 70°C.

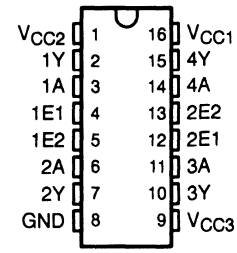
logic symbol†



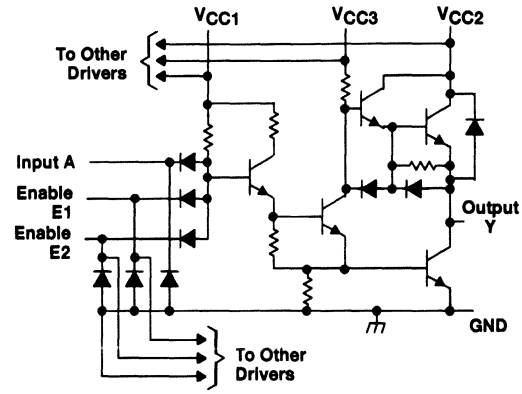
(7–48)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

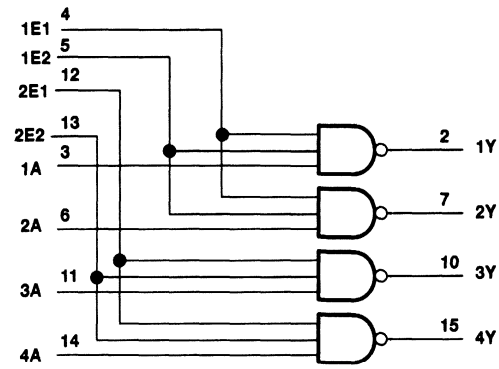
D OR N PACKAGE
(TOP VIEW)



schematic (each driver)



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) ..... −0.5 V to 7 V
Supply voltage range of V_{CC2} ..... −0.5 V to 25 V
Supply voltage range of V_{CC3} ..... −0.5 V to 30 V
Input voltage ..... 5.5 V
Peak output current (t_w < 10 ms, duty cycle < 50%) ..... 500 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Supply voltage, V_{CC3}	V_{CC2}	24	28	V
Voltage difference between supply voltages: $V_{CC3} - V_{CC2}$	0	4	10	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−10	mA
High-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, and operating free-air temperature (unless otherwise noted)

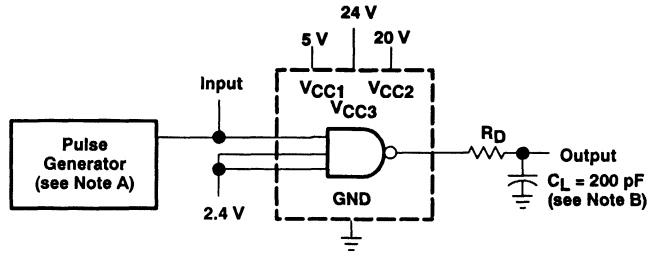
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA					−1.5	V
V_{OH}	High-level output voltage		V_{CC3} = V_{CC2} + 3 V,	V_{IL} = 0.8 V,	I_{OH} = −100 µA	V_{CC2}−0.3	V_{CC2}−0.1		V
			V_{CC3} = V_{CC2} + 3 V,	V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2}−1.3	V_{CC2}−0.9		
			V_{CC3} = V_{CC2},	V_{IL} = 0.8 V,	I_{OH} = −50 µA	V_{CC2}−1	V_{CC2}−0.7		
			V_{CC3} = V_{CC2},	V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2}−2.5	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		V_{IH} = 2 V,	I_{OL} = 10 mA			0.15	0.3	V
			V_{CC2} = 15 V to 28 V,	V_{IH} = 2 V,	I_{OL} = 40 mA		0.25	0.5	
V_F	Output clamp-diode forward voltage		V_I = 0,	I_F = 20 mA				1.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V					1	mA
I_{IH}	High-level input current	Any A	V_I = 2.4 V					40	µA
		Any E						80	
I_{IL}	low-level input current	Any A	V_I = 0.4 V				−1	−1.6	mA
		Any E					−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high		V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 24 V, No load	V_{CC3} = 28 V,		4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high						−2.2	0.25	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high						2.2	3.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low		V_{CC1} = 5.25 V, All inputs at 5 V,	V_{CC2} = 24 V, No load	V_{CC3} = 28 V,		31	47	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, all outputs low							2	
$I_{CC3(L)}$	Supply current from V_{CC1}, all outputs low						16	27	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high		V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 24 V, No load	V_{CC3} = 24 V,			0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high							0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition		V_{CC1} = 0, All inputs at 0 V,	V_{CC2} = 24 V, No load	V_{CC3} = 24 V,			0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition							0.5	

† All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, and T_A = 25°C except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

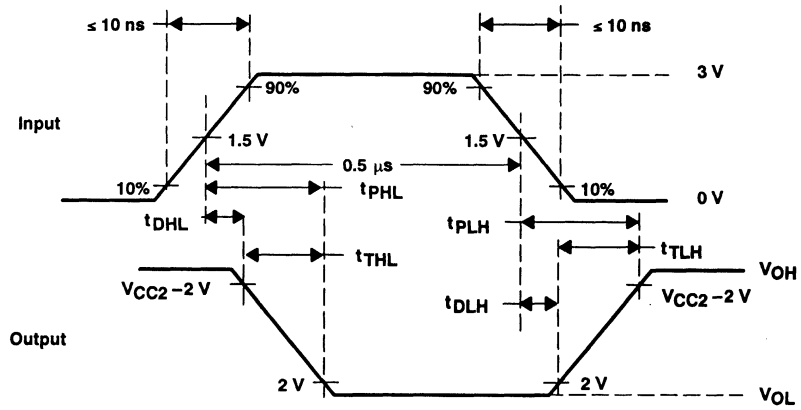
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 200 pF, R_D = 24 Ω, See Figure 1		20	30	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	50	ns
t_{TLH}	Transition time, low-to-high-level output			20	30	ns
t_{THL}	Transition time, high-to-low-level output			20	30	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 1. Test Circuit and Voltage Waveforms, Each Driver

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_O \sim 50\ \Omega$.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

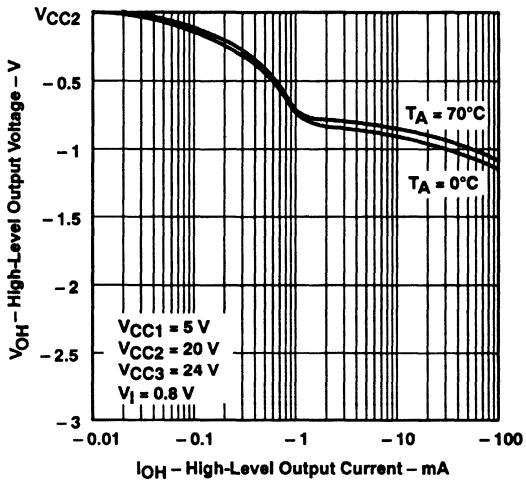


Figure 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

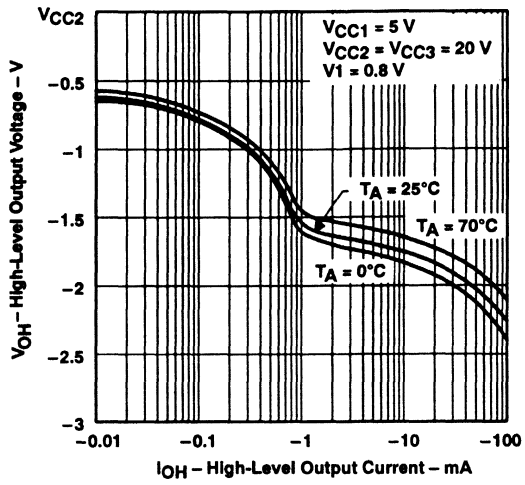


Figure 3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

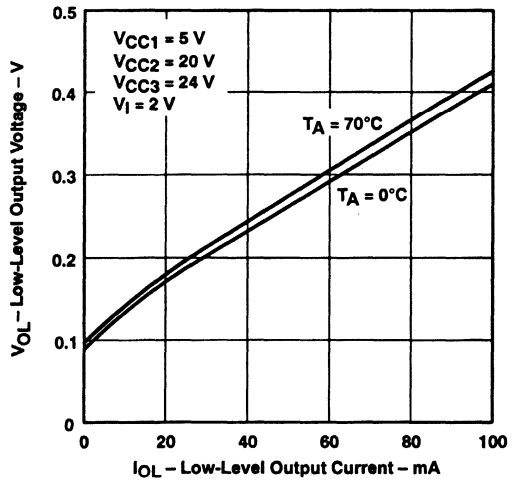


Figure 4

VOLTAGE TRANSFER CHARACTERISTICS

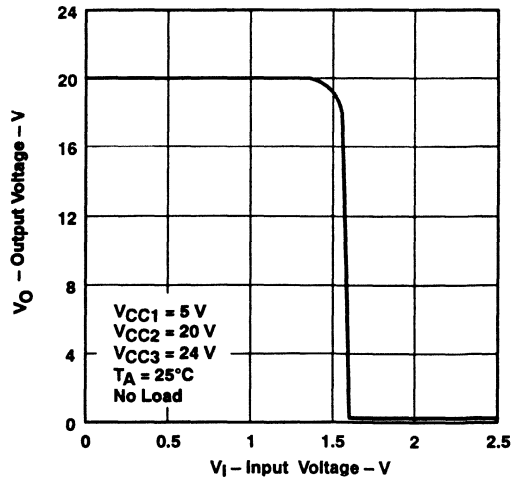


Figure 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

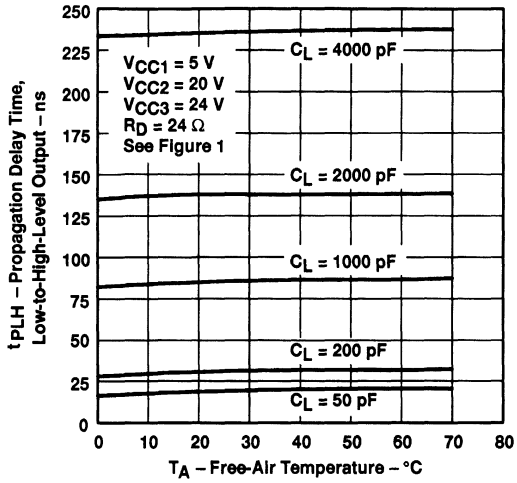


Figure 6

PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

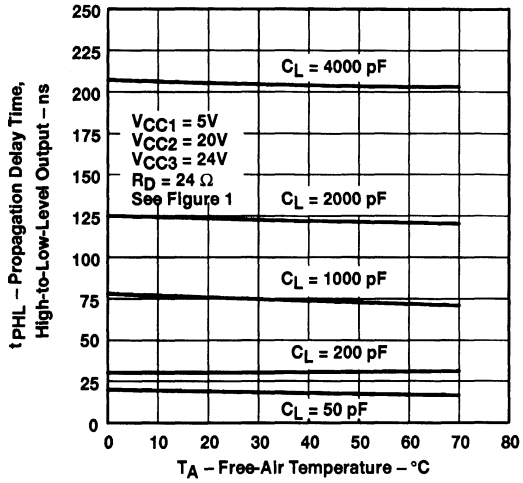


Figure 7

PROPAGATION DELAY TIME
LOW-TO-HIIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

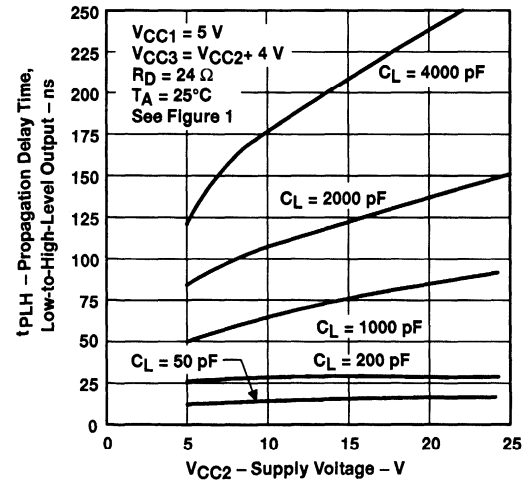


Figure 8

PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

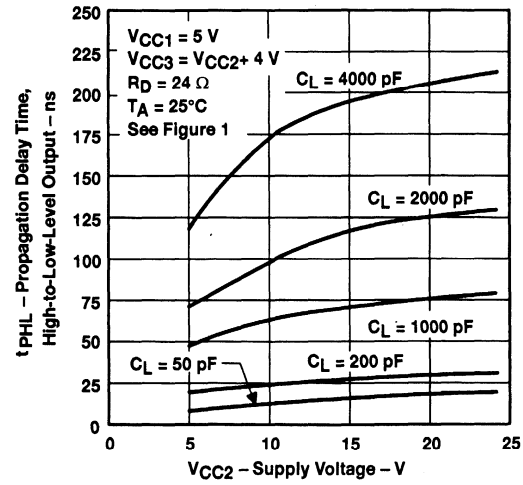


Figure 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

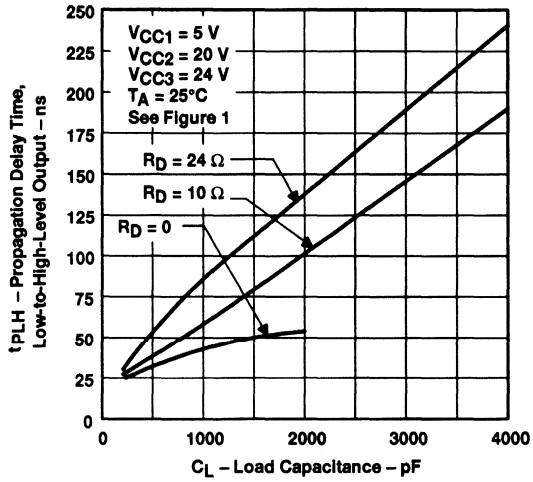


Figure 10

PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

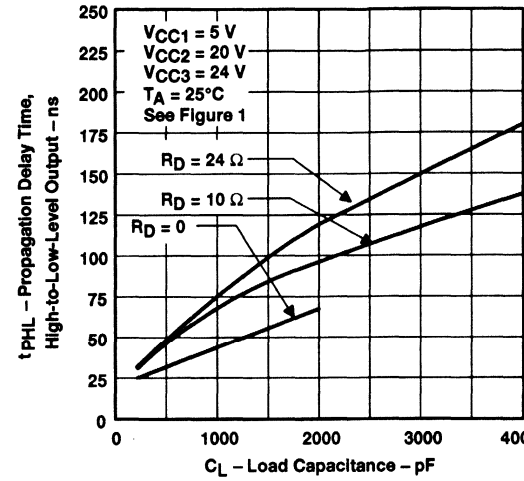


Figure 11

POWER DISSIPATION (ALL DRIVERS)
vs
FREQUENCY

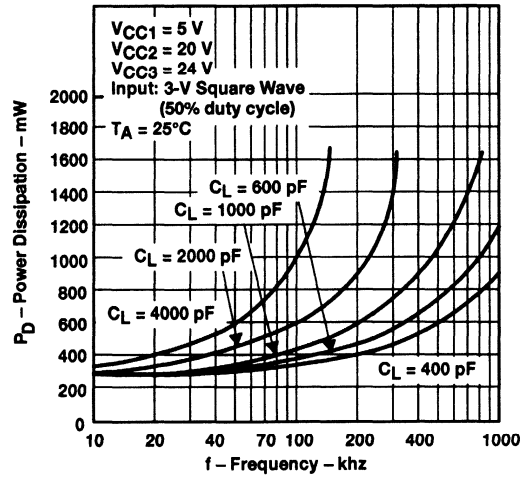


Figure 12

NOTE: For R_D = 0, operation with C_L > 2000 pF violates absolute maximum current rating.

APPLICATION INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pullup resistor is not satisfactory for high-speed applications. In Figure 13(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470-Ω pullup resistor. The input capacitance (C_{ISS}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the product of input capacitance and the pullup resistor is shown in Figure 13(b).

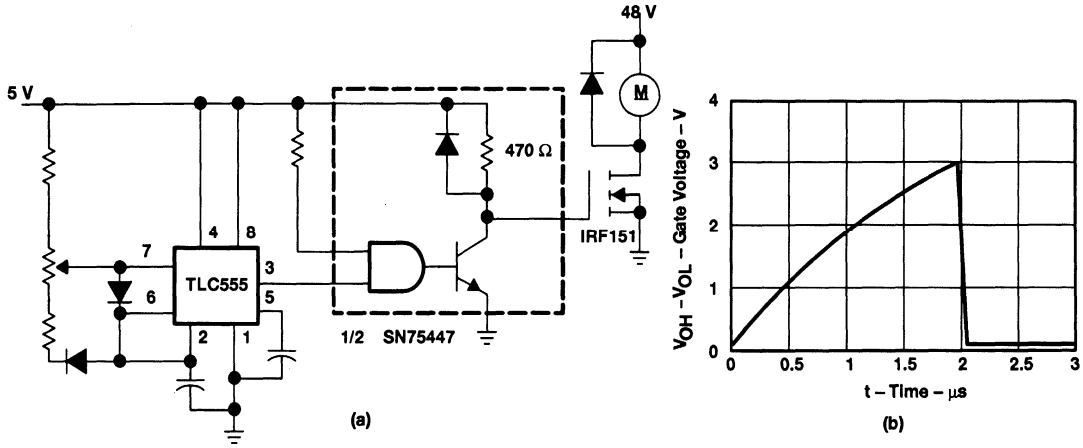


Figure 13. Power MOSFET Drive Using SN75447

A faster, more efficient drive circuit uses an active pull-up as well as an active pull-down output configuration, referred to as a totem-pole output. The SN75374 driver provides the high-speed totem-pole drive desired in an application of this type, see Figure 14(a). The resulting faster switching speeds are shown in Figure 14(b).

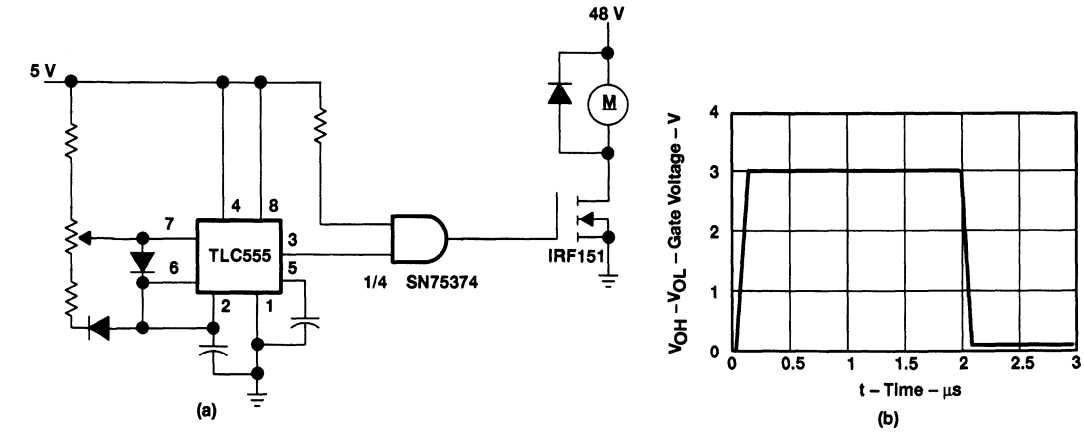


Figure 14. Power MOSFET Drive Using SN75374

APPLICATION INFORMATION

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{PK} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 14(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 14(a) is

$$I_{PK} = \frac{(3 - 0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V and assuming worst-case conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, V_{CC3} should be at least 3 V higher than V_{CC2}.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75374 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 12 shows the power dissipated in a typical SN75374 as a function of frequency and load capacitance. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_H t_H + P_L t_L}{T}$$

$$P_{C(AV)} \approx C V_c^2 f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

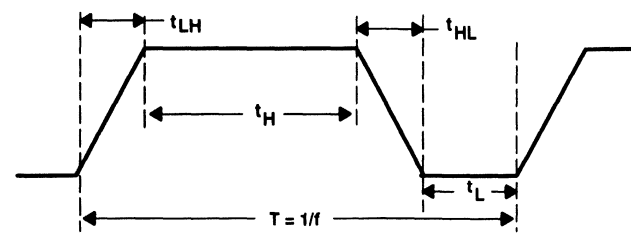


Figure 15. Output Voltage Waveform

where the times are as defined in Figure 15.

THERMAL INFORMATION

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

In the following power calculation, all four channels are operating under identical conditions: f = 0.2 MHz, V_{OH} = 19.9 V and V_{OL} = 0.15 V with V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, V_C = 19.75 V, C = 1000 pF, and the duty cycle = 60%. At 0.2 MHz for C_L < 2000 pF, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is low, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values,

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{4\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{-2.2\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) +$$

$$\left[(5\text{ V})\left(\frac{31\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{0\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58.2 mW per channel

Power during the charging time of the load capacitance is

$P_{C(AV)} = (1000\text{ pF})\ (19.75\text{ V})^2\ (0.2\text{ MHz})$ = 78 mW per channel

Total power for each driver is

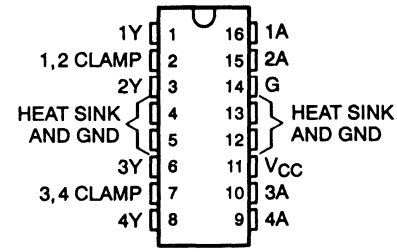
$P_{T(AV)}$ = 58.2 mW + 78 mW = 136.2 mW

The total package power is

$P_{T(AV)} = (136.2)\ (4)$ = 544.8 mW

- **Saturating Outputs With Low On-State Resistance**
- **Very Low Standby Power . . . 53 mW Max**
- **High-Impedance MOS- or TTL-Compatible Inputs**
- **Standard 5-V Supply Voltage**
- **No Power-Up or Power-Down Output Glitch**
- **Output Clamp Diodes for Transient Suppression**
- **2-W Power Package . . . 60°C/W $R_{\theta JA}$**
- **600-mA Output Current**
- **35-V Switching Voltage**

NE PACKAGE
(TOP VIEW)



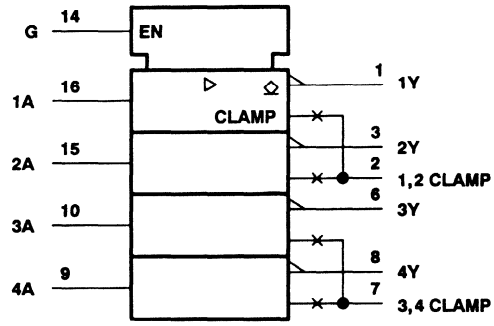
description

The SN75435 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. It features four inverting open-collector drivers with a common enable input that, when taken low, disables all four outputs. Each driver is protected against load shorts with its own latching overcurrent shutdown circuitry, which turns the output off when a load short is detected. A short on one load does not affect operation of the other three drivers. The latch for the shutdown holds the output off until the input or enable pin is taken low and then high again. A delay circuit is incorporated in the overcurrent shutdown to allow load capacitance of up to 5 nF at 35 V.

Applications include relay drivers, lamp drivers, solenoid drivers, motor drivers, LED drivers, line drivers, logic buffers, hammer drivers, and memory drivers.

The SN75435 is characterized for operation from 0°C to 70°C.

logic symbol†



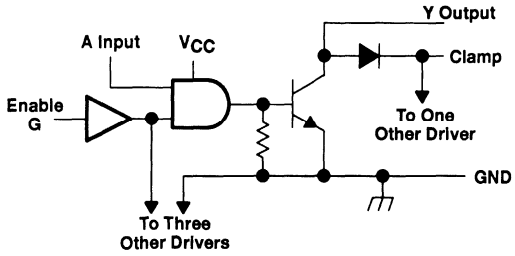
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

FUNCTION TABLE
(each NAND driver)

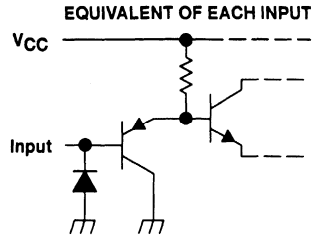
INPUTS		OUTPUT
A	G	Y
L	X	H
X	L	H
H	H	L

H = high level, L = low level
X = irrelevant

logic diagram (positive logic)



schematic of inputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Output supply voltage ..... 70 V
Output diode-clamp current ..... 1 A
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 2075 mW
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Output voltage			35	V
Output current			600	mA
Load capacitance (see Figure 3)			35	nF
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range

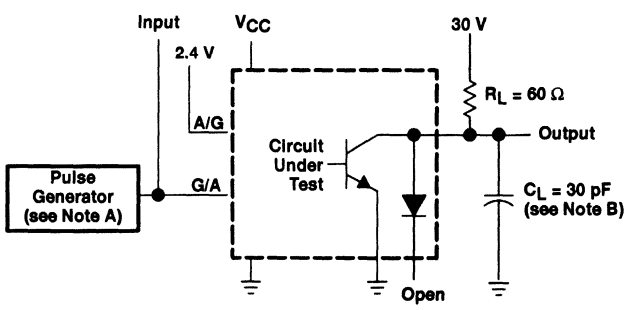
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA		−0.9	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V	I_{OL} = 300 mA		0.25	0.5	V
			I_{OL} = 600 mA		0.55	1	
V_R	Output clamp-diode reverse voltage	V_{CC} = 4.75 V,	I_R = 100 µA	70	100		V
V_F	Output clamp-diode forward voltage	I_F = 600 mA			1.2	1.6	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V			100	µA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.25 V		0.01	10	µA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.8 V		−0.5	−10	µA
	Overcurrent shutdown current	V_{CC} = 4.75 to 5.25 V		650	850		mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 0		6	10	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 5 V		55	75	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

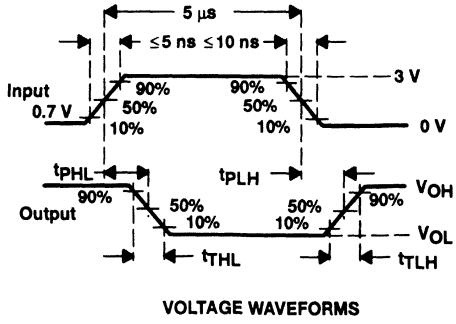
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 60 Ω, See Figure 1		750		ns
t_{PHL}	Propagation delay time, high-to-low-level output			750		ns
t_{TLH}	Transition time, low-to-high-level output			200		ns
t_{THL}	Transition time, high-to-low-level output			200		ns
V_{OH}	High-level output voltage after switching	See Figure 2	V_S−10			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

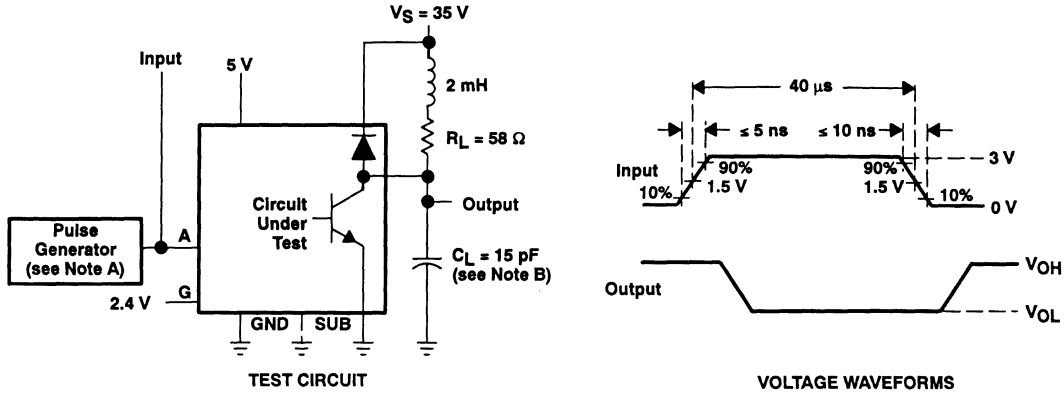


VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L include probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms

RECOMMENDED OPERATING CONDITIONS

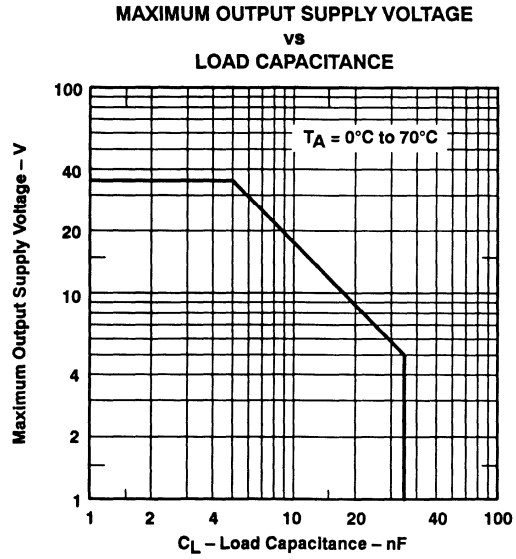


Figure 3

APPLICATION INFORMATION

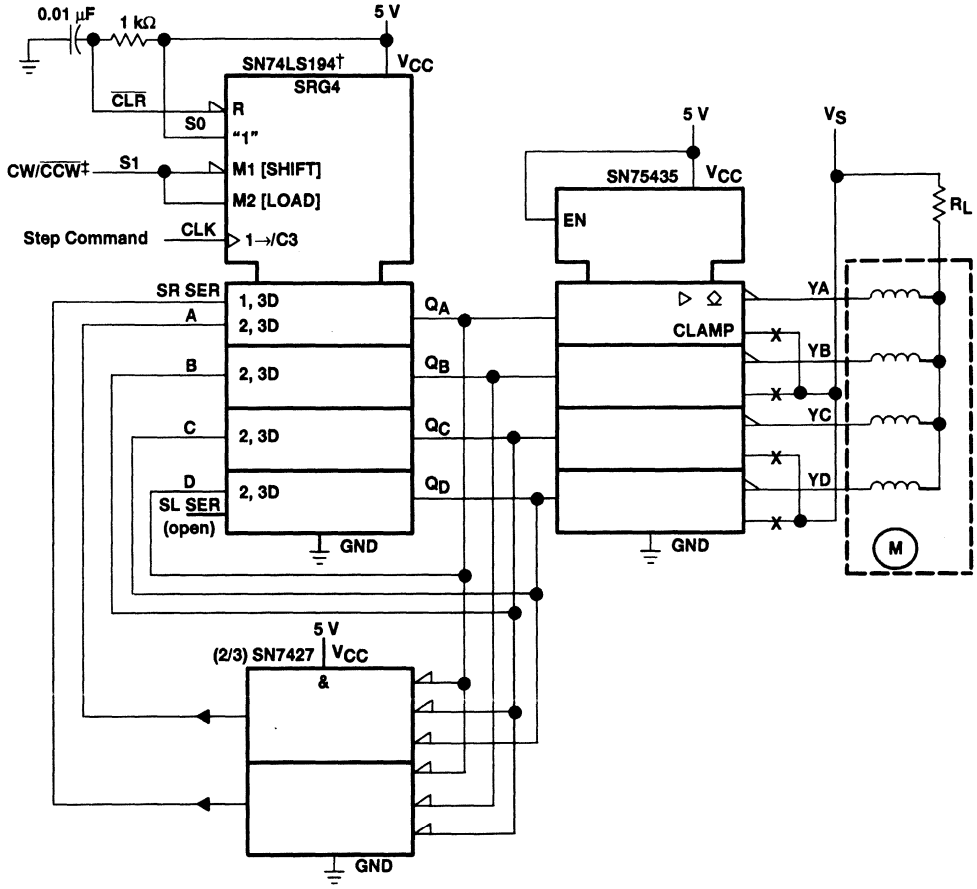


Figure 4. Four-Winding Stepper-Motor Control Circuit

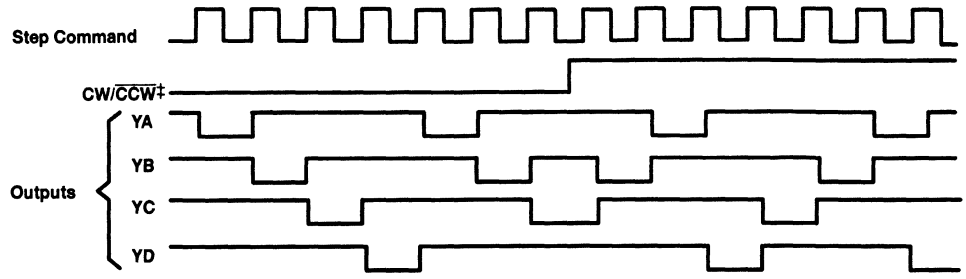
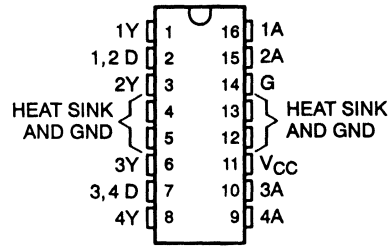


Figure 5. Timing Diagram for Motor Control Circuit

† The SN74LS194 is a universal shift register with both shift-right and shift-left capability. In this application, S0 is wired high, and only the shift-right and parallel-load modes are utilized. The logic symbol shown above has been simplified to show only the utilized modes.
‡ This signal is CW/$\overline{\text{CCW}}$ or $\overline{\text{CW}}$/CCW depending on motor winding.

- **Saturating Outputs With Low On-State Resistance**
- **High-Impedance Inputs Compatible With CMOS, MOS, and TTL Levels**
- **Very Low Standby Power . . . 21 mW Max**
- **High-Voltage Outputs . . . 70 V Min**
- **No Power-Up or Power-Down Output Glitch**
- **No Latch-Up Within Recommended Operating Conditions**
- **Output Clamp Diodes for Transient Suppression**
- **2-W Power Package**

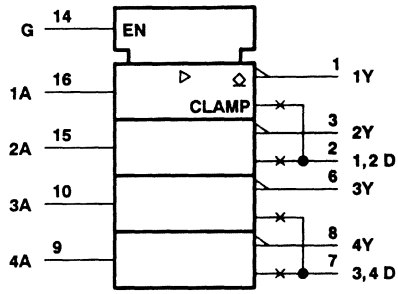
NE PACKAGE
(TOP VIEW)



description

The SN75436, SN75437A, and SN75438 quadruple peripheral drivers are designed for use in systems requiring high current, high voltage, and high load power. Each device features four inverting open-collector outputs with a common enable input that, when taken low, disables all four outputs. The envelope of 1-V characteristics exceeds the specifications sufficiently to avoid high-current latch-up. Applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand devices.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

FUNCTION TABLE
(each NAND driver)

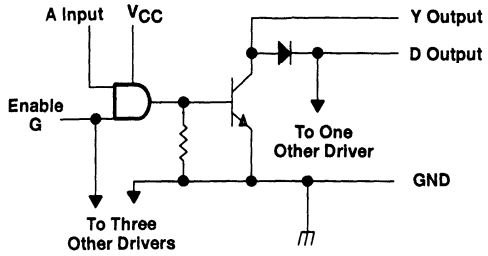
INPUTS		OUTPUT
A	G	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

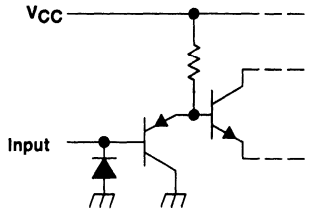
SELECTION GUIDE

FEATURE	SN75436	SN75437A	SN75438	UNIT
Maximum recommended output current	0.5	0.5	1	A
Maximum V_{OL} at maximum I_{OL}	0.5	0.5	1	V
Maximum recommended output supply voltage in an inductive switching circuit, V_S	50	35	35	V

logic diagram (positive logic, each driver)



equivalent schematic of each input



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} ..... 7 V
Input voltage, V_I ..... 30 V
Output current: SN75436, SN75437A (see Note 1) ..... 0.75 A
SN75438 ..... 1.25 A
Output clamp-diode current, I_{OK} ..... 1.25 A
Output voltage (off-state) ..... 70 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 2075 mW
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds ..... 260°C

NOTES: 1. All four sections of these circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
2. For operation above 25°C free-air temperature, derate linearly to 1328 mW at 70°C at the rate of 16.6 mW/°C.

recommended operating conditions

PARAMETER	SN75436			SN75437A			SN75438			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			2			V
Low-level input voltage, V_{IL}			0.8			0.8			0.8	V
Output supply voltage in inductive switching circuit (see Figure 2), V_S			50			35			35	V
Output current, I_O			0.5			0.5			1	A
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

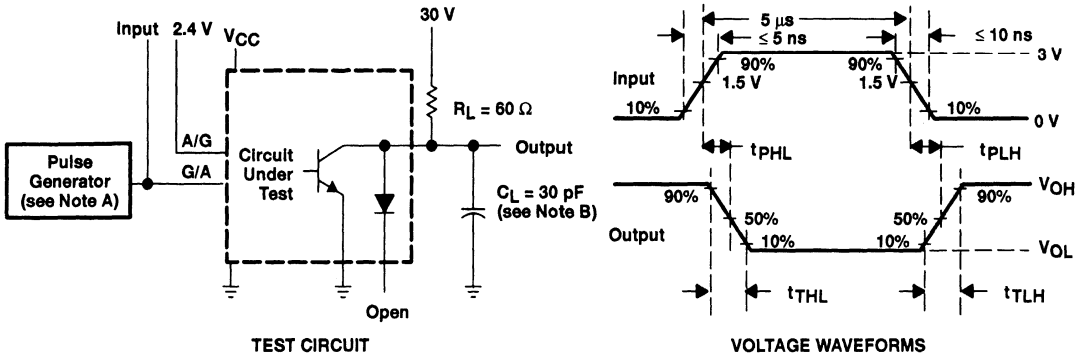
PARAMETER		TEST CONDITIONS		SN75436, SN75437A			SN75438			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA		−0.9	−1.5		−0.9	−1.5	V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V	I_{OL} = 250 mA		0.14	0.25		0.14	0.25	V
			I_{OL} = 500 mA		0.28	0.5		0.28	0.5	
			I_{OL} = 750 mA					0.42	0.75	
			I_{OL} = 1 A					0.6	1	
$V_{R(K)}$	Output clamp-diode reverse voltage	V_{CC} = 4.75 V,	I_R = 100 μA	70	100		70	100		V
$V_{F(K)}$	Output clamp-diode forward voltage	I_F = 500 mA			1	1.6		1	1.6	V
		I_F = 1 A						1.2	2	
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V	V_{IH} = 2 V, V_{OH} = 70 V		1	100		1	100	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.25 V		0.1	10		0.1	10	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.8 V		−0.25	−10		−0.25	−10	μA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 0		1	4		1	4	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 5 V		45	65		45	65	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

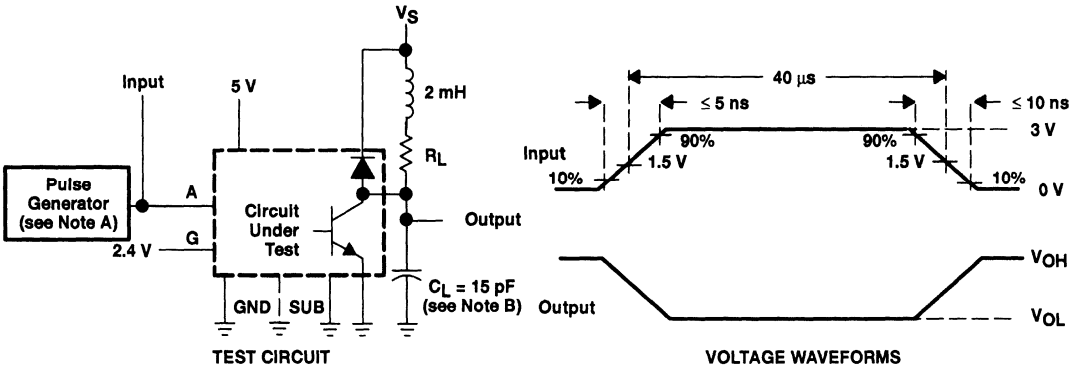
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		C_L = 30 pF, See Figure 1		1950	5000	ns
t_{PHL}	Propagation delay time, high-to-low-level output		R_L = 60 Ω,		150	500	ns
t_{TLH}	Transition time, low-to-high-level output				40		ns
t_{THL}	Transition time, high-to-low-level output				36		ns
V_{OH}	High-level output voltage after switching	SN75436	V_S = 50 V, R_L = 100 Ω, I_O ≈ 500 mA, See Figure 2	V_S−10			mV
		SN75437A	V_S = 35 V, R_L = 70 Ω, I_O ≈ 500 mA, See Figure 2	V_S−10			mV
		SN75438	V_S = 35 V, R_L = 35 Ω, I_O ≈ 1 A, See Figure 2	V_S−10			mV

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

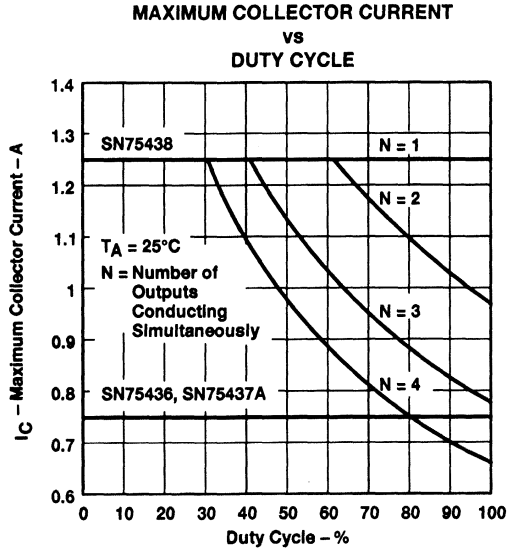


Figure 3

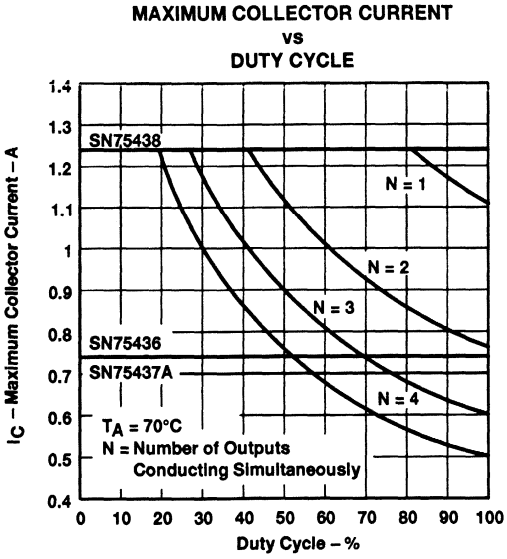


Figure 4

APPLICATION INFORMATION

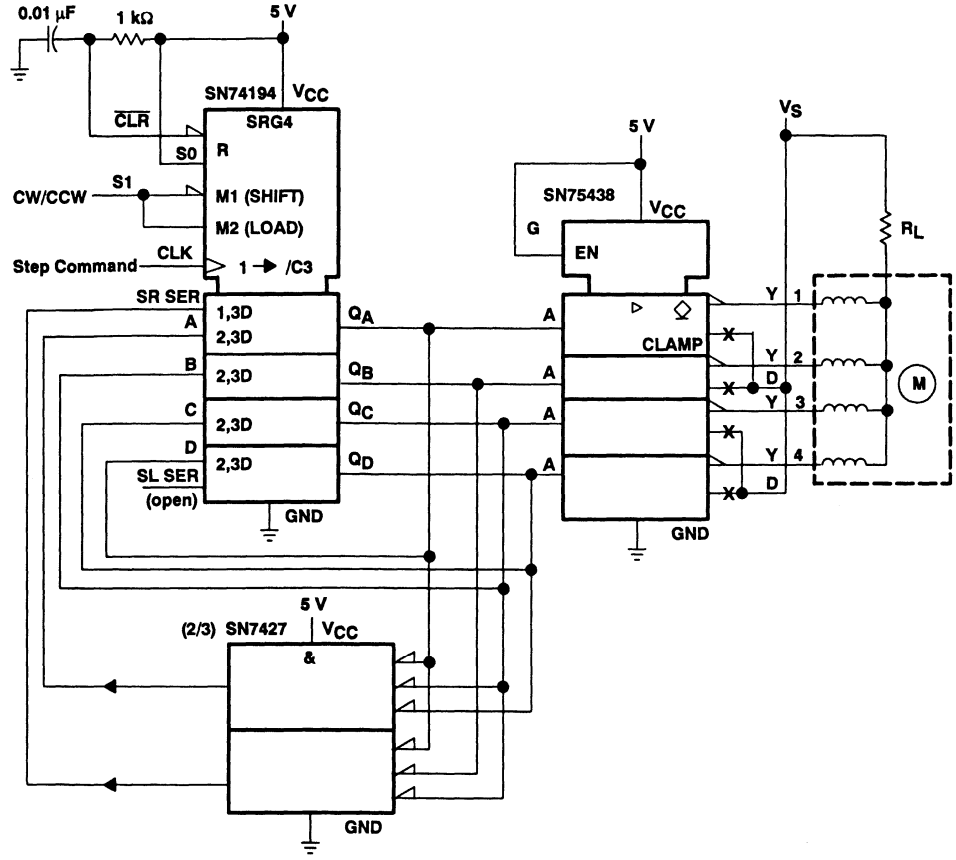


Figure 5. Four-Winding Stepper-Motor Control Circuit

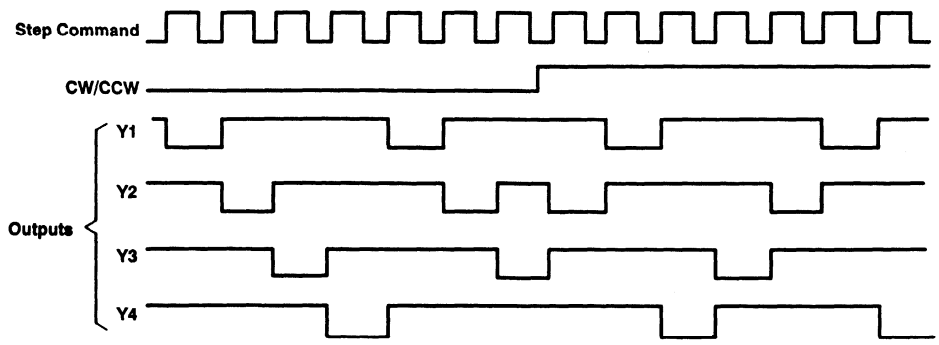
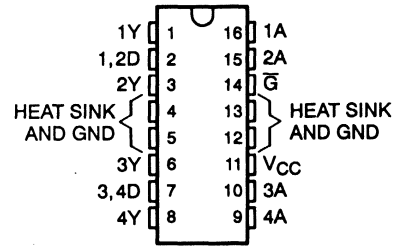


Figure 6. Timing Diagram

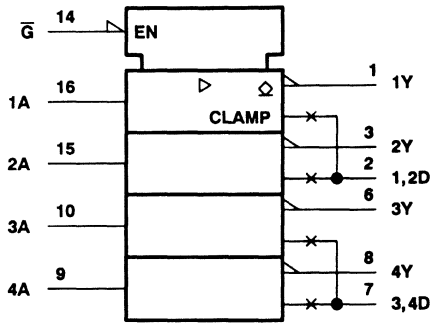
SLRS013A – D3116, MAY 1988 – REVISED NOVEMBER 1989

- **1.3-A Current Capability Each Channel**
- **Saturating Outputs With Low On-State Resistance**
- **Two Inverting and Two Noninverting Driver Channels With Common Active-Low Enable Input**
- **Key Application Is as a Complete Full-Step 4-Phase DC Stepper Motor Driver Using Only Three Directly Connected Logic Control Signal Lines From Standard Microprocessors**
- **High-Impedance Inputs Compatible With TTL or CMOS Levels**
- **Very Low Standby Power . . . 10 mW Typ**
- **50-V Noninductive Switching Voltage Capability**
- **40-V Inductive Switching Voltage Capability**
- **Output Clamp Diodes for Inductive Transient Protection**
- **2-W Power Package**

NE PACKAGE
(TOP VIEW)



logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

description

The SN75439 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. The device features two inverting and two noninverting open-collector outputs with a common-enable input that, when taken high, disables all four outputs. By pairing each inverting channel with a corresponding noninverting channel (such as channel 1 paired with channel 2 and channel 3 paired with channel 4), the device may be used as a complete full-step 4-phase dc stepper-motor driver using only two input logic control signals plus the enable signal, as shown in Figure 3. Other applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand loads.

The SN75439 is characterized for operation from 0°C to 70°C.

Function Tables

EACH CHANNEL 1 OR CHANNEL 4 DRIVER

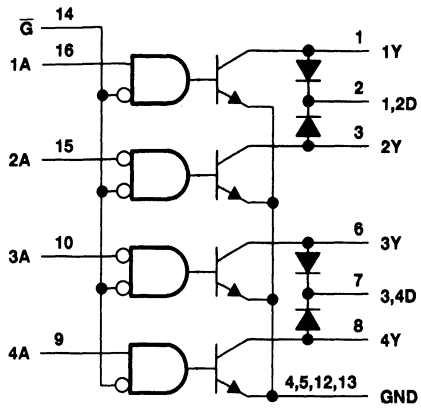
INPUTS		OUTPUT
A	$\overline{G}$	Y
H	L	L
L	X	H
X	H	H

EACH CHANNEL 2 OR CHANNEL 3 DRIVER

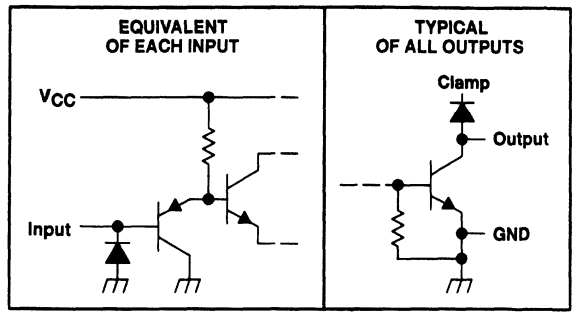
INPUTS		OUTPUT
A	$\overline{G}$	Y
L	L	L
H	X	H
X	H	H

H = high level, L = low level X = irrelevant

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.3 V to 7 V
Input voltage, V_I ..... 7 V
Output voltage range, V_O ..... −0.3 V to 52 V
Output voltage, V_O (inductive load) ..... 43 V
Output clamp-diode terminal voltage range, V_{OK} ..... −0.3 V to 52 V
Input current, I_I ..... −15 mA
Peak sink output current, I_{OM} (nonrepetitive, $t_w \leq 0.1$ ms) (see Note 2) ..... 1.5 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 50%) ..... 1.4 A
Continuous sink output current, I_O (see Note 2) ..... 1.3 A
Peak output clamp diode current, I_{OKM} (nonrepetitive, $t_w \leq 0.1$ ms) (see Note 2) ..... 1.5 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 50%) ..... 1.3 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) ..... 2075 mW
Continuous total dissipation at (or below) 65°C case temperature (see Note 3) ..... 5000 mW
Operating case or virtual junction temperature range ..... −55°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to the network GND (unless otherwise specified).
2. All four channels of this device may conduct rated current simultaneously; however, power dissipation average over a short time interval must fall within the continuous dissipation range.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. For operation above 65°C case temperature, derate linearly at the rate of 59 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Output supply voltage in inductive switching circuit, V_S (see Figure 2)			40	V
High-level input voltage, V_{IH}	2		5.25	V
Low-level input voltage, V_{IL}	−0.3†		0.8	V
Low-level output current, I_{OL}			1.3	A
Operating free-air temperature, T_A	0	25	70	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 A	See Note 4		0.2	0.35	V
		I_{OL} = 1 A			0.4	0.7	
		I_{OL} = 1.3 A			0.5	0.9	
$V_{F(K)}$	Output clamp-diode forward voltage	I_F = 0.5 A	See Note 4		1.1	1.9	V
		I_F = 1 A			1.3	2.2	
		I_F = 1.3 A			1.4	2.4	
I_{OH}	High-level output current	V_{OH} = 50 V,	V_{OK} = 50 V			100	μA
I_{IH}	High-level input current	$V_I = V_{IH}$				10	μA
I_{IL}	Low-level input current	V_I = 0 to 0.8 V				−10	μA
$I_{R(K)}$	Output clamp-diode reverse current (at Y output)	V_R = 50 V,	V_O = 0			100	μA
I_{CC}	Supply current	All outputs at high level (off)			2	8	mA
		All outputs at low level (on)			140	200	
		Two outputs at high level (off) and two outputs at low level (on)			70	110	

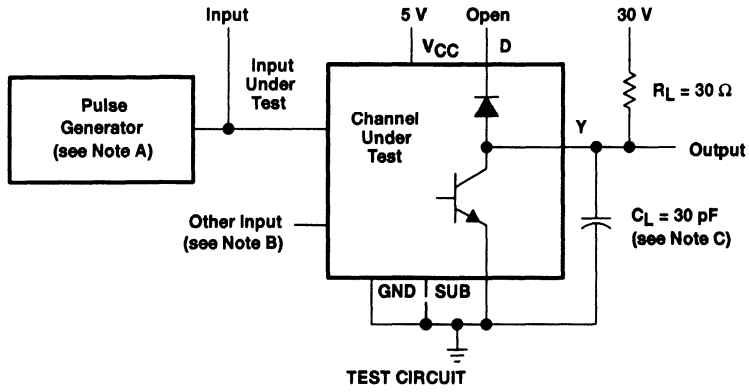
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 4: These parameters must be measured using pulse techniques, t_w = 1 ms, duty cycle ≤ 10%.

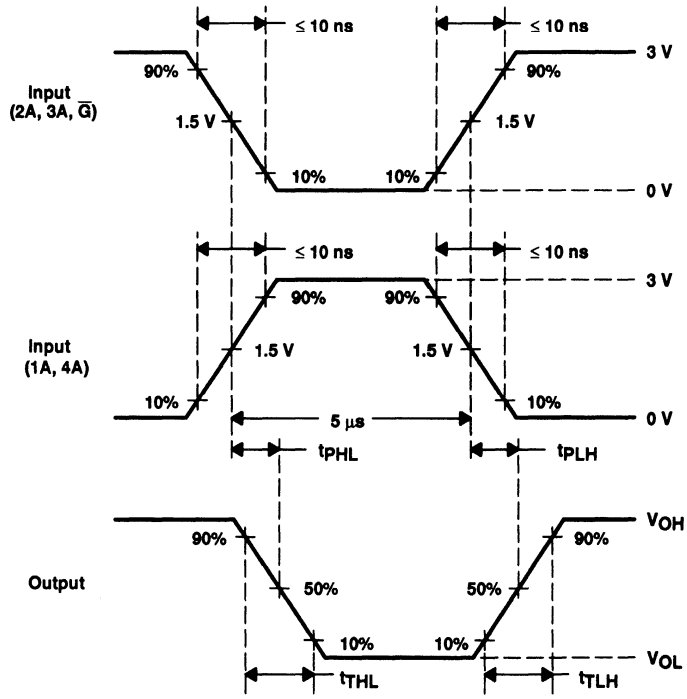
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_{OL} ≈ 1 A, R_L = 30 Ω,	C_L = 30 pF, See Figure 1		1500		ns
t_{PHL}	Propagation delay time, high-to-low-level output				100		ns
t_{TLH}	Transition time, low-to-high-level output				170		ns
t_{THL}	Transition time, high-to-low-level output				50		ns
V_{OH}	High-level output voltage (after switching inductive load)	V_S = 40 V, R_L = 31 Ω,	I_O ≈ 1.3 A, See Figure 2	V_S − 100			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

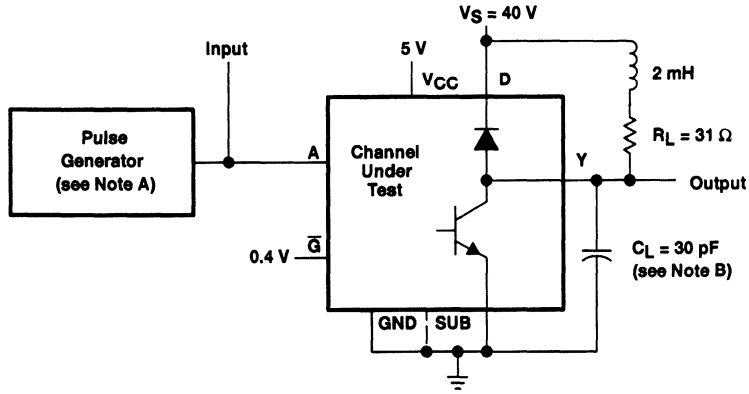


VOLTAGE WAVEFORMS

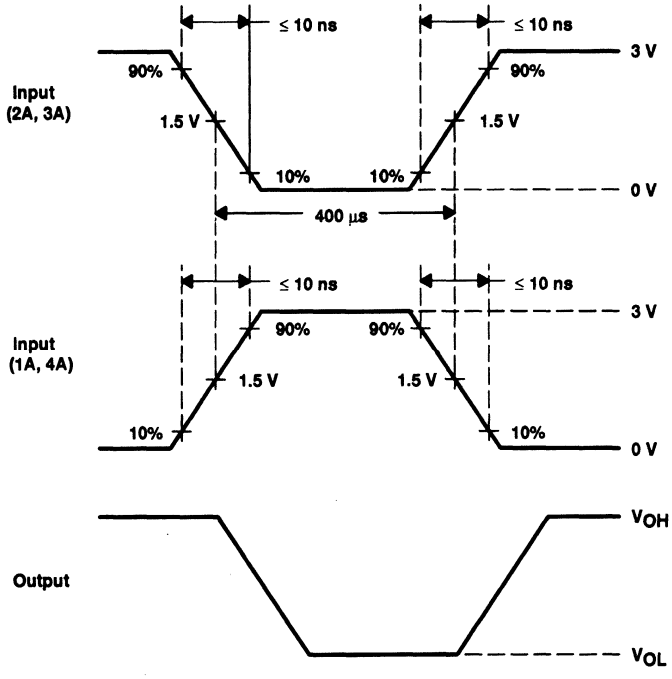
NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1 %, Z_O = 50 Ω.
B. Enable input $\overline{G}$ is at 0 V if input A is used as the switching input. When $\overline{G}$ is used as the switching input, the corresponding A input is at 0 V if testing channel 2 or channel 3 or at 3 V if testing channel 1 or channel 4.
C. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

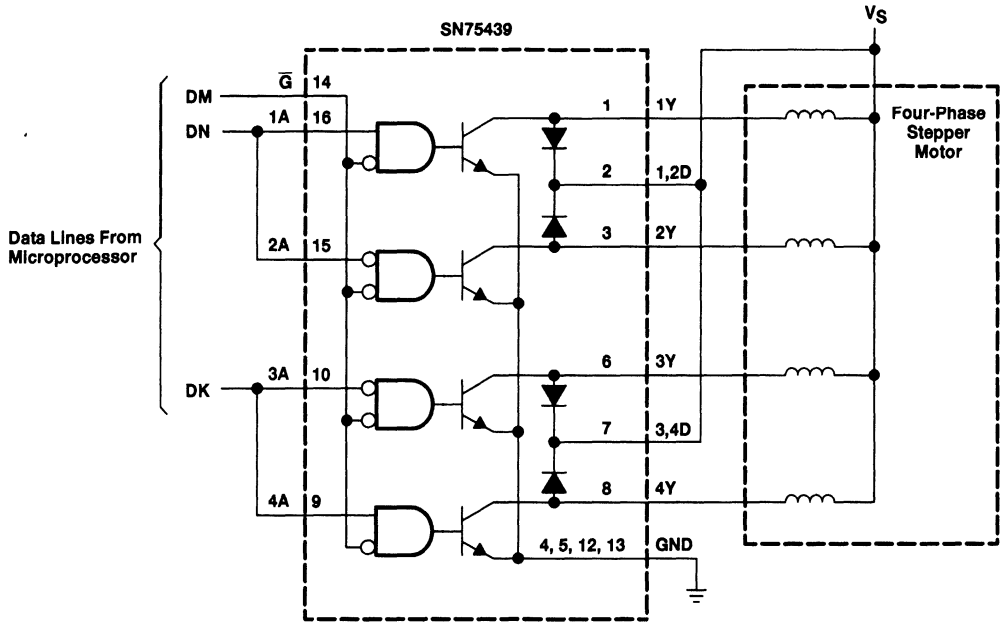


VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1 %, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Output Latch-Up Test Circuit and Voltage Waveforms

APPLICATION INFORMATION



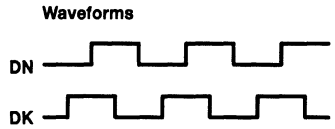
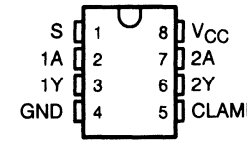


Figure 3. Full-Step Four-Phase Stepper-Motor Driver

SLRS020 – D2481, DECEMBER 1978 – REVISED DECEMBER 1989

- **Very Low Power Requirements**
- **Very Low Input Current**
- **Characterized for Use to 350 mA**
- **No Output Latch-Up at 50 V (After Conducting 300 mA)**
- **High-Voltage Outputs (70 V Min)**
- **Output Clamp Diodes for Transient Suppression (350 mA, 70 V)**
- **TTL- or MOS-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltage**
- **Suitable for Hammer-Driver Applications**

D OR P PACKAGE
(TOP VIEW)

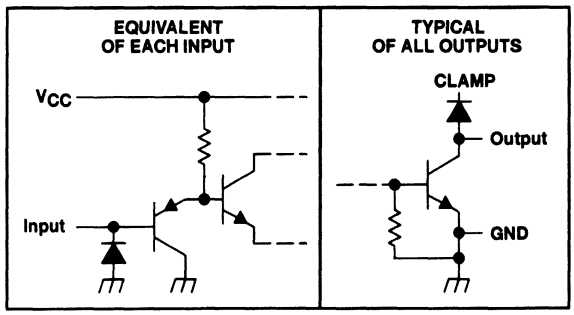


description

Series SN75446 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75446, SN75447, SN75448, and SN75449 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs.

Series SN75446 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



Function Tables

SN75446
(each AND driver)

INPUTS		OUTPUT
A	S	Y
H	H	H
L	X	L
X	L	L

SN75447
(each NAND driver)

INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

SN75448
(each OR driver)

INPUTS		OUTPUT
A	S	Y
H	X	H
X	H	H
L	L	L

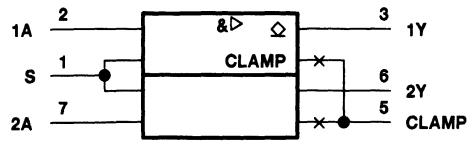
SN75449
(each NOR driver)

INPUTS		OUTPUT
A	S	Y
H	X	L
X	H	L
L	L	H

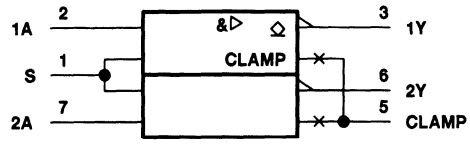
H = high level, L = low level
X = irrelevant

logic symbols†

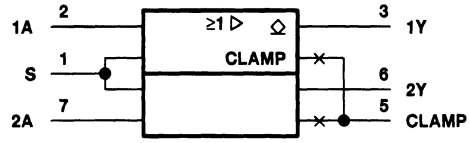
SN75446



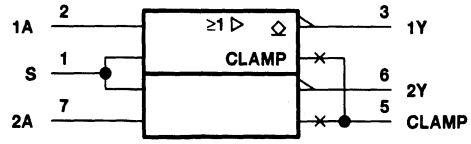
SN75447



SN75448



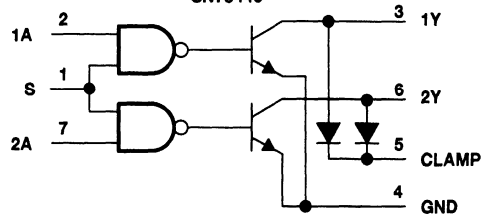
SN75449



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

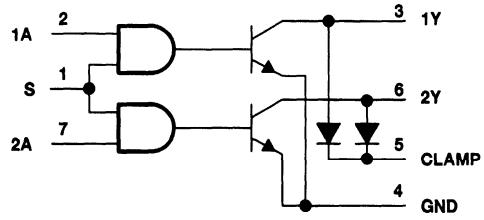
logic diagrams (positive logic)

SN75446



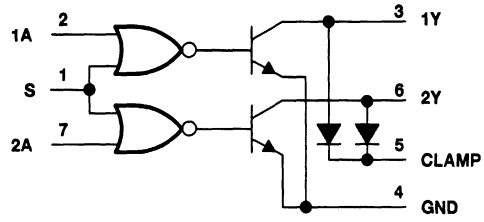
positive logic: $Y = AS$ or $\overline{\overline{A}+\overline{S}}$

SN75447



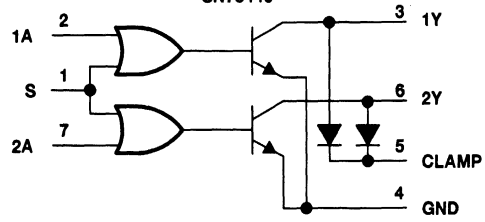
positive logic: $Y = \overline{AS}$ or $\overline{A}+\overline{S}$

SN75448



positive logic: $Y = A+S$ or $\overline{\overline{A}\,\overline{S}}$

SN75449



positive logic: $Y = \overline{A+S}$ or $\overline{A}\,\overline{S}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Output current (see Note 2) ..... 400 mA
Output clamp-diode current ..... 400 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to network GND.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

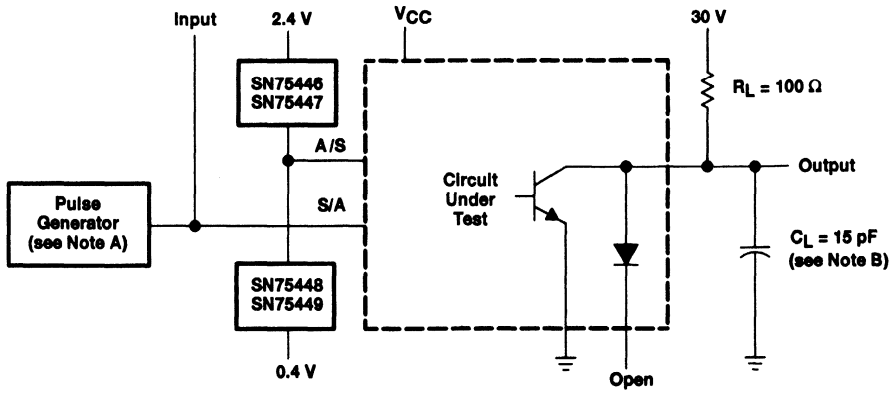
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -12$ mA			−0.9	−1.5	V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	$I_{OL} = 100$ mA		0.1	0.3	V
				$I_{OL} = 200$ mA		0.22	0.45	
				$I_{OL} = 300$ mA		0.45	0.65	
				$I_{OL} = 350$ mA		0.55	0.75	
$V_{O(BR)}$	Output breakdown voltage		$V_{CC} = 4.75$ V,	$I_{OH} = 100$ µA	70	100		V
$V_{R(K)}$	Output clamp-diode reverse voltage		$V_{CC} = 4.75$ V,	$I_R = 100$ µA	70	100		V
$V_{F(K)}$	Output clamp-diode forward voltage		$V_{CC} = 4.75$ V,	$I_F = 350$ mA	0.6	1.2	1.6	V
I_{OH}	High-level output current		$V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V,	$V_{IH} = 2$ V, $V_{OH} = 70$ V		1	100	µA
I_{IH}	High-level input current		$V_{CC} = 5.25$ V,	$V_I = 5.25$ V		0.01	10	µA
I_{IL}	Low-level input current	A input	$V_{CC} = 5.25$ V,	$V_I = 0.8$ V		−0.5	−10	µA
		Strobe S				−1	−20	
I_{CCH}	Supply current, outputs high	SN75446	$V_{CC} = 5.25$ V	$V_I = 5$ V		11	18	mA
		SN75447		$V_I = 0$		11	18	
		SN75448		$V_I = 5$ V		18	25	
		SN75449		$V_I = 0$		18	25	
I_{CCL}	Supply current, outputs low	SN75446	$V_{CC} = 5.25$ V	$V_I = 0$		11	18	mA
		SN75447		$V_I = 5$ V		11	18	
		SN75448		$V_I = 0$		18	25	
		SN75449		$V_I = 5$ V		18	25	

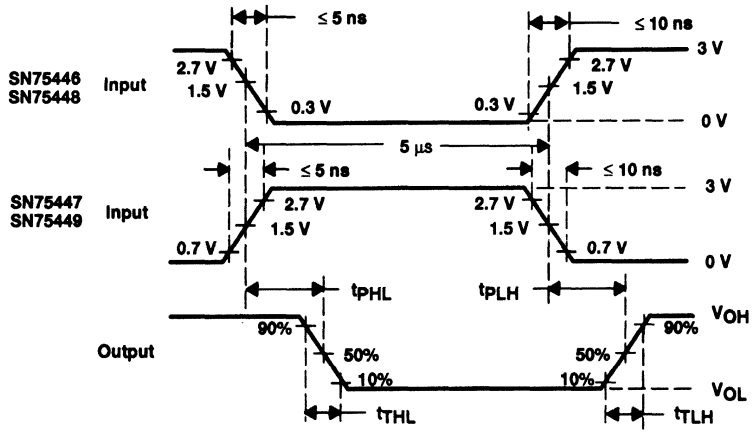
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$C_L = 15$ pF, $R_L = 100\ \Omega$, See Figure 1		300	750	ns
t_{PHL}	Propagation delay time, high-to-low-level output			200	500	ns
t_{TLH}	Transition time, low-to-high-level output			50	100	ns
t_{THL}	Transition time, high-to-low-level output			50	100	ns
V_{OH}	High-level output voltage after switching	$V_S = 55$ V, $I_O \approx 300$ mA, See Figure 2	$V_S - 0.018$			V

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

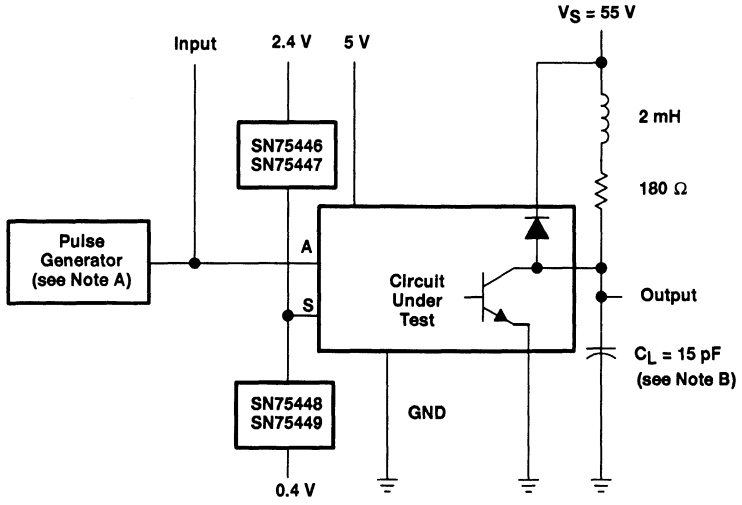


VOLTAGE WAVEFORMS

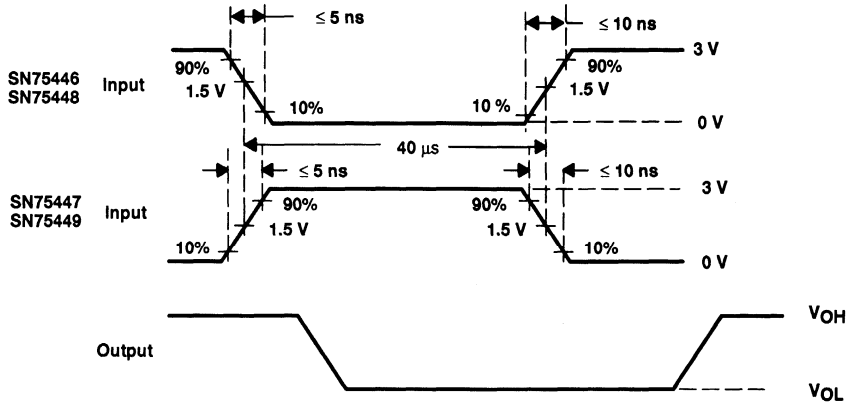
NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

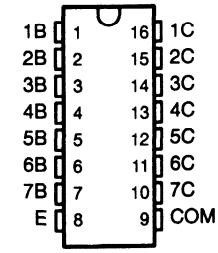
Figure 2. Latch-Up Test Circuit and Voltage Waveforms

SLRS023A – D2625, DECEMBER 1976 – REVISED APRIL 1993

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 100 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay Driver Applications**
- **Higher-Voltage Versions of ULN2001A, ULN2002A, ULN2003A, and ULN2004A, Respectively, for Commercial Temperature Range**

D OR N PACKAGE
(TOP VIEW)

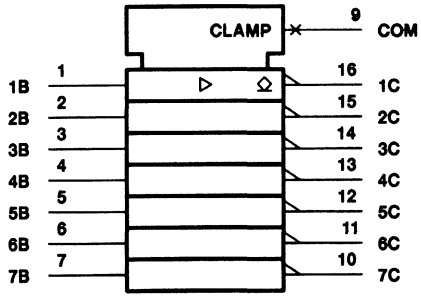


description

The SN75466, SN75467, SN75468, and SN75469 are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

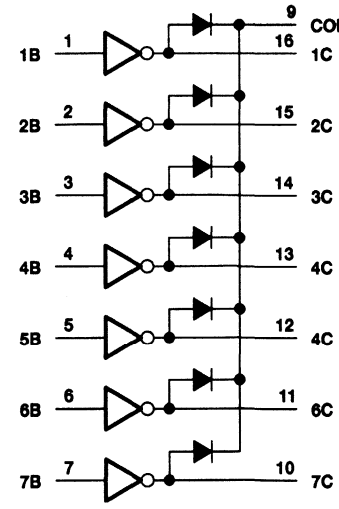
The SN75466 is a general-purpose array and can be used with TTL, P-MOS, CMOS, and other MOS technologies. The SN75467 is specifically designed for use with 14- to 25-V P-MOS devices, and each input has a zener diode and resistor in series to limit the input current to a safe limit. The SN75468 has a 2700-Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a 10.5-kΩ series base resistor to allow its operation directly from CMOS or P-MOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468 and the required voltage is less than that required by the SN75467.

logic symbol†

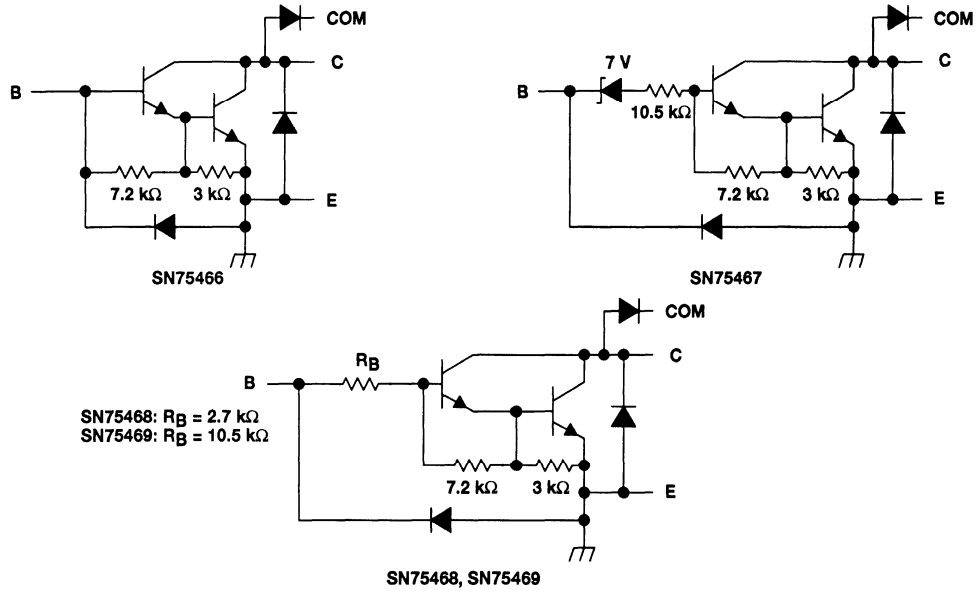


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

logic diagram



schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage	100 V
Input voltage (see Note 1)	30 V
Peak collector current (see Figures 14 and 15)	500 mA
Output clamp current, I_{OK}	500 mA
Total emitter-terminal current	−2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN75466			SN75467			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V,	I_C = 300 mA						13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
V_F	Clamp-diode forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V,	I_I = 0			50			50	µA
			V_{CE} = 100 V, T_A = 70°C	I_I = 0			100			100	
		2		V_I = 6 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 17 V						0.82	1.25	mA
h_{FE}	Static forward current transfer ratio	6	V_{CE} = 2 V,	I_C = 350 mA	1000						
I_R	Clamp-diode forward voltage	7	V_R = 100 V				50			50	µA
			V_R = 100 V,	T_A = 70°C			100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		SN75468			SN75469			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V,	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	I_I = 250 µA ,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA ,	I_C = 350 mA		1.2	1.6		1.2	1.6	
V_F	Clamp-diode forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V,	I_I = 0			50			50	µA
			V_{CE} = 100 V, T_A = 70°C	I_I = 0			100			100	
		2		V_I = 1 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp-diode reverse current	7	V_R = 100 V				50			50	µA
			V_R = 100 V,	T_A = 70°C			100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

switching characteristics, T_A = 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_S = 50 V, R_L = 163 Ω, C_L = 15 pF, See Figure 9		0.25	1	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.25	1	μs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, See Figure 10	V_S–20			mV

PARAMETER MEASUREMENT INFORMATION

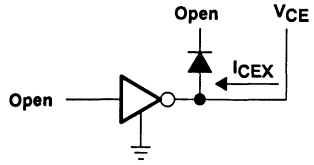


Figure 1. I_{CEX}

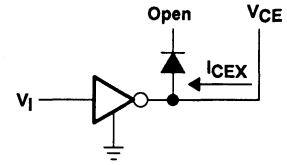


Figure 2. I_{CEX}

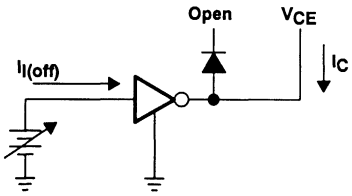


Figure 3. $I_{I(off)}$

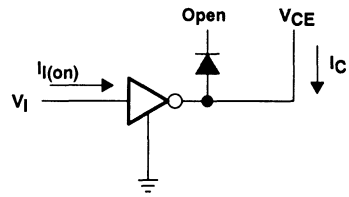


Figure 4. I_I

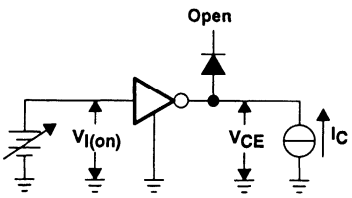
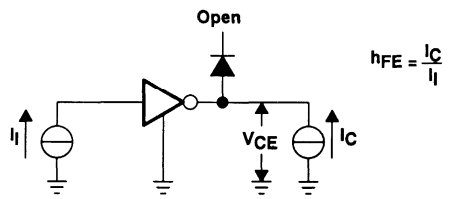


Figure 5. $V_{I(on)}$



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 6. h_{FE}, $V_{CE(sat)}$

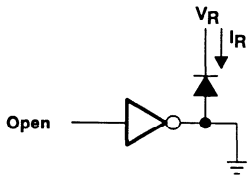


Figure 7. I_R

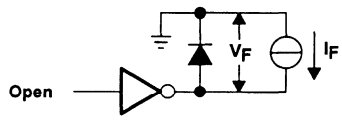


Figure 8. V_F

PARAMETER MEASUREMENT INFORMATION

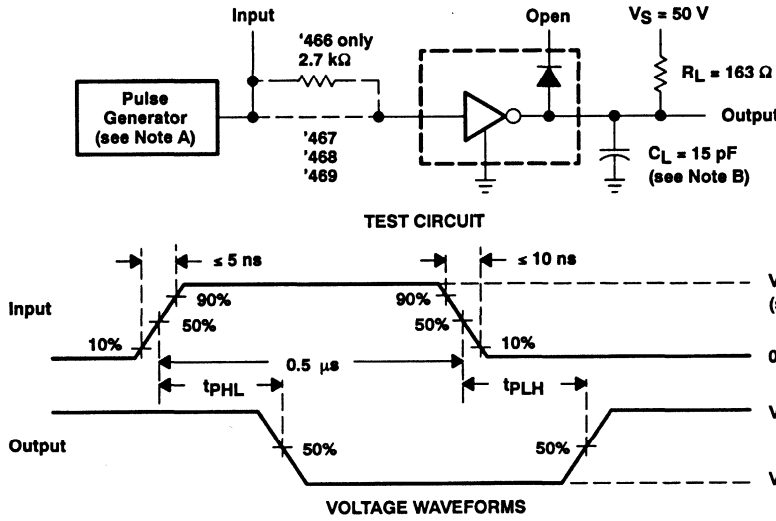


Figure 9. Test Circuit and Voltage Waveforms

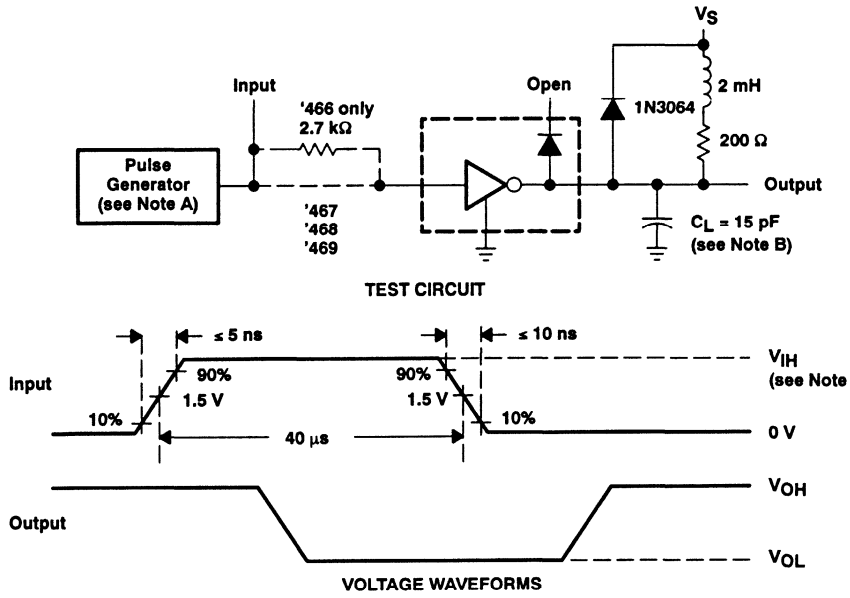


Figure 10. Latch-Up Test Circuit and Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the '466 and '468, V_{IH} = 3 V; for the '467, V_{IH} = 13 V; for the '469, V_{IH} = 8 V.

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

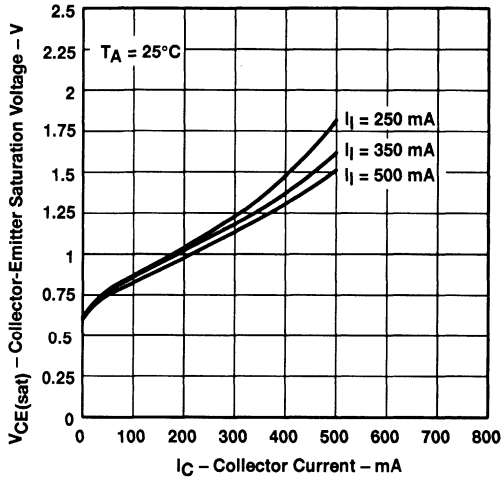


Figure 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

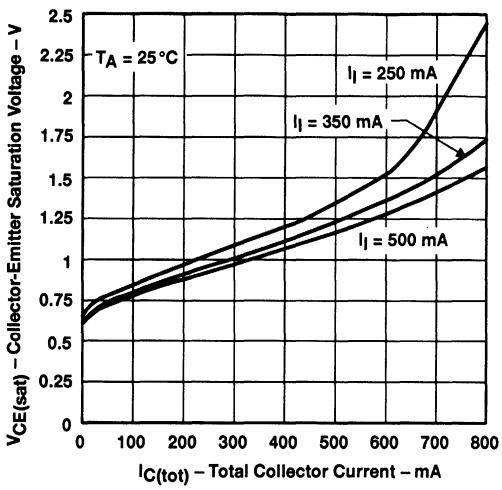


Figure 12

COLLECTOR CURRENT vs INPUT CURRENT

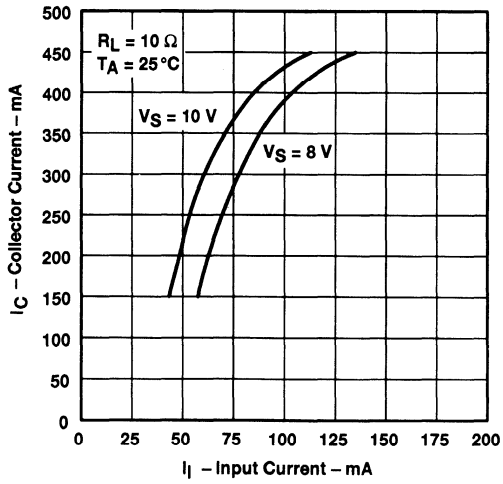


Figure 13

THERMAL INFORMATION

D PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

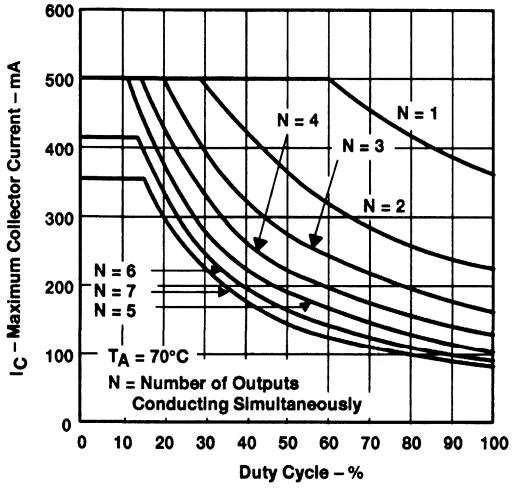


Figure 14

N PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

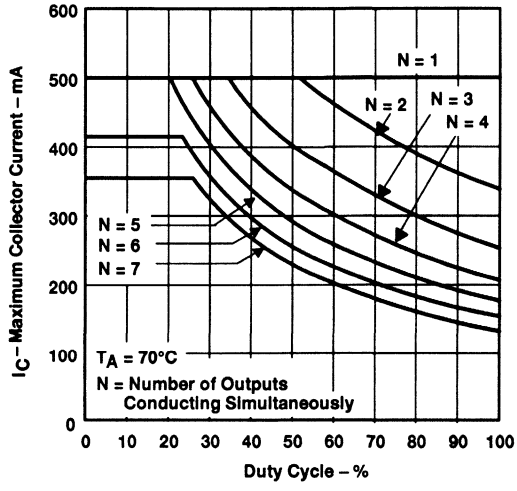


Figure 15

APPLICATION INFORMATION

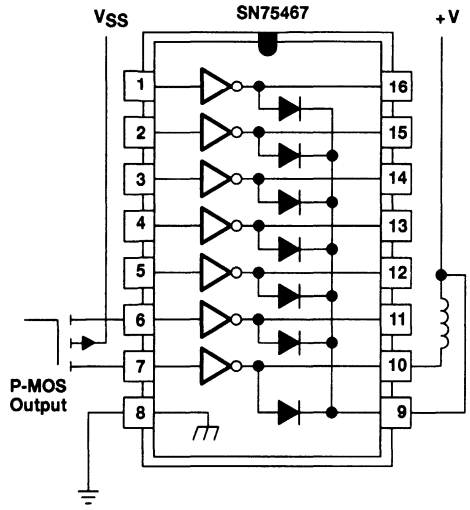


Figure 16. P-MOS to Load

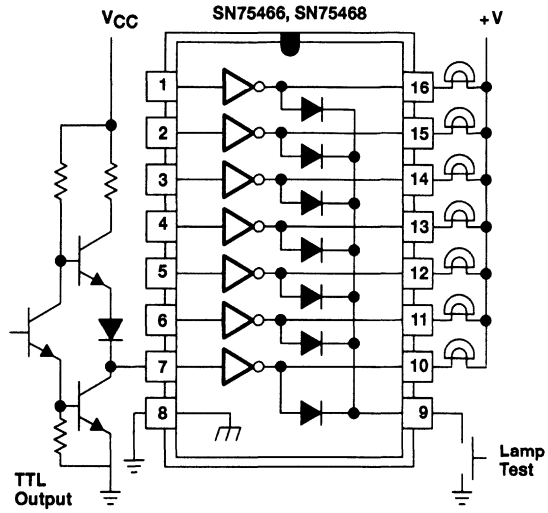


Figure 17. TTL to Load

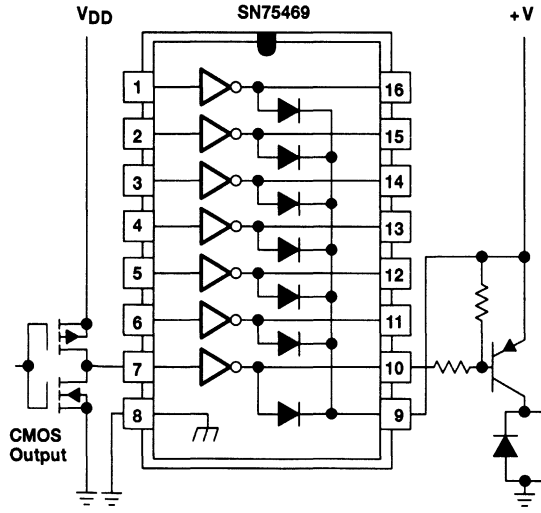


Figure 18. Buffer for Higher Current Loads

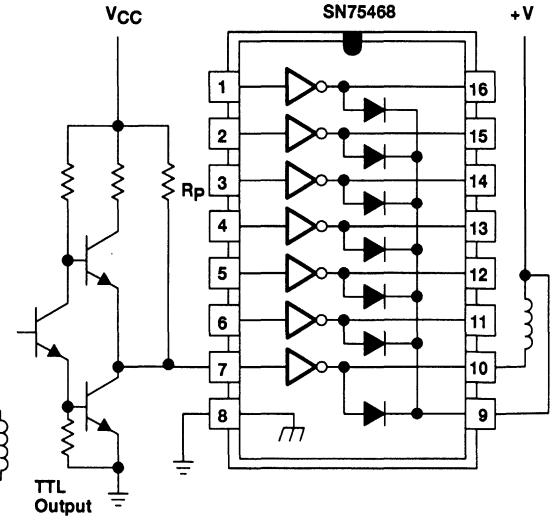


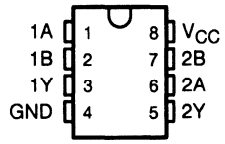
Figure 19. Use of Pullup Resistors to Increase Drive Current

SLRS024 – D2130, DECEMBER 1976 – REVISED MAY 1990

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE HIGH-CURRENT DRIVER APPLICATIONS

- **Characterized for Use to 300 mA**
- **High-Voltage Outputs**
- **No Output Latch-Up at 55 V (After Conducting 300 mA)**
- **Medium-Speed Switching**
- **Circuit Flexibility for Varied Applications and Choice of Logic Function**
- **TTL-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltages**
- **Plastic DIP (P) With Copper Lead Frame Provides Cooler Operation and Improved Reliability**

D OR P PACKAGE
(TOP VIEW)



SUMMARY OF SERIES SN75471

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN75471	AND	D, P
SN75472	NAND	D, P
SN75473	OR	D, P

description

Series SN75471 dual peripheral drivers are functionally interchangeable with Series SN75451B and Series SN75461 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds than Series 75451B (limits are the same as Series SN75461). Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN75471, SN75472, and SN75473 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic), with the output of the logic gates internally connected to the bases of the npn output transistors.

Series SN75471 drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Interemitter voltage (see Note 2) ..... 5.5 V
Off-state output voltage ..... 70 V
Continuous collector or output current (see Note 3) ..... 400 mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 3) ..... 500 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to the network GND, unless otherwise specified.
2. This is the voltage between two emitters, A and B.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

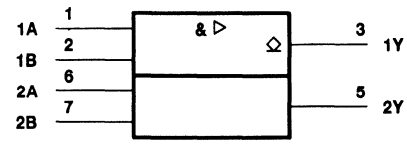
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

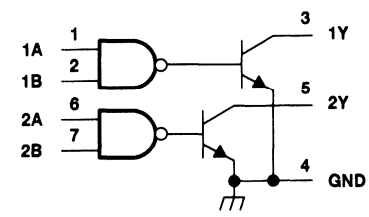
	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

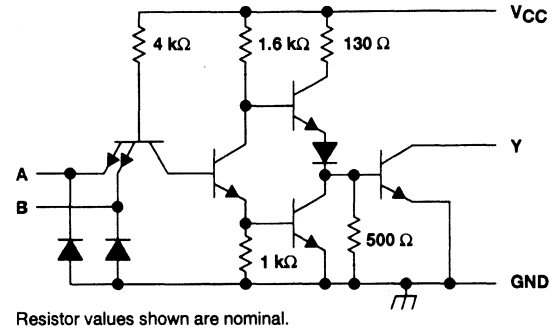


FUNCTION TABLE
(each driver)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic: $Y = AB$ or $\overline{\overline{A} + \overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

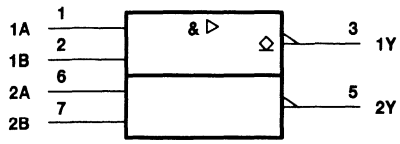
PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA			−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V,	V_{IH} = 2 V,	V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V			−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 5 V			7	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 0			52	65	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

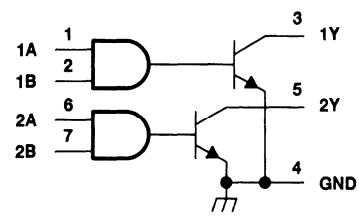
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, R_L = 50 Ω,	C_L = 15 pF, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output				25	40	
t_{TLH}	Transition time, low-to-high-level output				8	20	
t_{THL}	Transition time, high-to-low-level output				10	20	
V_{OH}	High-level output voltage after switching	V_S = 55 V, See Figure 2	I_O ≈ 300 mA,	V_S−18			mV

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

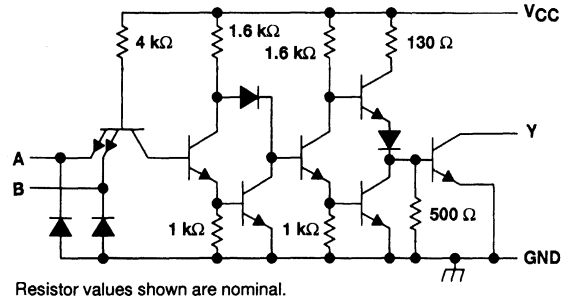


FUNCTION TABLE (each driver)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

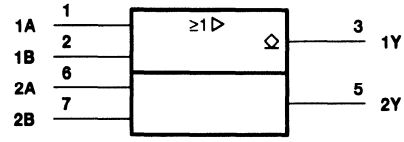
PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA			−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V,	V_{IH} = 2 V,	V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V			−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 5 V			13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 0			61	76	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

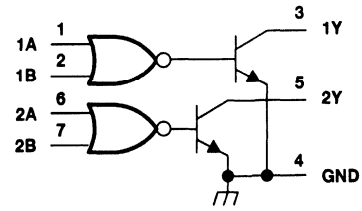
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, R_L = 50 Ω,	C_L = 15 pF, See Figure 1		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	50	
t_{TLH}	Transition time, low-to-high-level output				13	25	
t_{THL}	Transition time, high-to-low-level output				10	20	
V_{OH}	High-level output voltage after switching	V_S = 55 V, See Figure 2	I_O ≈ 300 mA,	V_S−18			mV

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

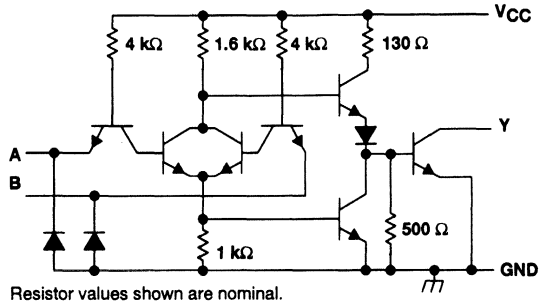


FUNCTION TABLE (each driver)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
$Y = A + B$ or $\overline{\overline{A}\,\overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

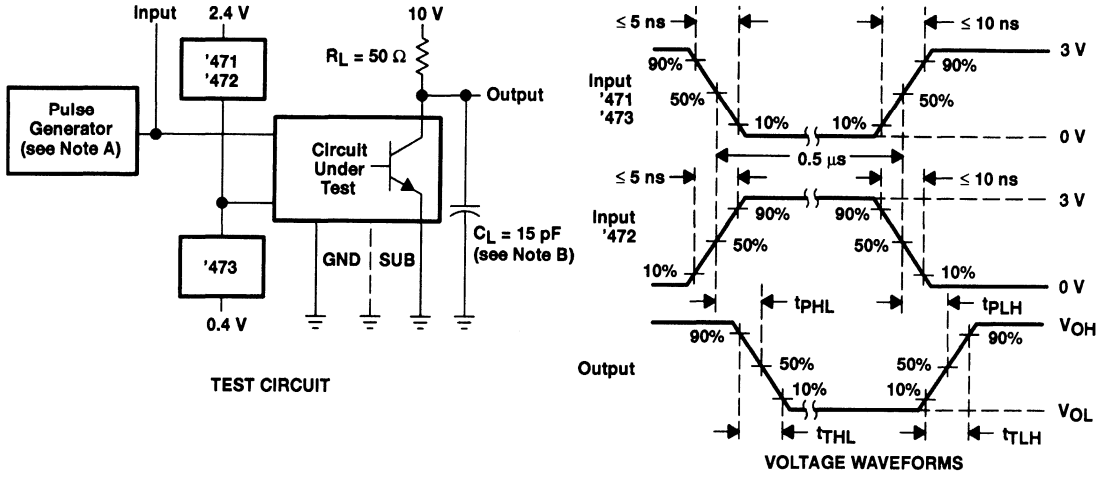
PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA			−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V,	V_{IH} = 2 V,	V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V,	V_{IL} = 0.8 V,	I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.4 V			−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 5 V			8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 0			58	76	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

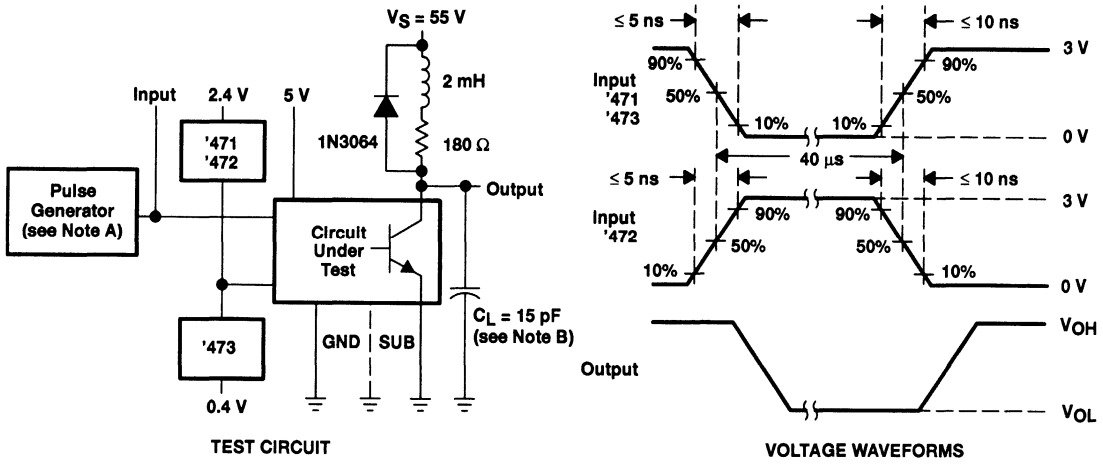
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, R_L = 50 Ω,	C_L = 15 pF, See Figure 1			30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output					25	40	
t_{TLH}	Transition time, low-to-high-level output					8	25	
t_{THL}	Transition time, high-to-low-level output					10	25	
V_{OH}	High-level output voltage after switching	V_S = 55 V, See Figure 2	I_O ≈ 300 mA,		V_S−18			mV

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Switching Times

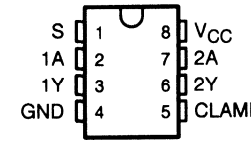


NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, $Z_O \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Latch-Up Test

- **Characterized for Use to 300 mA**
- **No Output Latch-Up at 55 V (After Conducting 300 mA)**
- **High-Voltage Outputs (100 V Typical)**
- **Output Clamp Diodes for Transient Suppression (300 mA, 70 V)**
- **TTL- or MOS-Compatible Diode-Clamped Inputs**
- **PNP Inputs Reduce Input Current**
- **Standard Supply Voltage**
- **Suitable for Hammer-Driver Applications**
- **Plastic DIP (P) With Copper Lead Frame Provides Cooler Operation and Improved Reliability**

D OR P PACKAGE
(TOP VIEW)

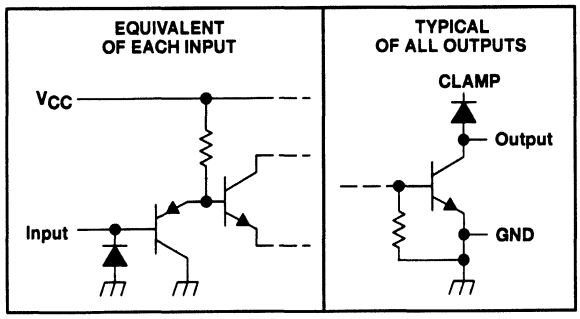


description

The SN75476 through SN75479 are dual peripheral drivers designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, SN75478, and SN75479 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage clamp diodes on the outputs for inductive transient protection.

The SN75476, SN75477, SN75478, and SN75479 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



Function Tables

SN75476
(each AND driver)

INPUTS		OUTPUT
A	S	Y
H	H	H
L	X	L
X	L	L

SN75477
(each NAND driver)

INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

SN75478
(each OR driver)

INPUTS		OUTPUT
A	S	Y
H	X	H
X	H	H
L	L	L

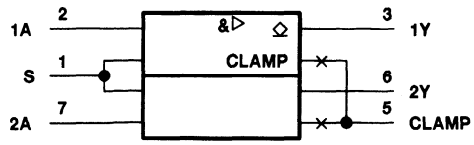
SN75479
(each NOR driver)

INPUTS		OUTPUT
A	S	Y
H	X	L
X	H	L
L	L	H

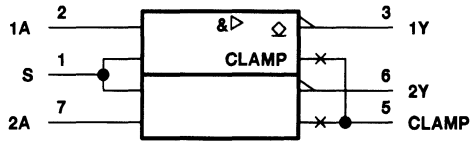
H = high level, L = low level
X = irrelevant

logic symbols†

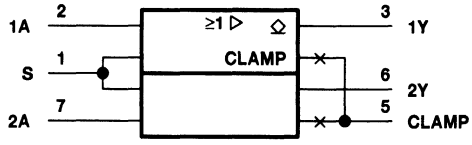
SN75476



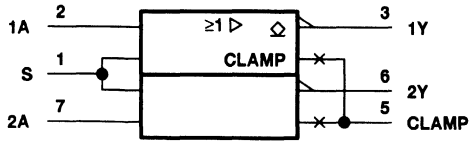
SN75477



SN75478



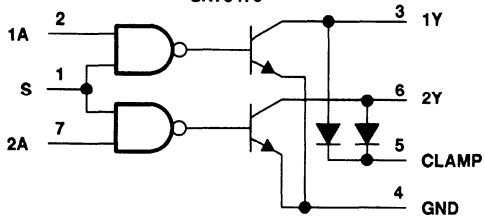
SN75479



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

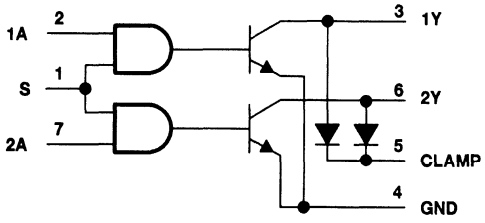
logic diagrams (positive logic)

SN75476



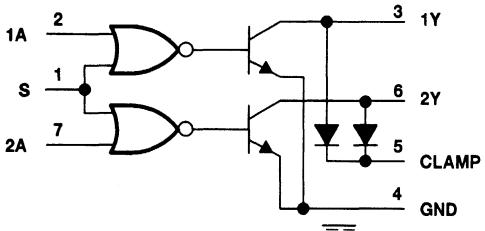
positive logic: $Y = AS$ or $\overline{\overline{A}+\overline{S}}$

SN75477



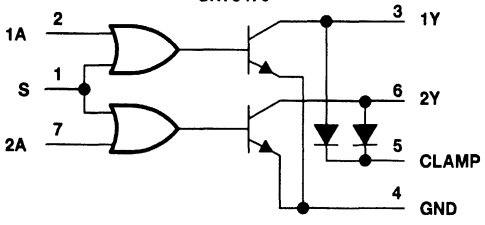
positive logic: $Y = \overline{AS}$ or $\overline{A}+\overline{S}$

SN75478



positive logic: $Y = A+S$ or $\overline{\overline{A}\,\overline{S}}$

SN75479



positive logic: $Y = \overline{A+S}$ or $\overline{A}\,\overline{S}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage, V_I ..... 5.5 V
Continuous output current (see Note 2) ..... 400 mA
Peak output current: $t_w \leq 10$ ms, duty cycle $\leq 50\%$ ..... 500 mA
$t_w \leq 30$ ns, duty cycle $\leq 0.002\%$ ..... 3 A
Output clamp current, I_{OK} ..... 400 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to network GND.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range

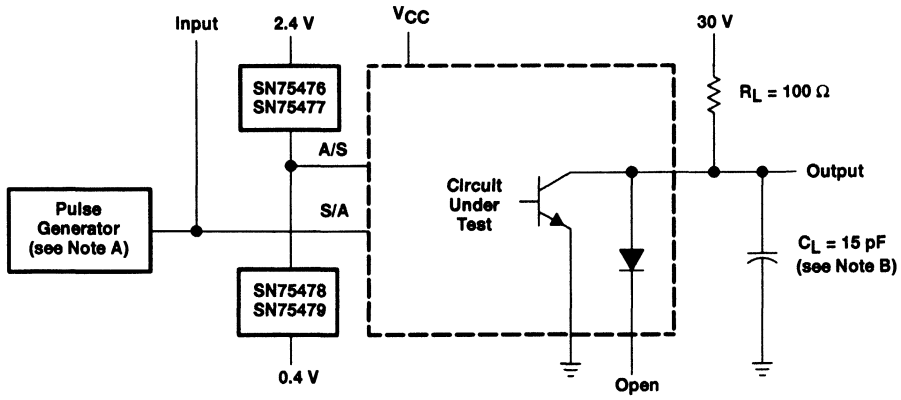
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA			−0.95	−1.5	V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 100 mA		0.16	0.3	V
				I_{OL} = 175 mA		0.22	0.5	
				I_{OL} = 300 mA		0.33	0.6	
$V_{O(BR)}$	Output breakdown voltage		V_{CC} = 4.5 V,	I_{OH} = 100 µA	70	100		V
$V_{R(K)}$	Output clamp reverse voltage		V_{CC} = 4.5 V,	I_R = 100 µA	70	100		V
$V_{F(K)}$	Output clamp forward voltage		V_{CC} = 4.5 V,	I_F = 300 mA	0.8	1.15	1.6	V
I_{OH}	High-level output current		V_{CC} = 4.5 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V		1	100	µA
I_{IH}	High-level input current		V_{CC} = 5.5 V,	V_I = 5.5 V		0.01	10	µA
I_{IL}	Low-level input current	A input	V_{CC} = 5.5 V,	V_I = 0.8 V		−80	−110	µA
		Strobe S				−160	−220	
I_{CCH}	Supply current, outputs high	SN75476	V_{CC} = 5.5 V	V_I = 5 V		10	17	mA
		SN75477		V_I = 0		10	17	
		SN75478		V_I = 5 V		10	17	
		SN75479		V_I = 0		10	17	
I_{CCL}	Supply current, outputs low	SN75476	V_{CC} = 5.5 V	V_I = 0		54	75	mA
		SN75477		V_I = 5 V		54	75	
		SN75478		V_I = 0		54	75	
		SN75479		V_I = 5 V		54	75	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

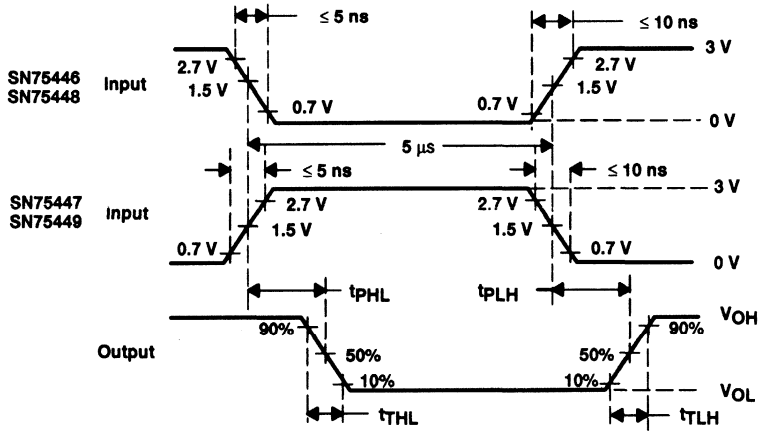
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 100 Ω, See Figure 1		200	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output			200	350	ns
t_{TLH}	Transition time, low-to-high-level output			50	125	ns
t_{THL}	Transition time, high-to-low-level output			90	125	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, I_O = 300 mA, See Figure 2	V_S−18			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

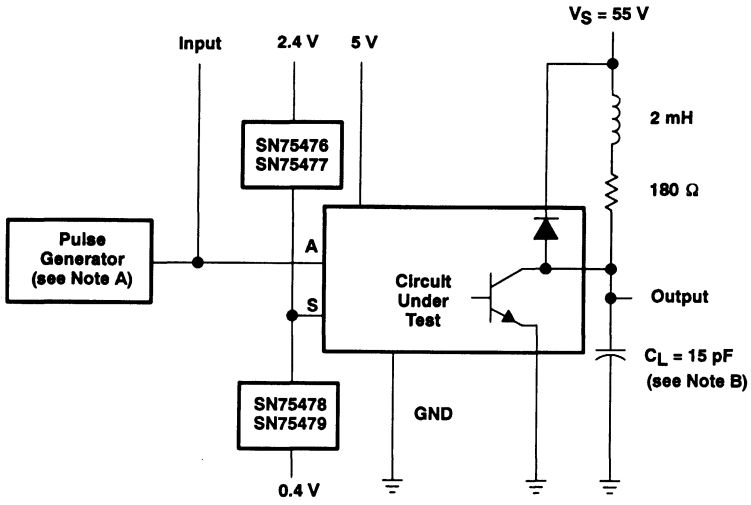


VOLTAGE WAVEFORMS

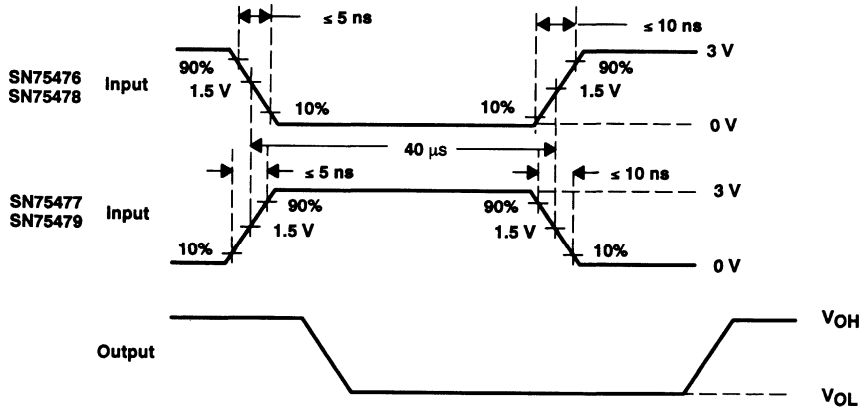
NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

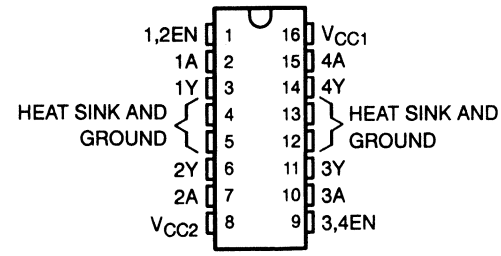
NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms

SLRS007A – D2942, NOVEMBER 1986 – REVISED APRIL 1993

- **1-A Output Current Capability Per Driver**
- **Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers**
- **Designed for Positive-Supply Applications**
- **Wide Supply Voltage Range: 4.5 V to 36 V**
- **TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs**
- **Separate Input-Logic Supply**
- **Thermal Shutdown**
- **Internal ESD Protection**
- **Input Hysteresis Improves Noise Immunity**
- **3-State Outputs**
- **Minimized Power Dissipation**
- **Sink/Source Interlock Circuitry Prevents Simultaneous Conduction**
- **No Output Glitch During Power Up or Power Down**
- **Improved Functional Replacement for the SGS L293**

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each driver)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level, L = low-level
X = irrelevant
Z = high-impedance (off)
† In the thermal shutdown mode, the output is in a high-impedance state regardless of the input levels.

description

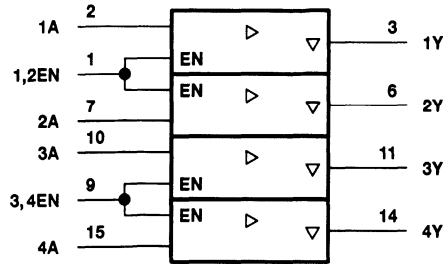
The SN754410 and the SN754411 are quadruple high-current half-H drivers designed to provide bidirectional drive currents of up to 1 A at voltages from 4.5 V to 36 V. They are designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are compatible with TTL and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

External high-speed output clamp diodes should be used for inductive-transient suppression with the SN754411. A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage V_{CC2} is used for the output circuits.

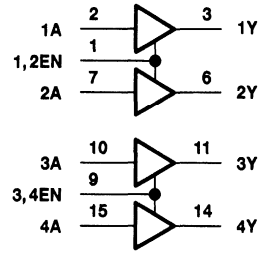
The SN754410 and SN754411 are designed for operation from −40°C to 85°C.

logic symbol†

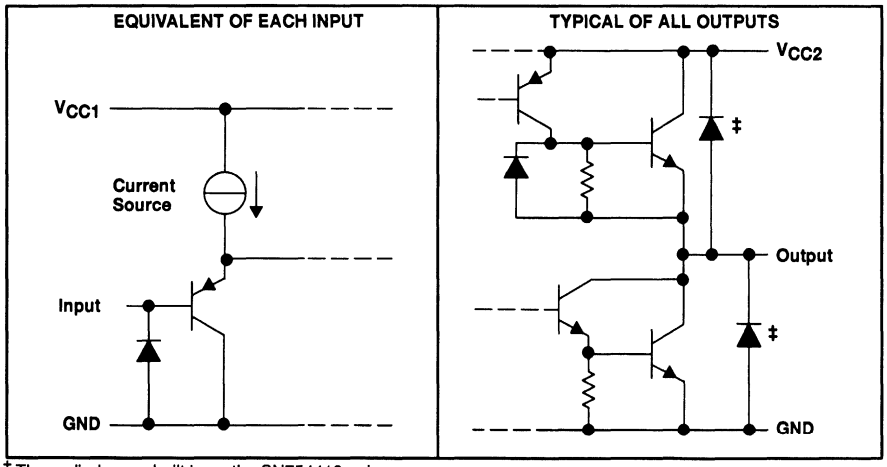


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



‡ These diodes are built in on the SN754410 only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage range, V_{CC1} (see Note 1) ..... −0.5 V to 36 V
Output supply voltage range, V_{CC2} ..... −0.5 V to 36 V
Input voltage, V_I ..... 36 V
Output voltage range, V_O ..... −3 V to V_{CC2} + 3 V
Peak output current (nonrepetitive, $t_w \leq 5$ ms) ..... ±2 A
Continuous output current, I_O ..... ±1.1 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 2075 mW
Operating free-air temperature range ..... −40°C to 85°C
Operating case or virtual junction temperature range ..... −40°C to 150°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. All voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC1}	4.5	5.5	V
Output supply voltage, V_{CC2}	4.5	36	V
High-level input voltage, V_{IH}	2	5.5	V
Low-level input voltage, V_{IL}	−0.3†	0.8	V
Operating virtual junction temperature, T_J	−40	125	°C
Operating free-air temperature, T_A	−40	85	°C

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of supply voltage and operating virtual junction temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -12$ mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	$I_{OH} = -0.5$ A		$V_{CC2}-1.5$	$V_{CC2}-1.1$		V
		$I_{OH} = -1$ A		$V_{CC2}-2$			
		$I_{OH} = -1$ A,	$T_J = 25°C$	$V_{CC2}-1.8$	$V_{CC2}-1.4$		
V_{OL}	Low-level output voltage	$I_{OL} = 0.5$ A			1	1.4	V
		$I_{OL} = 1$ A				2	
		$I_{OL} = 1$ A,	$T_J = 25°C$		1.2	1.8	
V_{OKH}‡	High-level output clamp voltage	$I_{OK} = -0.5$ A			$V_{CC2}+1.4$	$V_{CC2}+2$	V
		$I_{OK} = 1$ A			$V_{CC2}+1.9$	$V_{CC2}+2.5$	
V_{OKL}‡	Low-level output clamp voltage	$I_{OK} = 0.5$ A			−1.1	−2	V
		$I_{OK} = -1$ A			−1.3	−2.5	
I_{OZ}	Off-state (high-impedance state) output current	$V_O = V_{CC2}$				500	μA
		$V_O = 0$				−500	
I_{IH}	High-level input current	$V_I = 5.5$ V				10	μA
I_{IL}	Low-level input current	$V_I = 0$				−10	μA
I_{CC1}	Logic supply current	$I_O = 0$	All outputs at high level			38	mA
			All outputs at low level			70	
			All outputs at high impedance			25	
I_{CC2}	Output supply current	$I_O = 0$	All outputs at high level			33	mA
			All outputs at low level			20	
			All outputs at high impedance			5	

† All typical values are at $V_{CC1} = 5$ V, $V_{CC2} = 24$ V, $T_A = 25°C$.
‡ Valid for SN754410 only

switching characteristics, $V_{CC1} = 5$ V, $V_{CC2} = 24$ V, $C_L = 30$ pF, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output from A input	See Figure 1		800		ns
t_{DHL}	Delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns
t_{PZH}	Enable time to the high level	See Figure 2		700		ns
t_{PZL}	Enable time to the low level			400		ns
t_{PHZ}	Disable time from the high level			900		ns
t_{PLZ}	Disable time from the low level			600		ns

PARAMETER MEASUREMENT INFORMATION

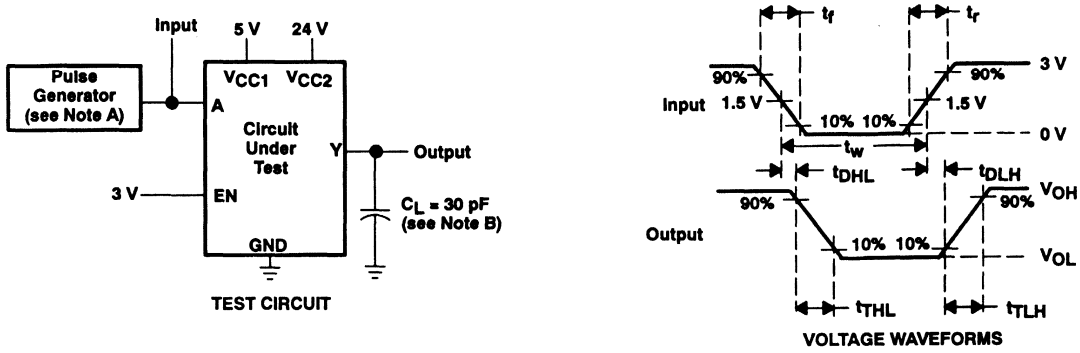


Figure 1. Test Circuit and Switching Times From Data Inputs

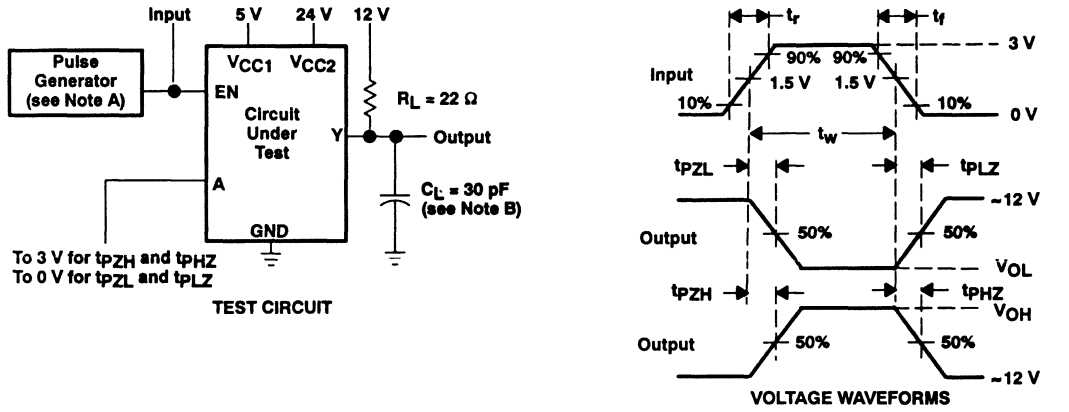


Figure 2. Test Circuit and Switching Times From Enable Inputs

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10$ µs, PRR = 5 kHz, $Z_O = 50$ Ω.
B. C_L includes probe and jig capacitance.

APPLICATION INFORMATION

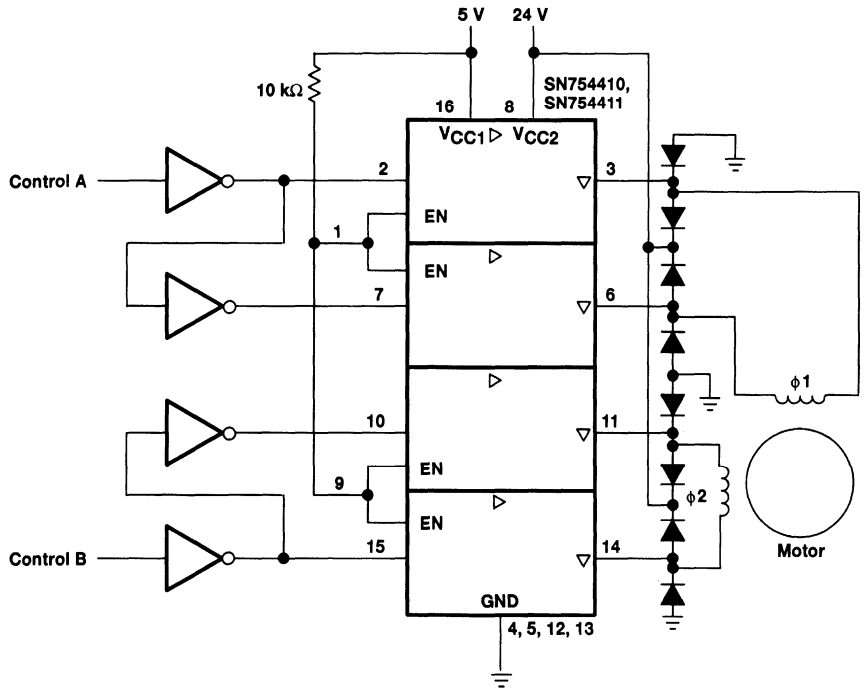


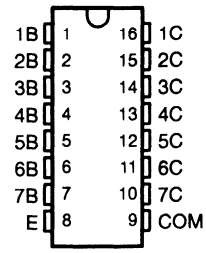
Figure 3. Two-Phase Motor Driver

SLDS036A – D2624, DECEMBER 1976 – REVISED APRIL 1993

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay Driver Applications**
- **Designed to Be Interchangeable With Sprague ULN2001A Series**

D OR N PACKAGE
(TOP VIEW)

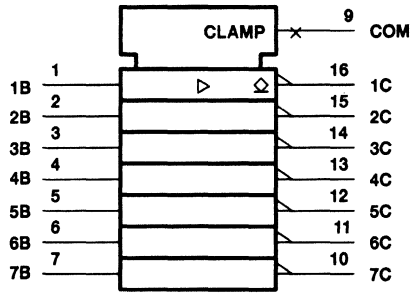


description

The ULN2001A, ULN2002A, ULN2003A, and ULN2004A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions, see the SN75465 through SN75469.

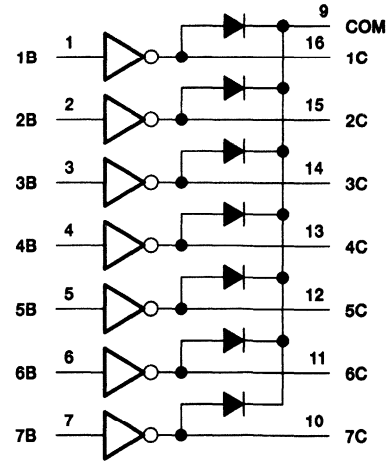
The ULN2001A is a general-purpose array and can be used with TTL, P-MOS, CMOS, and other MOS technologies. The ULN2002A is specifically designed for use with 14- to 25-V P-MOS devices. Each input of this device has a zener diode and resistor in series to control the input current to a safe limit. The ULN2003A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A has a 10.5-kΩ series base resistor to allow its operation directly from CMOS or P-MOS devices that use supply voltages of 6 to 15 V. The required input current of the ULN2004A is below that of the ULN2003A, and the required voltage is less than that required by the ULN2002A.

logic symbol†

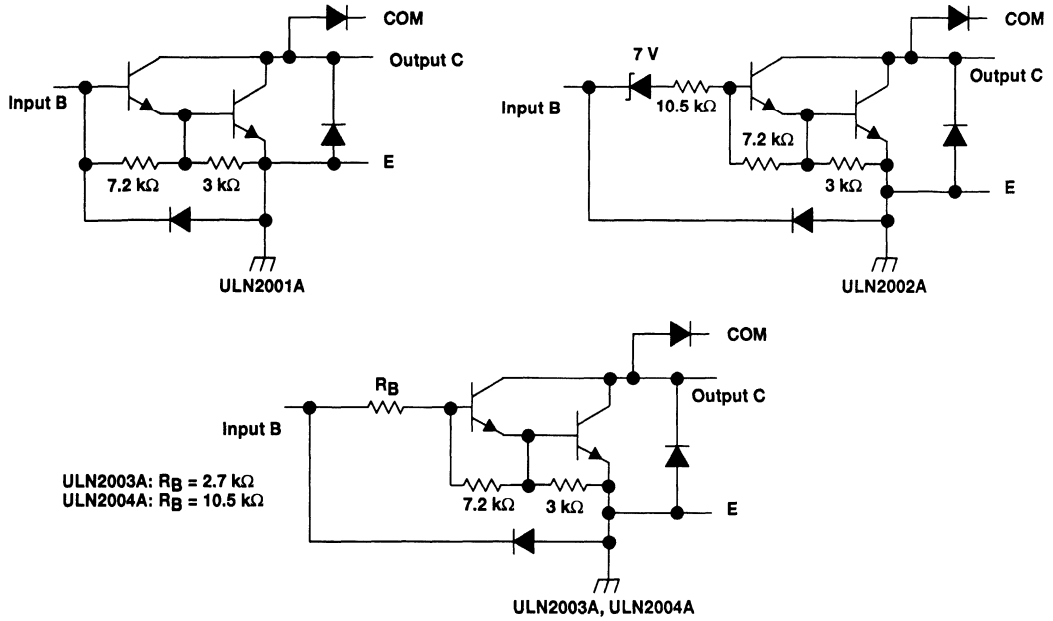


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage	50 V
Input voltage, V_I (see Note 1)	30 V
Peak collector current (see Figures 14 and 15)	500 mA
Output clamp current, I_{OK}	500 mA
Total emitter-terminal current	−2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	−20°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2001A			ULN2002A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V,	I_C = 300 mA						13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
V_F	Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	µA
			V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
		2		V_I = 6 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 17 V						0.82	1.25	mA
I_R	Clamp reverse current	7	V_R = 50 V,	T_A = 70°C			100			100	µA
h_{FE}	Static forward current transfer ratio	5	V_{CE} = 2 V,	I_C = 350 mA	1000						
I_R	Clamp reverse current	7	V_R = 50 V				50			50	µA
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2003A			ULN2004A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V	I_C = 125 mA						5	V
				I_C = 200 mA			2.4			6	
				I_C = 250 mA			2.7				
				I_C = 275 mA						7	
				I_C = 300 mA			3				
				I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 µA,	I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 µA,	I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 µA,	I_C = 350 mA		1.2	1.6		1.2	1.6	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V,	I_I = 0			50			50	µA
			V_{CE} = 50 V, T_A = 70°C	I_I = 0			100			100	
		2		V_I = 1 V						500	
V_F	Clamp forward voltage	8	I_F = 350 mA			1.7	2		1.7	2	V
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 µA,	50	65		50	65		µA
I_I	Input current	4	V_I = 3.85 V			0.93	1.35				mA
			V_I = 5 V						0.35	0.5	
			V_I = 12 V						1	1.45	
I_R	Clamp reverse current	7	V_R = 50 V				50			50	µA
			V_R = 50 V,	T_A = 70°C			100			100	
C_i	Input capacitance		V_I = 0,	f = 1 MHz		15	25		15	25	pF

switching characteristics, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 9		0.25	1	µs
t_{PHL}	Propagation delay time, high-to-low-level output			0.25	1	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, See Figure 10	V_S–20			mV

PARAMETER MEASUREMENT INFORMATION

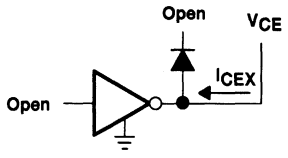


Figure 1. I_{CEX} Test Circuit

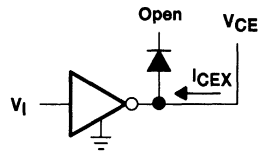


Figure 2. I_{CEX} Test Circuit

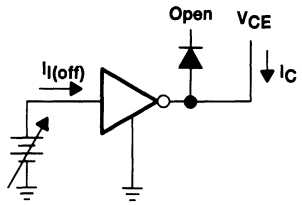


Figure 3. $I_{I(off)}$ Test Circuit

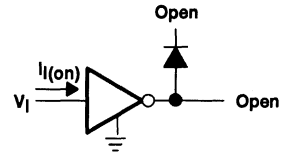
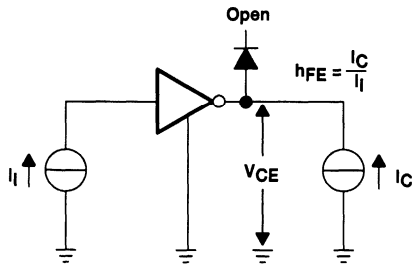


Figure 4. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 5. h_{FE}, $V_{CE(sat)}$ Test Circuit

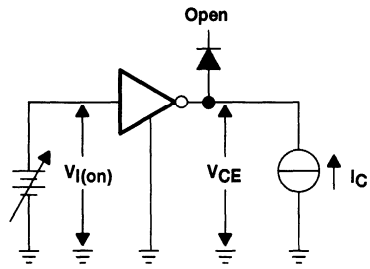


Figure 6. $V_{I(on)}$ Test Circuit

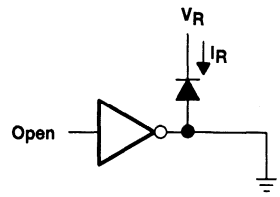


Figure 7. I_R Test Circuit

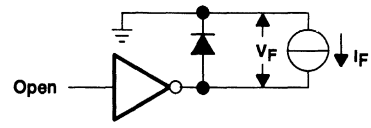


Figure 8. V_F Test Circuit

PARAMETER MEASUREMENT INFORMATION

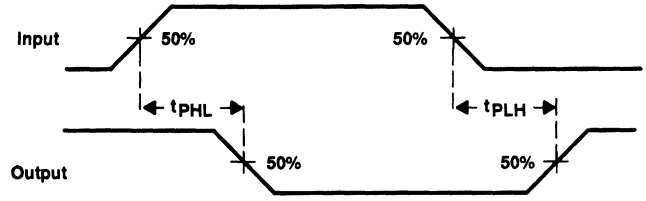
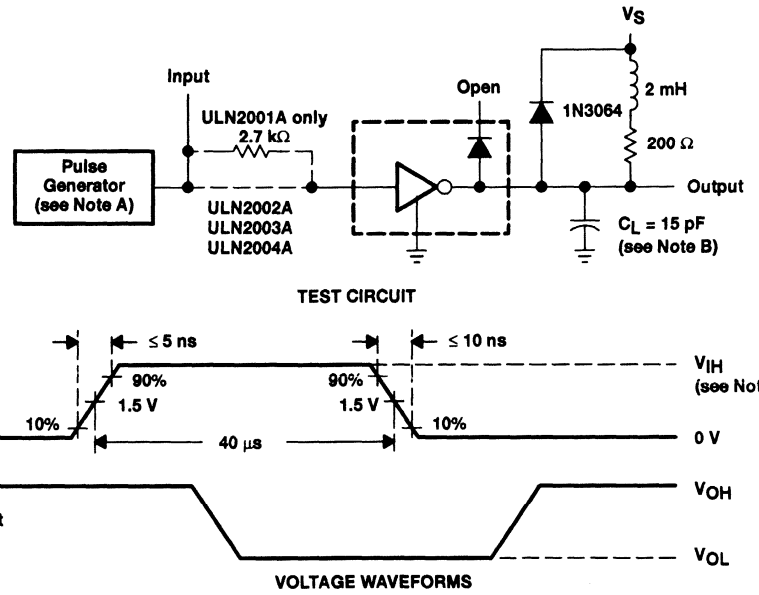


Figure 9. Propagation Delay Time Waveforms



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the ULN2001A and the ULN2003A, V_{IH} = 3 V; for the ULN2002A, V_{IH} = 13 V; for the ULN2004A, V_{IH} = 8 V.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

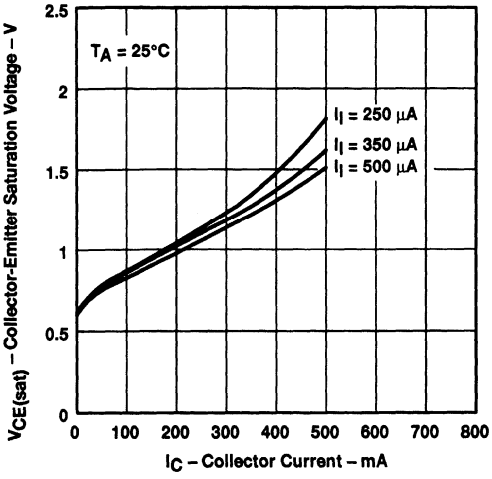


Figure 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs TOTAL COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

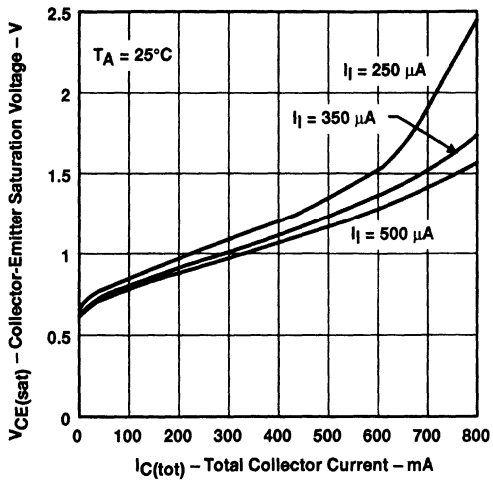


Figure 12

COLLECTOR CURRENT vs INPUT CURRENT

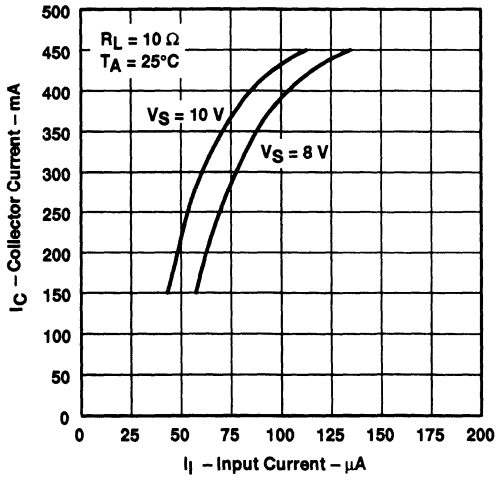


Figure 13

THERMAL INFORMATION

D PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

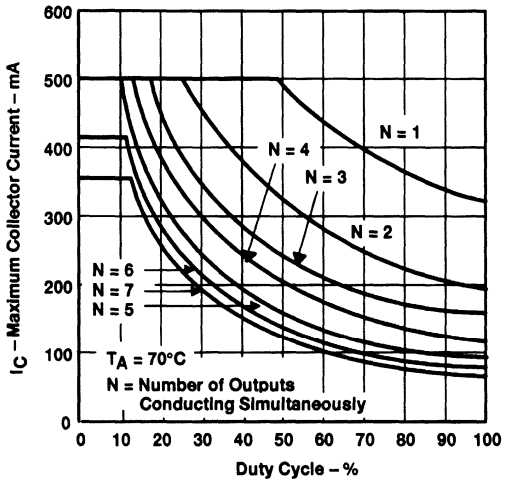


Figure 14

N PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

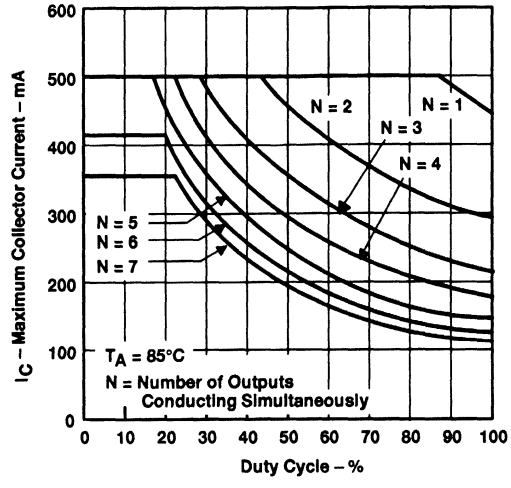


Figure 15

APPLICATION INFORMATION

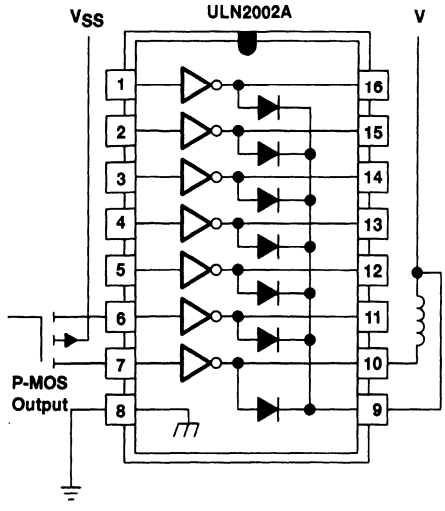


Figure 16. P-MOS to Load

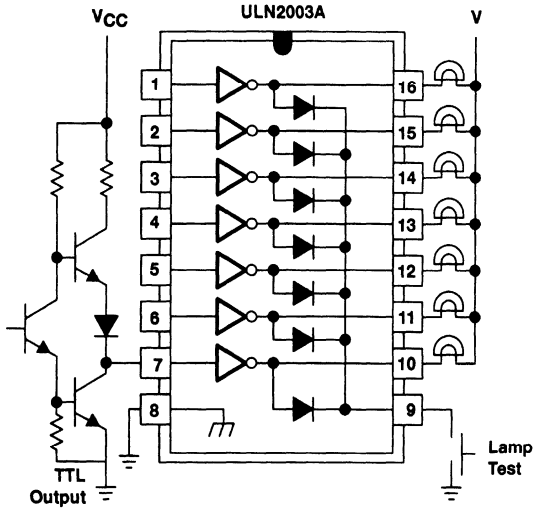


Figure 17. TTL to Load

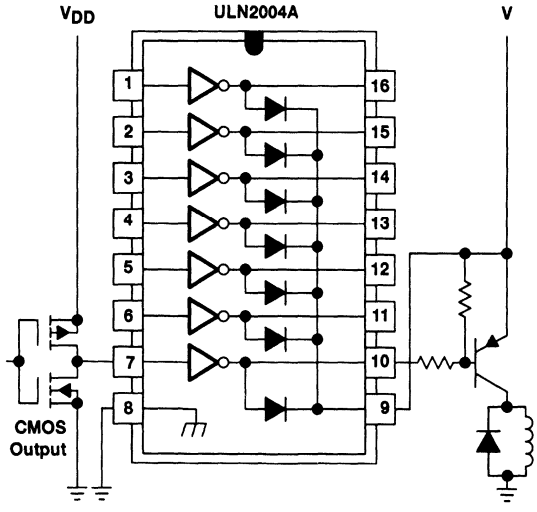


Figure 18. Buffer for Higher Current Loads

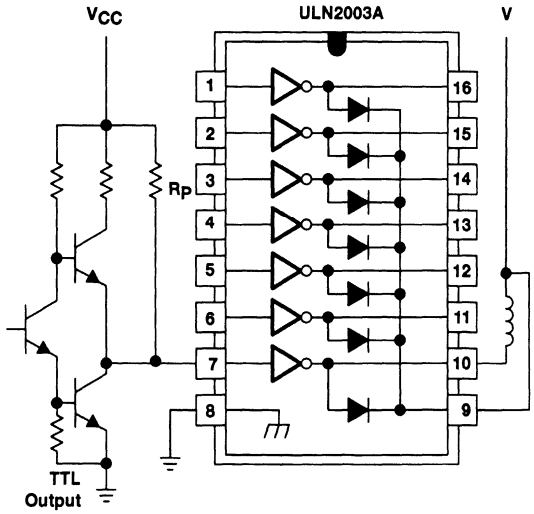


Figure 19. Use of Pullup Resistors to Increase Drive Current

SLDS039 – D2580, MAY 1980 – REVISED SEPTEMBER 1986

- **Output Collector Current . . . 1.5 A Max**
- **2-W Dissipation Rating**
- **High Output-Voltage Capability**
- **Output Sink- or Source-Current Capabilities**
- **Input Compatible With TTL or 5-V CMOS**
- **Designed for Interchangeability With Sprague ULN2074 and ULN2075**

description

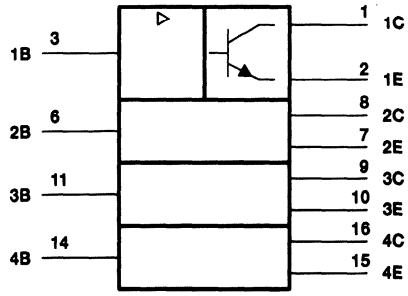
The ULN2074 and ULN2075 are monolithic, quadruple, high-voltage, high-current npn darlington-transistor amplifier devices. They feature high-voltage outputs with collector-current ratings of 1 .5 A for each Darlington pair.

The ULN2074 and ULN2075 are unique general-purpose devices, each featuring uncommitted collectors and emitters to allow for either sinking or sourcing the output current. These devices offer the system designer the flexibility of tailoring the circuit to the application. Typical applications include logic buffers, relay drivers, lamp drivers, and hammer drivers.

For proper operation, the SUBSTRATE must be connected to the most negative voltage.

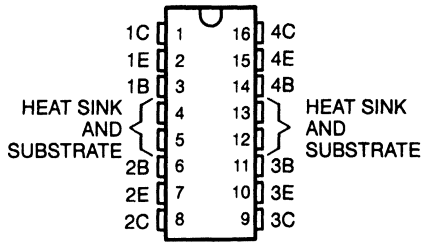
The ULN2074 and ULN2075 are characterized for operation from –20°C to 85°C.

logic symbol†

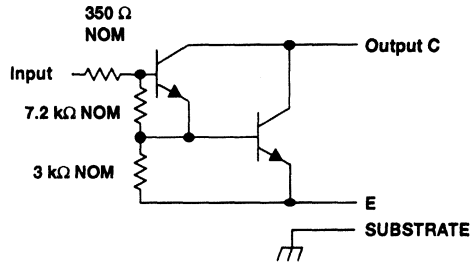


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NE PACKAGE
(TOP VIEW)



schematic (each switch)



SLDS039 – D2580, MAY 1980 – REVISED SEPTEMBER 1986

absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	ULN2074	ULN2075	UNIT
Collector-emitter voltage	50	80	V
Input voltage with respect to SUBSTRATE	30	60	V
Peak voltage with respect to SUBSTRATE (see Figures 9, 10, and 11)	1.5	1.5	A
Input current	25	25	mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 1)	2075	2075	mW
Operating free-air temperature range	−20 to 85	−20 to 85	°C
Storage temperature range	−55 to 150	−55 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	260	°C

NOTE 1: For operation above 25°C free-air temperature, derate total power linearly to 1079 mW at 85°C at the rate of 16.6 mW/°C.

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		ULN2074		ULN2075		UNIT
					MIN	MAX	MIN	MAX	
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V,	I_C = 100 mA	35		50		V
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V,	I_C = 1 A		2		2	V
			V_{CE} = 2 V, See Note 2	I_C = 1.5 A,		2.5		2.5	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 625 μA,	I_C = 500 mA		1.1		1.1	V
			I_I = 935 μA,	I_C = 750 mA		1.2		1.2	
			I_I = 1.25 mA,	I_C = 1 A		1.3		1.3	
			I_I = 2 mA, See Note 2	I_C = 1.25 A,		1.4			
			I_I = 2.25 mA, See Note 2	I_C = 1.5 A,				1.5	
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V			100			μA
			V_{CE} = 50 V,	T_A = 70°C		500			
			V_{CE} = 80 V					100	
			V_{CE} = 80 V,	T_A = 70°C				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V		2	4.3	2	4.3	mA
			V_I = 3.75 V		4.5	9.6	4.5	9.6	

NOTE 2: These parameters must be measured on one output at a time using pulse techniques, t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6		1	μs
t_{PHL}	Propagation delay time, high-to-low-level output			1.5	μs

PARAMETER MEASUREMENT INFORMATION

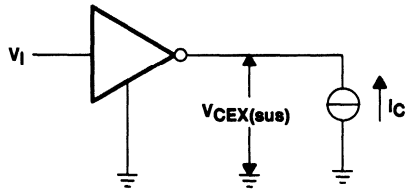


Figure 1. $V_{CEX(sus)}$ Test Circuit

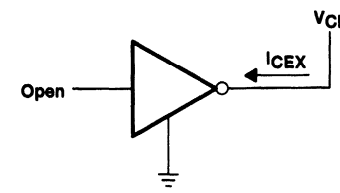


Figure 2. I_{CEX} Test Circuit

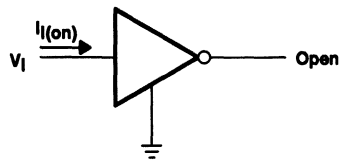


Figure 3. $I_{I(on)}$ Test Circuit

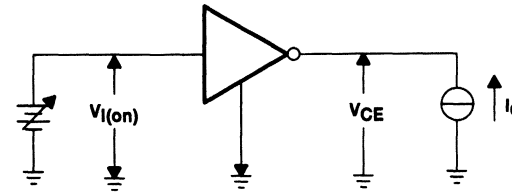


Figure 4. $V_{I(on)}$ Test Circuit

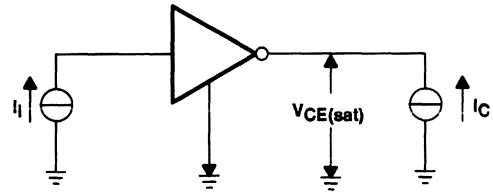
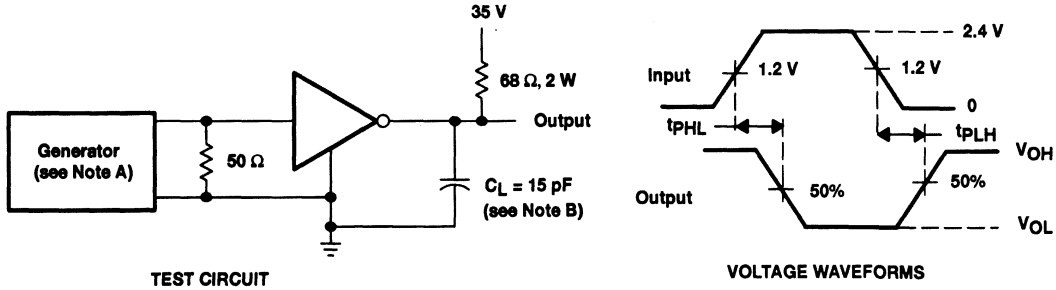


Figure 5. $V_{CE(sat)}$ Test Circuit



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_O = 50 Ω.
B. C_L includes all probe and stray capacitance.

Figure 6. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

INPUT CURRENT vs INPUT VOLTAGE

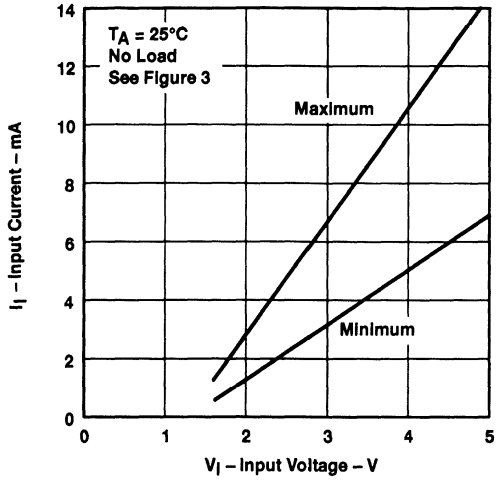


Figure 7

COLLECTOR CURRENT vs BASE CURRENT

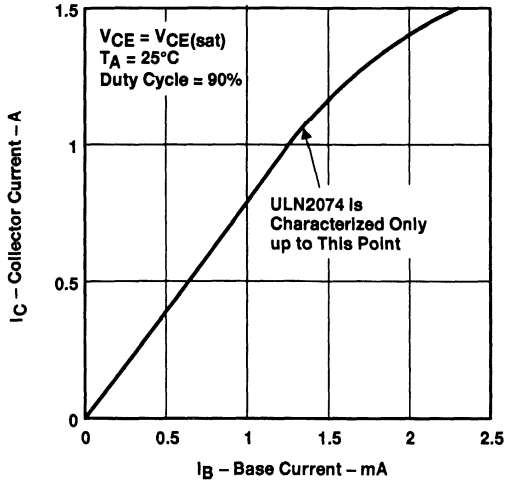


Figure 8

THERMAL INFORMATION

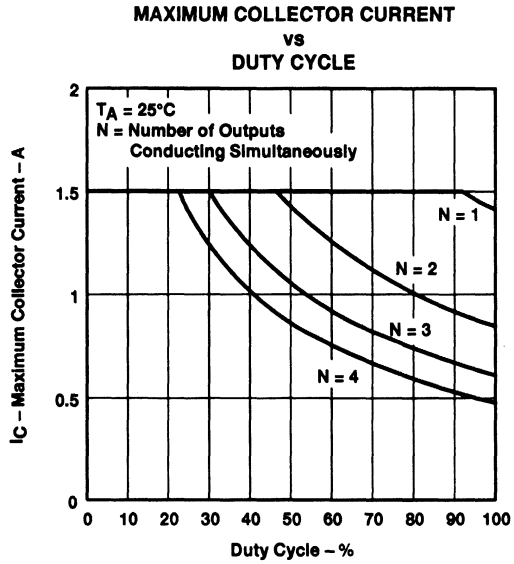


Figure 9

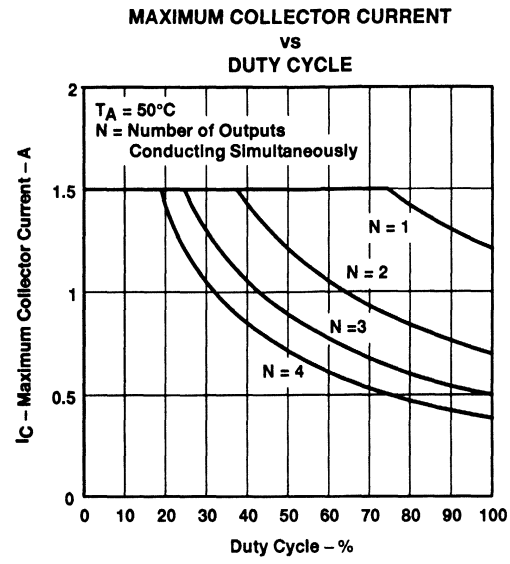


Figure 10

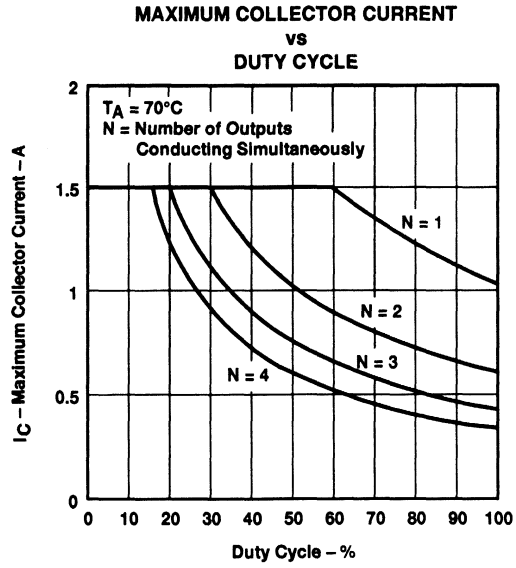


Figure 11

APPLICATION INFORMATION

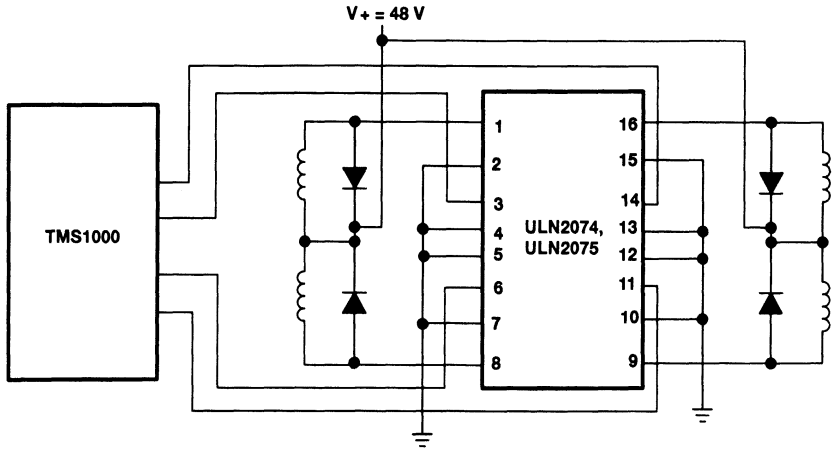


Figure 12. Relay Driver Interface With External Clamp Diodes

4 Display Drivers

SLDS013B – D2471, DECEMBER 1985 – REVISED MAY 1993

- **Controls 32 Electrodes**
- **100-V Totem-Pole Outputs**
- **Low Standby Power Consumption**
- **All Outputs Contain Sink and Source Clamp Diodes**
- **15-mA Steady-State Output Current**
- **Rugged DMOS Outputs**
- **CMOS Inputs**
- **Direct Replacement for SN55500D and SN75500A**

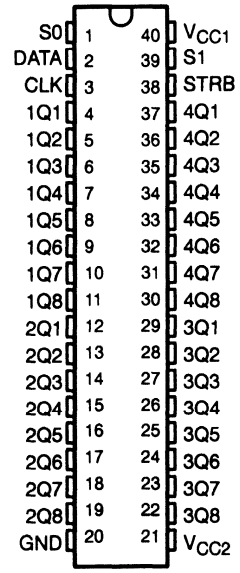
description

The SN55500E, SN65500E, and SN75500E are monolithic BIDFET† integrated circuits designed to perform the line-select operation of a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

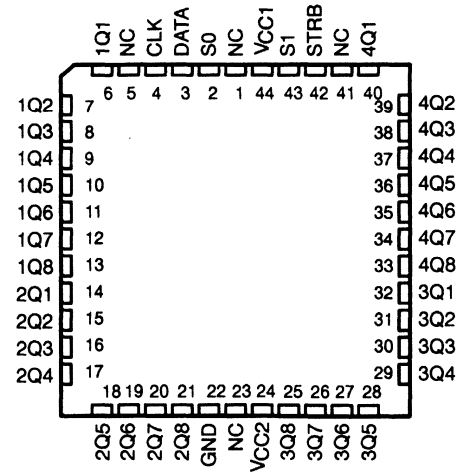
The outputs of these drivers are normally low and can be selectively switched high when the strobe input is low. Selection of the outputs is achieved through the data S0 and S1 inputs. The 8-bit data stored internally in the serial register is inverted and sent to one of four output sections by the 2-line to 4-line decoder. All other outputs remain low. Internal circuits provide a high-current pulse to the level-shifting circuit during positive output transitions. When the output transition is complete, the low steady-state current reduces the circuit's standby power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55500E is characterized for operation over the full military temperature range of −55°C to 125°C. The SN65500E is characterized for operation from −40°C to 85°C. The SN75500E is characterized for operation from 0°C to 70°C.

SN55500E . . . J PACKAGE
SN65500E, SN75500E . . . N PACKAGE
(TOP VIEW)



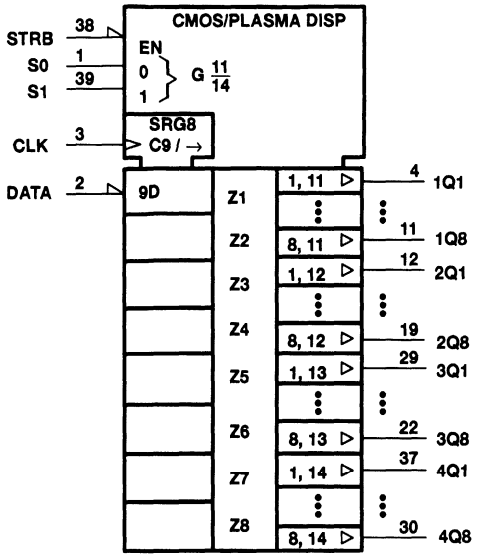
SN55500E . . . FD OR FJ PACKAGE
SN65500E, SN75500E . . . FN PACKAGE
(TOP VIEW)



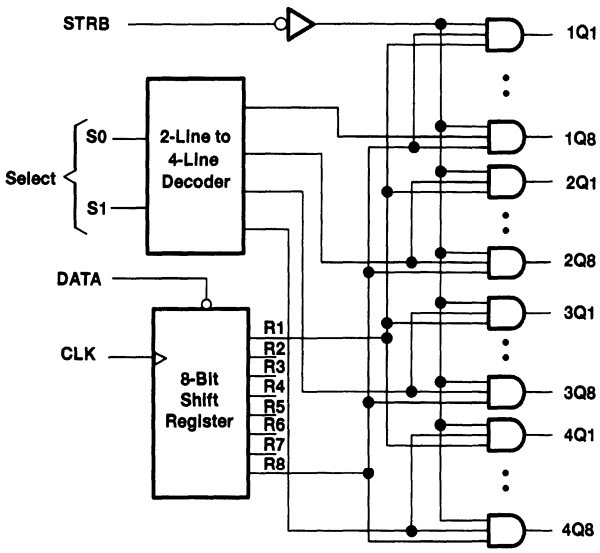
NC – No internal connection

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbol†



functional block diagram (positive logic)



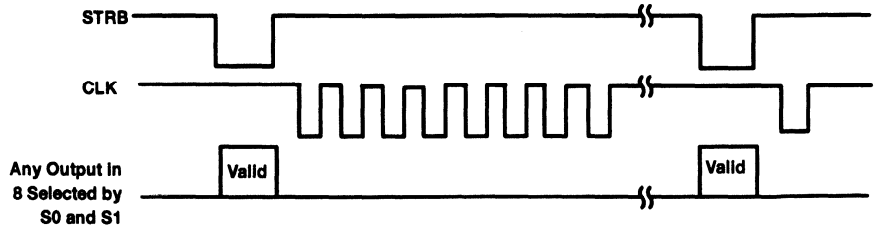
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J and N packages.

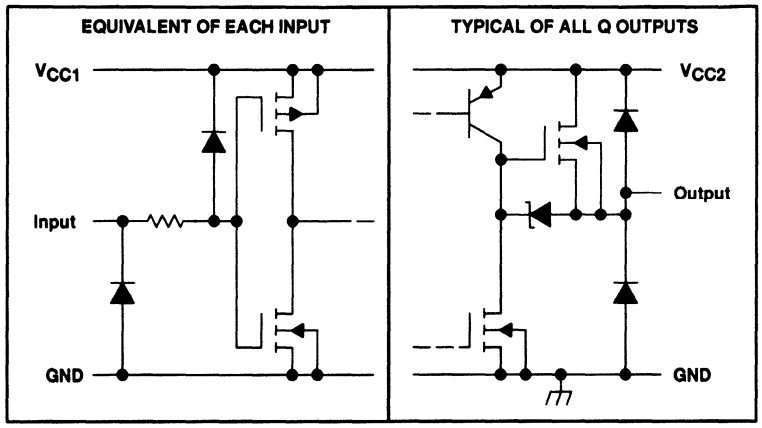
FUNCTION TABLE

FUNCTION	INPUTS					OUTPUTS						
	DATA	CLK	SELECT S1	SELECT S0	STRB	SHIFT REGISTER R1	SHIFT REGISTER R2	SHIFT REGISTER R3 . . . R8	1Q1 . . . 1Q8	2Q1 . . . 2Q8	3Q1 . . . 3Q8	4Q1 . . . 4Q8
Load	H	↑	X	X	H	L	$R1_n$	$R2_n$ . . . $R7_n$	L . . . L	L . . . L	L . . . L	L . . . L
	L	↑	X	X	H	H	$R1_n$	$R2_n$ . . . $R7_n$	L . . . L	L . . . L	L . . . L	L . . . L
Strobe	X	X	X	X	H	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	L . . . L	L . . . L	L . . . L
	X	H	L	L	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	R1 . . . R8	L . . . L	L . . . L	L . . . L
	X	H	L	H	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	R1 . . . R8	L . . . L	L . . . L
	X	H	H	L	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	L . . . L	R1 . . . R8	L . . . L
	X	H	H	H	L	$R1_n$	$R2_n$	$R3_n$ . . . $R8_n$	L . . . L	L . . . L	L . . . L	R1 . . . R8

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1 . . . R8 = levels currently at internal outputs of shift registers one through eight, respectively.
$R1_n$ . . . $R8_n$ = levels at shift-register outputs R1 through R8, respectively, before the most recent ↑ transition of the clock.

typical operating sequence





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1): SN55500E ..... 13.8 V
SN65500E, SN75500E ..... 15 V
Supply voltage, V_{CC2} ..... 100 V
Input voltage ..... V_{CC1} + 0.3 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN55500E ..... −55°C to 125°C
SN65500E ..... −40°C to 85°C
SN75500E ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C
Case temperature for 60 seconds: FD or FJ package ..... 260°C
Case temperature for 10 seconds: FN package ..... 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FD or FJ	1825 mW	14.6 mW/°C	1168 mW	949 mW	365 mW
FN	1775 mW	14.2 mW/°C	1136 mW	923 mW	—
J	3050 mW	24.4 mW/°C	1952 mW	1586 mW	610 mW
N	1275 mW	10.2 mW/°C	816 mW	663 mW	—

recommended operating conditions

		SN55500E			SN65500E			SN75500E			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC1}		10.8	12	13.2	10.8	12	13.2	10.8	12	13.2	V
Supply voltage, V_{CC2}		0		100	0		100	0		100	V
High-level input voltage as a percentage of V_{CC1}, V_{IH}		75%			75%			75%			
Low-level input voltage as a percentage of V_{CC1}, V_{IL}				25%			25%			25%	
High-level output clamp current				20			20			20	mA
Low-level output clamp current				−20			−20			−20	mA
Clock frequency, f_{clock} (see Figure 2)		0		8	0		8	0		8	MHz
Duration of high or low clock pulse, t_w		62			62			62			ns
Setup time, t_{su}	Data inputs before CLK↑	20			20			20			ns
	Select inputs before STRB↓	50			50			50			
Hold time, t_h	Data inputs after CLK↑ (see Note 2)	50			50			50			ns
	Strobe input high after CLK↑	50			50			50			
	Select inputs after STRB↑	50			50			50			
Operating free-air temperature, T_A		−55			−40		85	0		70	°C
Operating case temperature, T_C				125							°C

NOTE 2: For operation above 25°C junction temperature, refer to Figure 2.

electrical characteristics over recommended operating free-air temperature range

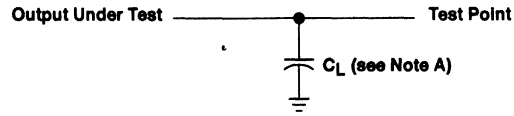
PARAMETER		TEST CONDITIONS		SN55500E			SN65500E			SN75500E			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp voltage	V_{CC1} = 12 V,	I_I = −12 mA		−1	−1.5		−1	−1.5		−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		94	97.5		95	97.5		V
			I_{OH} = −10 mA	92	94.5		92	94.5		93	94.5		
			I_{OH} = −15 mA	90	93.5		90	93.5		91	93.5		
V_{OL}	Low-level output voltage	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2		0.85	2	V
			I_{OL} = 10 mA		2	4		2	4		2	4	
			I_{OL} = 15 mA		2.75	5		2.75	5		2.75	5	
V_{OK}	Output clamp voltage	V_{CC2} = 0	I_O = 20 mA		1	2.5		1	2.5		1	2.5	V
			I_O = −20 mA		−1.2	−2.5		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High-level input current	V_{CC1} = 13.2 V,	V_I = V_{IH} min			1			1			1	μA
I_{IL}	Low-level input current	V_{CC1} = 13.2 V,	V_I = V_{IL} max			−1			−1			−1	μA
I_{CC1}	Supply current	V_{CC1} = 13.2 V,	V_{CC2} = 100 V		0.05	1		0.05	1		0.05	1	mA
I_{CC2}	Supply current	V_{CC2} = 100 V			1	5		1	5		1	3	mA

† All typical values are at V_{CC1} = 12 V, T_A = 25°C.

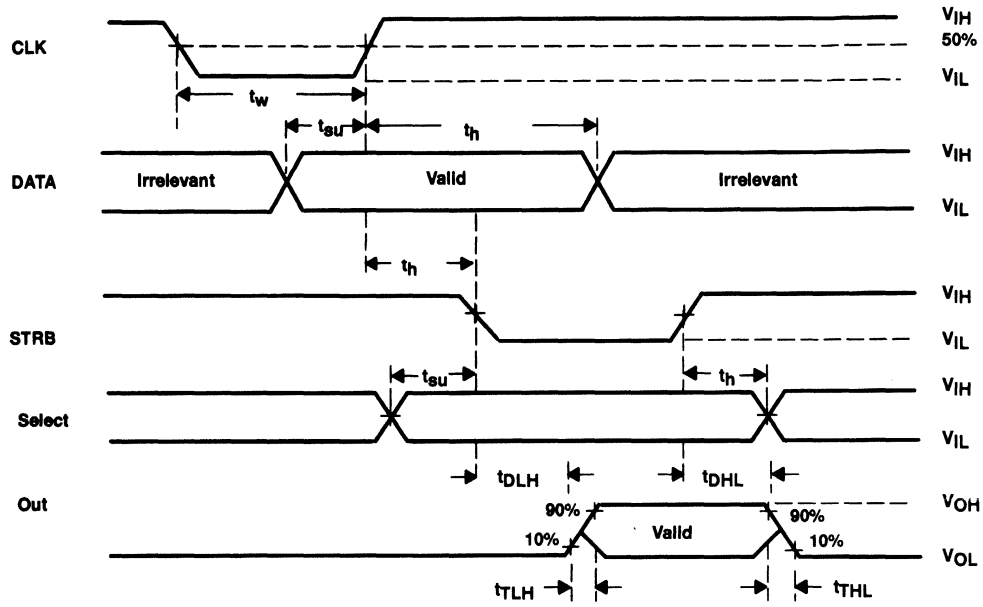
switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level output from strobe input	C_L = 30 pF, See Figure 1		250	ns
t_{DLH}	Delay time, low-to-high-level output from strobe input			450	ns
t_{THL}	Transition time, high-to-low-level output			200	ns
t_{TLH}	Transition time, low-to-high-level output			300	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A. C_L includes probe and jig capacitance.

Figure 1. Load Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

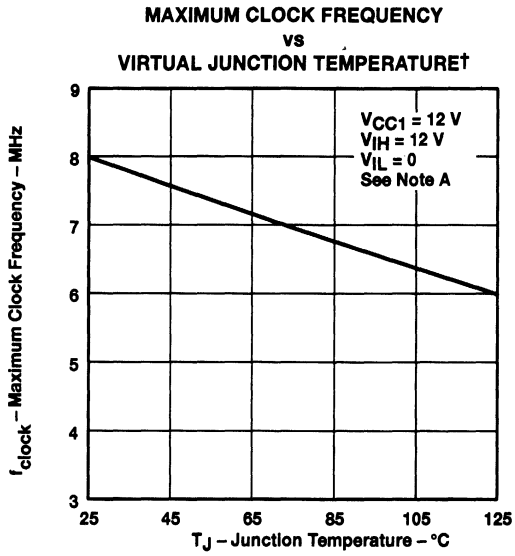


Figure 2

† Only the 25°C to 70°C portion of the curve applies to the SN75500E.
NOTE A: This curve assumes a symmetrical clock pulse.

THERMAL INFORMATION

junction temperature formula

$$T_J = T_A + P_D R_{\theta JA}$$

$$T_J = T_C + P_D R_{\theta JC}$$

where

T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

PACKAGE TYPE	$R_{\theta JA}$	$R_{\theta JC}$
FD 44-pin ceramic	68°C/W	20°C/W
FN 44-pin plastic	70°C/W	22°C/W
J 40-pin ceramic	45°C/W	12°C/W
N 40-pin plastic	97°C/W	27°C/W

SLDS012B – D2472, MARCH 1983 – REVISED APRIL 1993

- **Controls 32 Electrodes**
- **100-V Totem-Pole Outputs**
- **Low Standby Power Consumption**
- **All Outputs Contain Sink and Source Clamp Diodes**
- **15-mA Steady-State Output Current**
- **Rugged DMOS Outputs**
- **CMOS Inputs**
- **Direct Replacement for SN75501C**

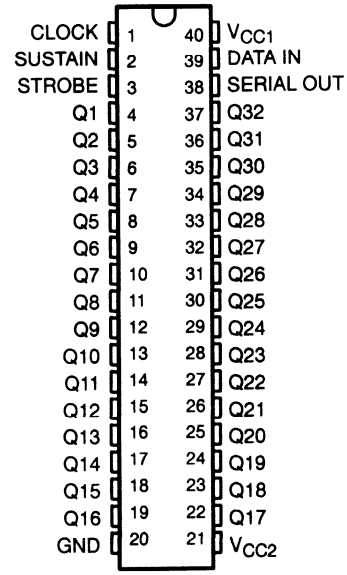
description

The SN55501E, SN65501E, and SN75501E are monolithic BIDFET† integrated circuits designed to provide the serial-to-parallel conversion and level translation of data in a matrix-addressable display. The device inputs are diode-clamped CMOS inputs.

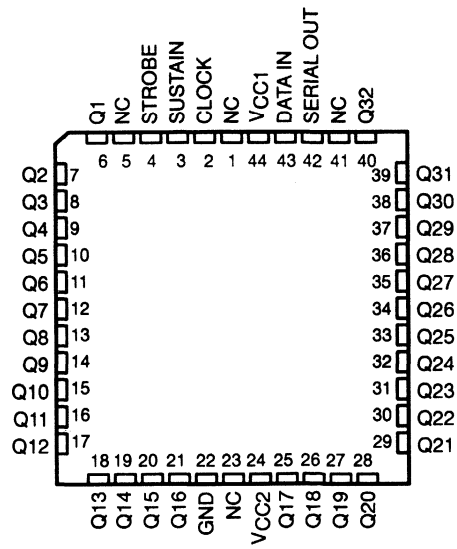
The Q outputs of these drivers are normally high and can be switched either selectively or together. Any output whose associated register bit (in the internal 32-bit serial register) contains a low switches low when STROBE is low if SUSTAIN is high. All other outputs remain high. When SUSTAIN is low, all outputs switch low independently of the data or strobe inputs. This feature can be used to generate a portion of the SUSTAIN pulse required in the operation of an ac plasma display. The internal level-shift circuits provide additional drive during the times that the outputs switch high to facilitate fast rise times while maintaining low standby power consumption. All outputs contain clamp diodes to the V_{CC2} and GND supply inputs.

The SN55501E is characterized for operation over the full military temperature range of −55°C to 125°C. The SN65501E is characterized for operation from −40°C to 85°C. The SN75501E is characterized for operation from 0°C to 70°C.

SN55501E . . . J PACKAGE
SN65501E, SN75501E . . . N PACKAGE
(TOP VIEW)



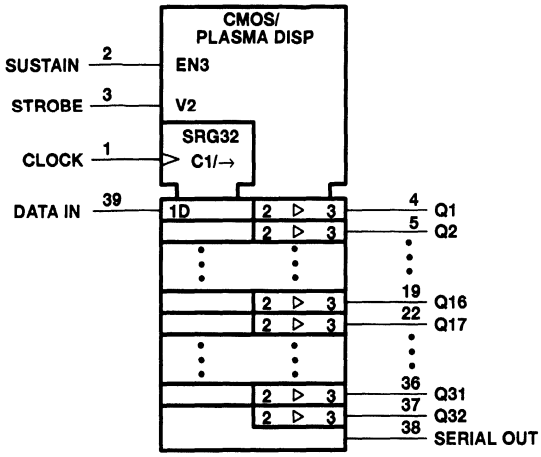
SN55501E . . . FD OR FJ PACKAGE
SN65501E, SN75501E . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

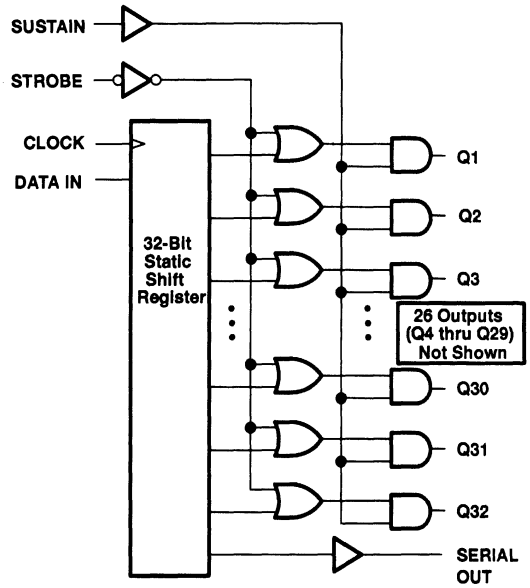
† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J and N packages.

functional block diagram (positive logic)

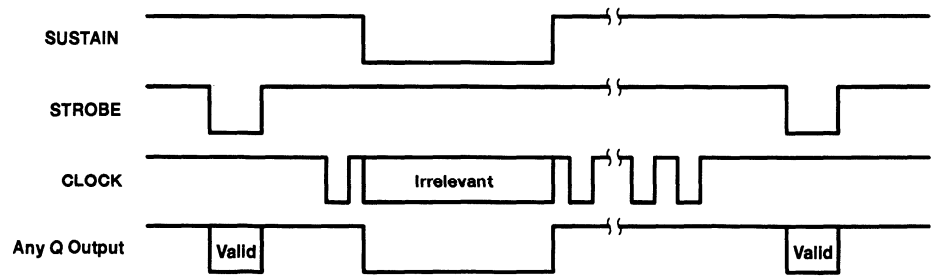


FUNCTION TABLE

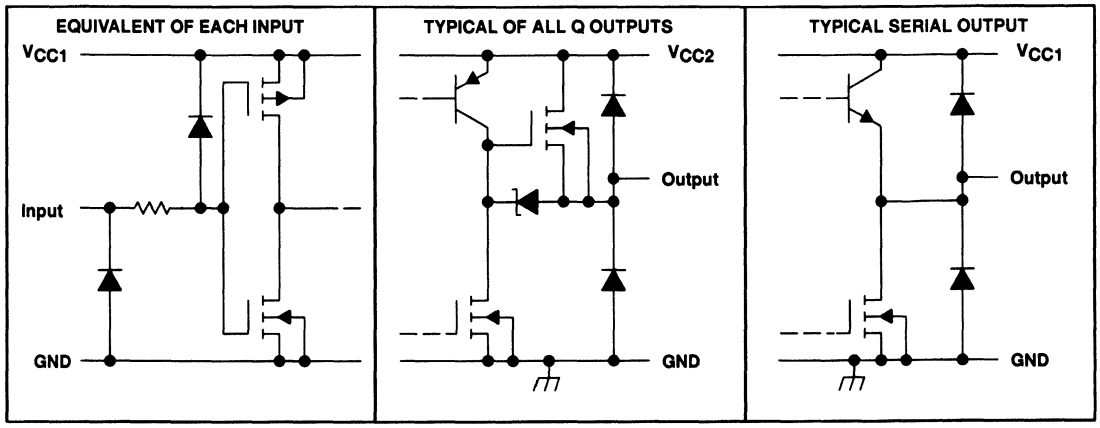
FUNCTION	INPUTS				OUTPUTS						
	DATA	CLOCK	STROBE	SUSTAIN	SHIFT REGISTERS R1	SHIFT REGISTERS R2	SHIFT REGISTERS R3 . . . R32	SERIAL DATA	Q1	Q2	Q3 . . . Q32
Load	H	↑	H	H	H	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . H
	L	↑	H	H	L	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	H	H	H . . . H
Strobe	X	X	H	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	H	H	H . . . H
	X	H	L	H	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	R1	R2	R3 . . . R32
Sustain	X	X	X	L	$R1_n$	$R2_n$	$R3_n$ . . . $R32_n$	$R32_n$	L	L	L . . . L

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
R1 . . . R32 = levels currently at internal outputs of shift registers one through thirty-two, respectively.
$R1_n$ . . . $R32_n$ = levels at shift-register outputs R1 through R32 respectively, before the most recent ↑ transition at the CLOCK input.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 15 V
Supply voltage, V_{CC2} ..... 100 V
Input voltage range ..... V_{CC1} to 0.3 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN55501E ..... −55°C to 125°C
SN65501E ..... −40°C to 85°C
SN75501E ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds: FD, FJ, or FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package ..... 300°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FD or FJ	1825 mW	14.6 mW/°C	1168 mW	949 mW	365 mW
FN	1775 mW	14.2 mW/°C	1136 mW	923 mW	—
J	3050 mW	24.4 mW/°C	1952 mW	1586 mW	610 mW
N	1275 mW	10.2 mW/°C	816 mW	663 mW	—

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}			10.8	12	13.2	V
Supply voltage, V_{CC2}			0		100	V
High-level input voltage, V_{IH}			0.75 V_{CC1}			V
Low-level input voltage, V_{IL}					0.25 V_{CC1}	V
High-level Q output clamp current, I_{OKH}					20	mA
Low-level Q output clamp current, I_{OKL}					−20	mA
Clock frequency at (or below) 25°C junction temperature , f_{clock} (see Note 2)			0		8	MHz
Duration of high or low clock pulse, t_w			62			ns
Setup time, t_{su}	Data inputs before CLOCK↑		20			ns
Hold time, t_h	Data inputs after CLOCK↑		50			ns
	STROBE high after CLOCK↑		150			
	STROBE high after SUSTAIN↑		250			
Operating free-air temperature, T_A		SN55501E	−55		125	°C
		SN65501E	−40		85	
		SN75501E	0		70	
Operating case temperature, T_C		SN55501E			125	°C

NOTE 2: See Figure 3 for maximum clock frequency when devices are operated in cascade or for operation above T_J = 25°C.

electrical characteristics over recommended operating free-air temperature range

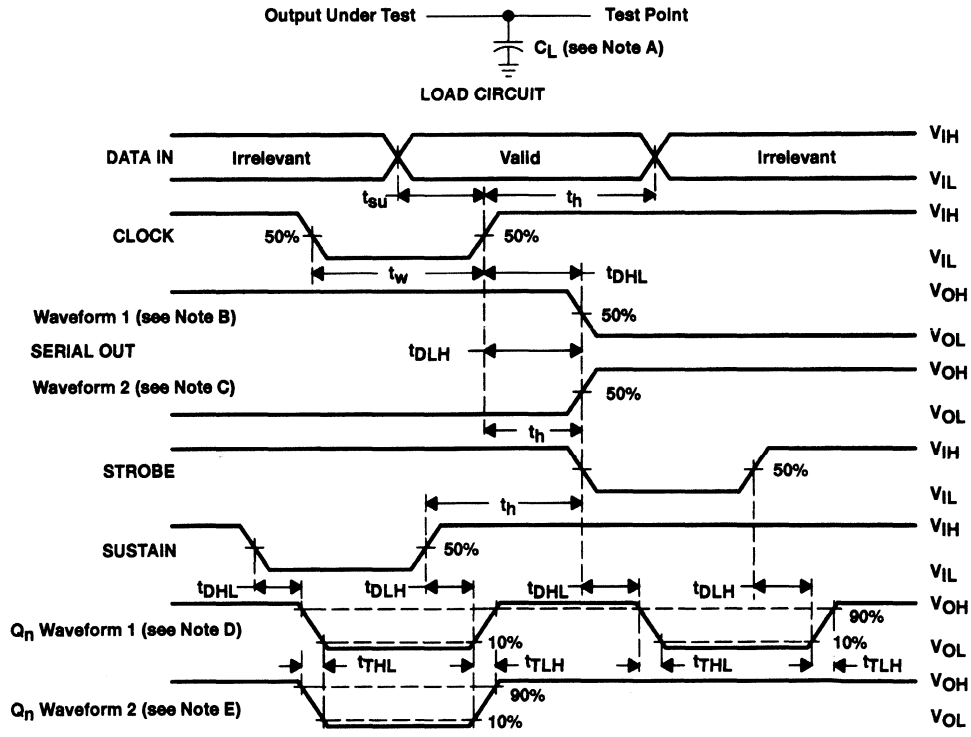
PARAMETER			TEST CONDITIONS		SN55501E, SN65501E			SN75501E			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp voltage		V_{CC1} = 12 V,	I_I = 12 mA		−1	−1.5		−1	−1.5	V
V_{OH}	High-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OH} = −1 mA	94	97.5		95	97.5		V
				I_{OH} = −10 mA	92	94.5		93	94.5		
				I_{OH} = −15 mA	90	93.5		91	93.5		
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OH} = −100 µA	9	10		9	10		
V_{OL}	Low-level output voltage	Q outputs	V_{CC1} = 13.2 V, V_{CC2} = 100 V	I_{OL} = 1 mA		0.85	2		0.85	2	V
				I_{OL} = 10 mA		2	4		2	4	
				I_{OL} = 15 mA		2.75	5		2.75	5	
		SERIAL OUT	V_{CC1} = 10.8 V,	I_{OL} = 100 µA		0.1	1		0.1	1	
V_{OK}	Output clamp voltage	Q outputs	V_{CC2} = 0	I_{OK} = 20 mA		1	2.5		1	2.5	V
				I_{OK} = −20 mA		−1.2	−2.5		−1.2	−2.5	
I_{IH}	High-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IH} = V_{IH}min,			1			1	µA
I_{IL}	Low-level input current		V_{CC1} = 13.2 V, V_{CC2} = 100 V	V_{IL} = V_{IL}max,			−1			−1	µA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 13.2 V,	V_{CC2} = 100 V		0.05	1		0.05	1	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC2} = 100 V			1	5		1	3	mA

† Typical values are at V_{CC1} = 12 V, T_A = 25°C.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 100 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DHL}	Delay time, high-to-low-level outputs	STROBE to Q outputs	C_L = 30 pF			250	ns
		SUSTAIN to Q outputs	C_L = 30 pF			250	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{DLH}	Delay time, low-to-high-level outputs	STROBE to Q outputs	C_L = 30 pF			450	ns
		SUSTAIN to Q outputs	C_L = 30 pF			450	
		CLOCK to SERIAL OUT	C_L = 20 pF			147	
t_{THL}	Transition time, high-to-low-level Q output		C_L = 30 pF			200	ns
t_{TLH}	Transition time, low-to-high-level Q output		C_L = 30 pF			300	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. SERIAL OUT waveform for internal conditions such that a low is registered in R32.
C. SERIAL OUT waveform for internal conditions such that a high is registered in R32.
D. Q_n output with a low stored in associated register R_n.
E. Q_n output with a high stored in associated register R_n.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

MAXIMUM CLOCK FREQUENCY
vs
JUNCTION TEMPERATURE

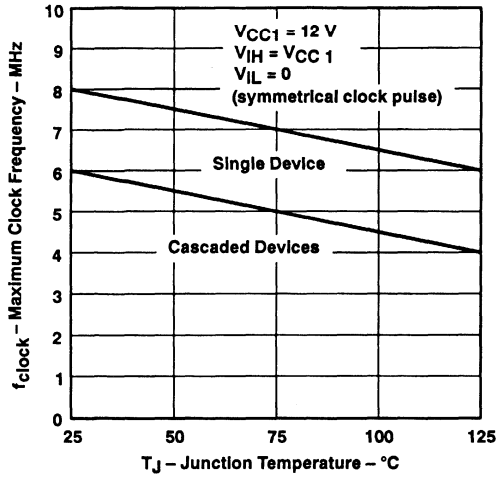


Figure 2

INPUT VOLTAGE LOGIC LEVEL LIMITS
vs
V_{CC1} SUPPLY VOLTAGE

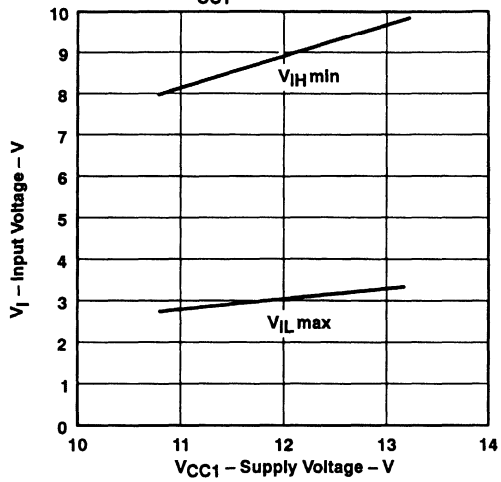


Figure 3

THERMAL CHARACTERISTICS

junction temperature formula

$$T_J = T_A + P_D R_\theta$$

where:

T_J = virtual junction temperature
T_A = free-air temperature
P_D = average device power dissipation
R_θ = thermal resistance (junction-to-air, $R_{\theta JA}$, or junction-to-case, $R_{\theta JC}$)

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$
FD or FJ	68°C/W	20°C/W
FN	70°C/W	22°C/W
J	45°C/W	12°C/W
N	100°C/W	27°C/W

SGLS003 – D2743, APRIL 1986

- **Each Device Drives 32 Electrodes**
- **High-Voltage Open-Drain DMOS Outputs**
- **50-mA Output Current Capability**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

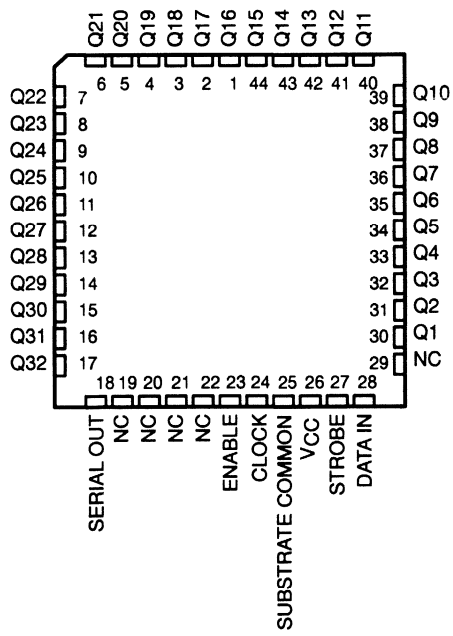
description

The SN55551 and SN55552 are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible, and all outputs are high-voltage open-drain DMOS transistors. The SN55552 output sequence is reversed from the SN55551 for ease in printed-circuit-board layout.

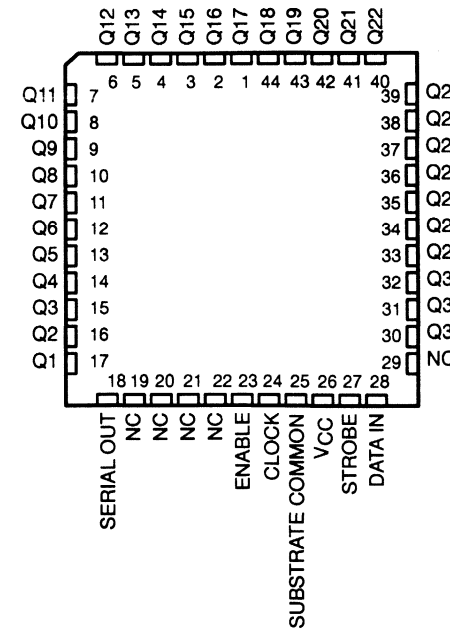
The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to SUBSTRATE COMMON. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at ENABLE allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The serial data output (SERIAL OUT) from the shift register may be used to cascade additional devices. This output is not affected by ENABLE or STROBE.

The SN55551 and SN55552 are characterized for operation over the full military temperature range of −55°C to 125°C.

SN55551 . . . FD PACKAGE
(TOP VIEW)



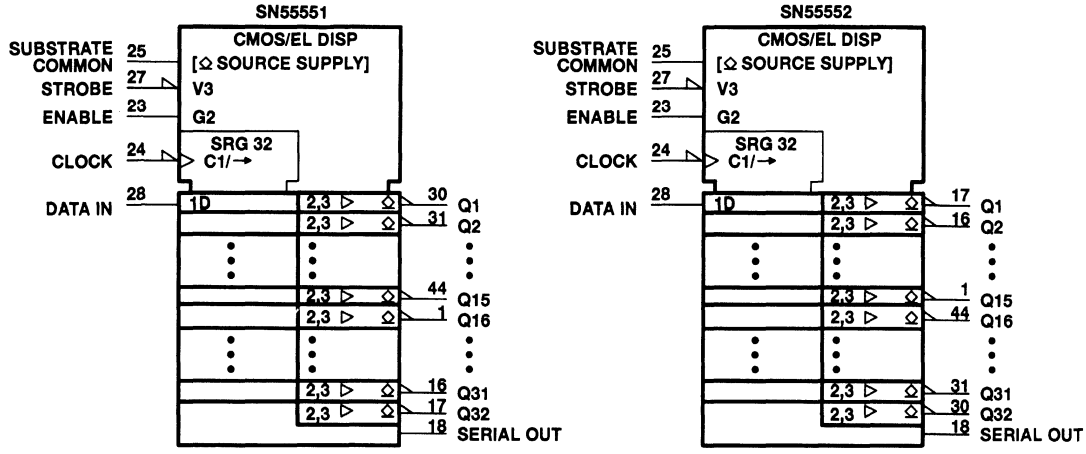
SN55552 . . . FD PACKAGE
(TOP VIEW)



NC – No internal connection

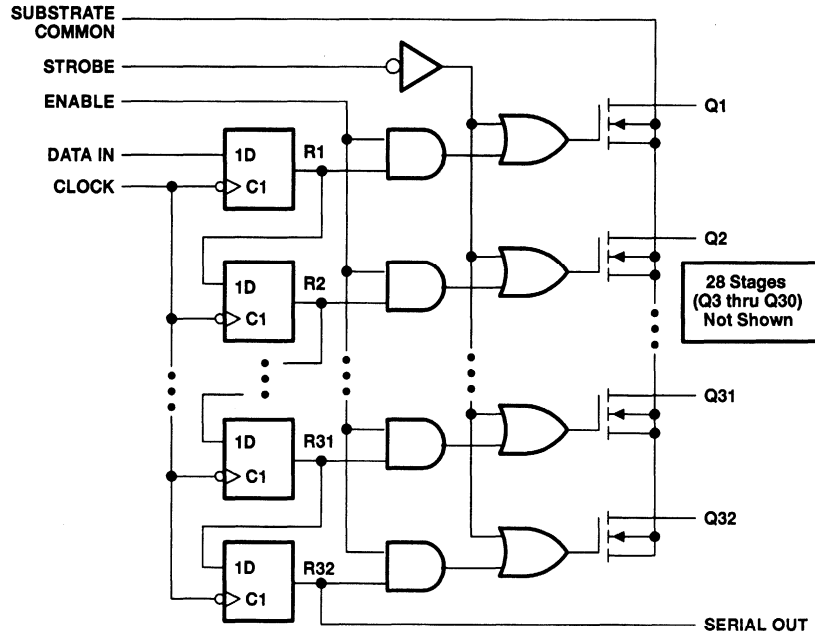
† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The symbol ⏢ here indicates an n-channel open-drain output.

logic diagram (positive logic)



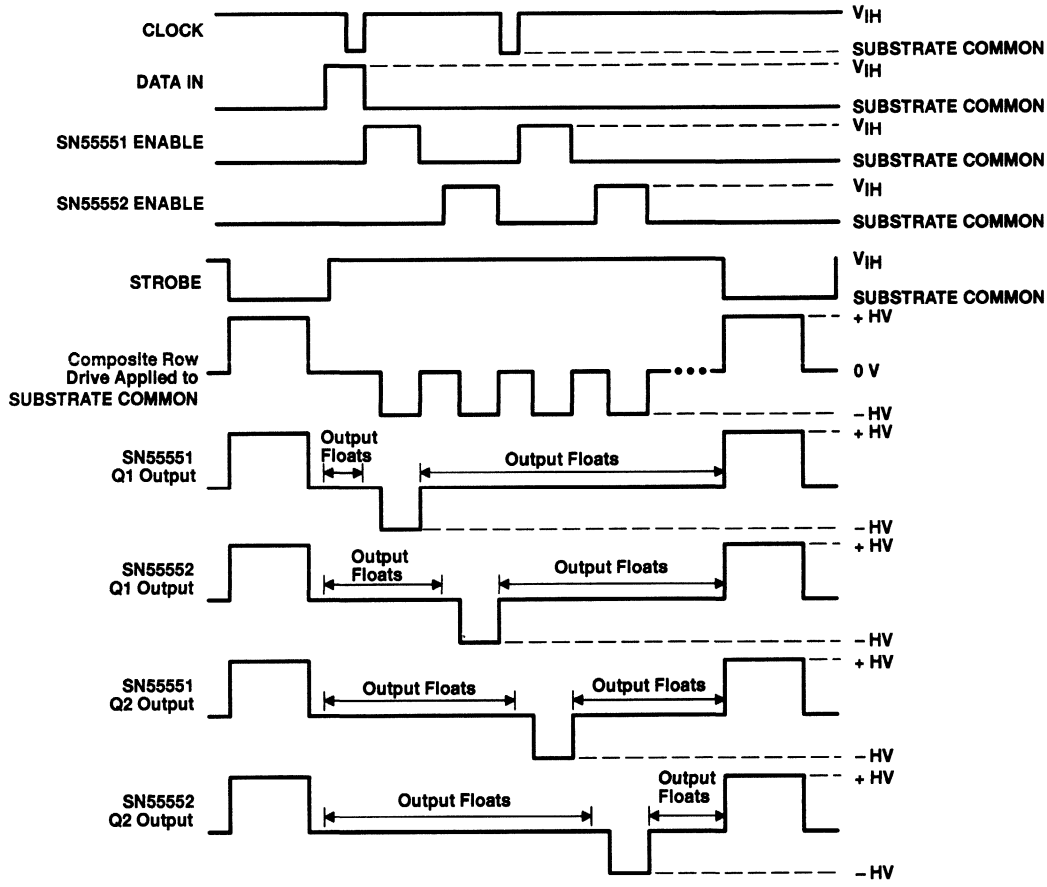
FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	ENABLE	STROBE		SERIAL	Q1 THRU Q32
Load	↓	X	X	Load and Shift†	R32	Determined by ENABLE and STROBE
	No ↓	X	X	No change	R32	Determined by ENABLE and STROBE
Enable	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
Strobe	X	X	L	As determined above	R32	All Q outputs on

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.

† Register R32 takes on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

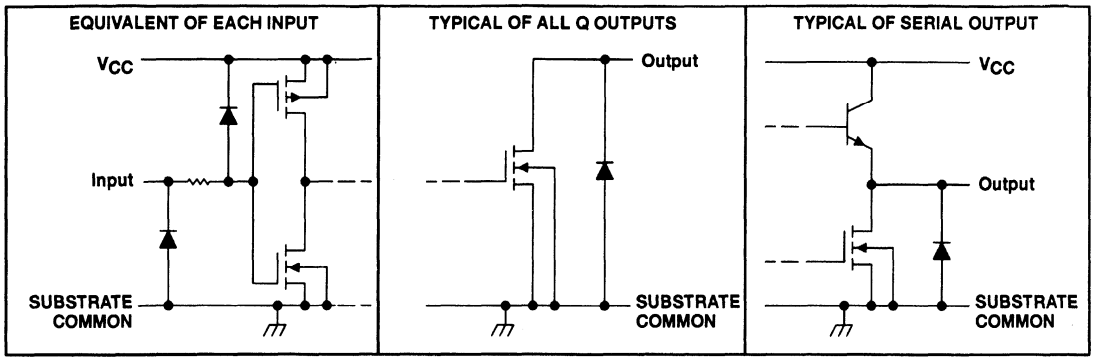
typical operating sequence



HV = high voltage

NOTE: During operation, CLOCK, DATA IN, ENABLE, and STROBE are referenced to the composite row drive signal received at SUBSTRATE COMMON of the device.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 18 V
Off-state Q output voltage, $V_{O(off)}$ ..... 225 V
Input voltage ..... V_{CC} + 0.3 V
Substrate common terminal current (see Note 2) ..... 1.5 A
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 3) ..... 1825 mW
Minimum operating free-air temperature ..... – 55°C
Operating case temperature ..... 125°C
Storage temperature range ..... –65°C to 150°C
Case temperature for 60 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to SUBSTRATE COMMON.
2. Duty cycle is limited by package dissipation.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 14.6 mV/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		10.8	12	15	V
High-level input voltage, V_{IH}		0.75 V_{CC}		V_{CC} +0.3	V
Low-level input voltage, V_{IL}		–0.3		0.25 V_{CC}	V
Off-state Q output voltage, $V_{O(off)}$		0		200	V
On-state output current, duty cycle ≤ 1 %, $I_{O(on)}$	V_{CC} = 10.8 V, T_C = 25°C			50	mA
	V_{CC} = 15 V, T_C = 25°C			80	
Clock frequency, f_{clock}, T_A = 25°C				6.25	MHz
Pulse duration, CLOCK high or low, t_w, T_A = 25°C		80			ns
Setup time, DATA IN before CLOCK↓, t_{su}, T_A = 25°C		20			ns
Hold time, DATA IN after CLOCK↓, t_h, T_A = 25°C		110			ns
Operating free-air temperature, T_A		–55			°C
Operating case temperature, T_C				125	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 12 V, SUBSTRATE COMMON at 0 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	SERIAL OUT	I_O = −100 μA	10		V
V_{OL}	Low-level output voltage	Q outputs	I_O = 50 mA		50	V
		SERIAL OUT	I_O = 100 μA		1.5	
$I_{O(off)}$	Off-state Q-output current		V_O = 200 V		50	μA
I_{IH}	High-level input current		V_I = 12 V		5	μA
I_{IL}	Low-level input current		V_I = 0		−5	μA
I_{CC}	Supply current				500	μA

switching characteristics, V_{CC} = 12 V, T_C = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DLH}	Delay time, CLOCK↓ to SERIAL OUT↓	C_L = 45 pF to COMMON SUBSTRATE, See Figure 1		200	ns
t_{DHL}	Delay time, CLOCK↓ to SERIAL OUT↑			200	ns
$t_{d(on)}$	Delay time, ENABLE to Q output↓	V_{CC} = 100 V, R_L = 2 kΩ, C_L = 45 pF to SUBSTRATE COMMON, See Figure 1		500	ns

RECOMMENDED OPERATING CONDITIONS

MAXIMUM ON-STATE Q OUTPUT CURRENT
vs
SUPPLY VOLTAGE

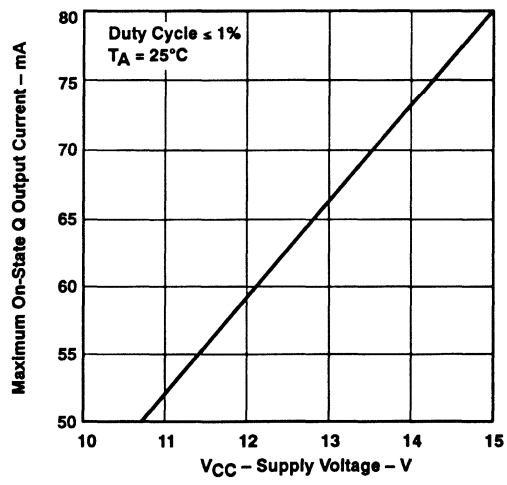
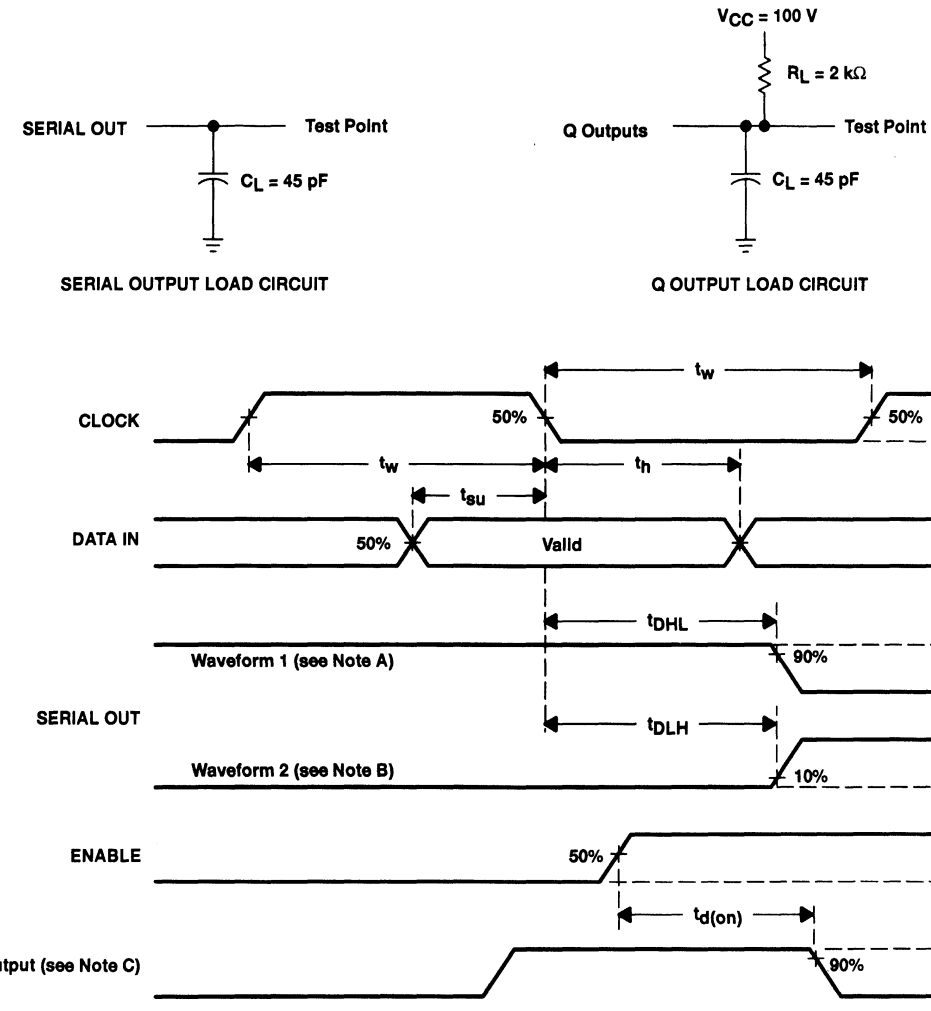


Figure 1

PARAMETER MEASUREMENT INFORMATION

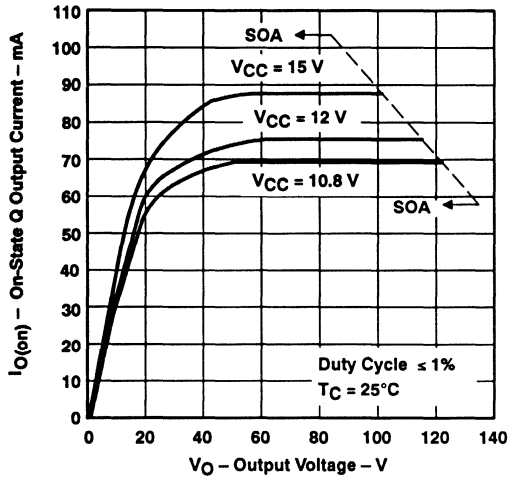


NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.
B. Waveform 2 is for internal conditions such that a high is clocked into R32.
C. To measure $t_{d(on)}$, a high is stored in the associated register.

Figure 2. Switching Characteristics, Load Circuits and Voltage Waveforms

TYPICAL CHARACTERISTICS

ON-STATE Q OUTPUT CURRENT
vs
OUTPUT VOLTAGE



SOA = Safe Operating Area

Figure 3

OUTPUT SATURATION CURRENT
vs
JUNCTION TEMPERATURE

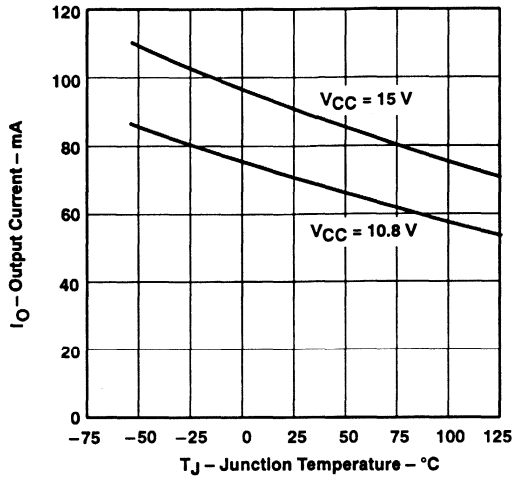


Figure 4

SGLS004 – D2744, APRIL 1986

- **Each Device Drives 32 Electrodes**
- **60-V Output Voltage Swing Capability**
- **15-mA Output Source and Sink Current Capability**
- **High-Speed Serially Shifted Data Input**
- **Totem-Pole Outputs**
- **Latches on All Driver Outputs**

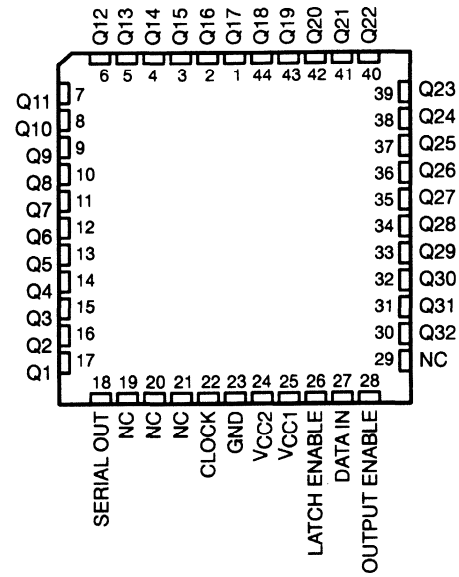
description

The SN55553 and SN55554 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN55554 output sequence is reversed from the SN55553 for ease in printed-circuit-board layout.

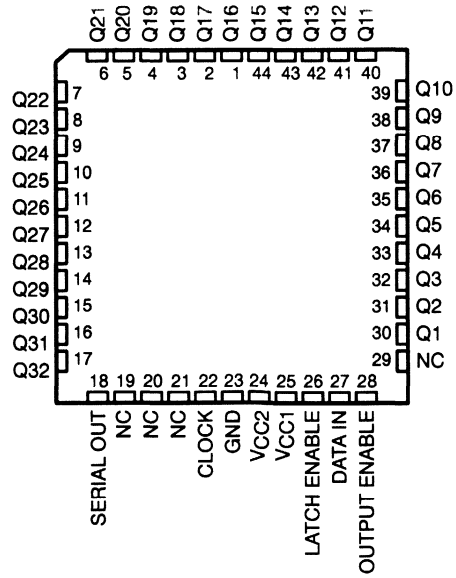
The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN55553 and SN55554 are characterized for operation over the full military temperature range of −55°C to 125°C.

SN55553 . . . FD PACKAGE
(TOP VIEW)



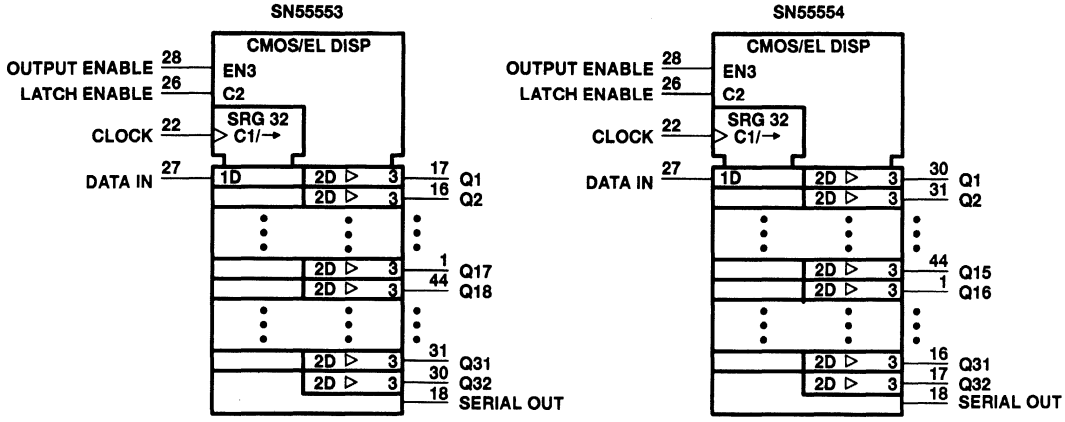
SN55554 . . . FD PACKAGE
(TOP VIEW)



NC – No internal connection

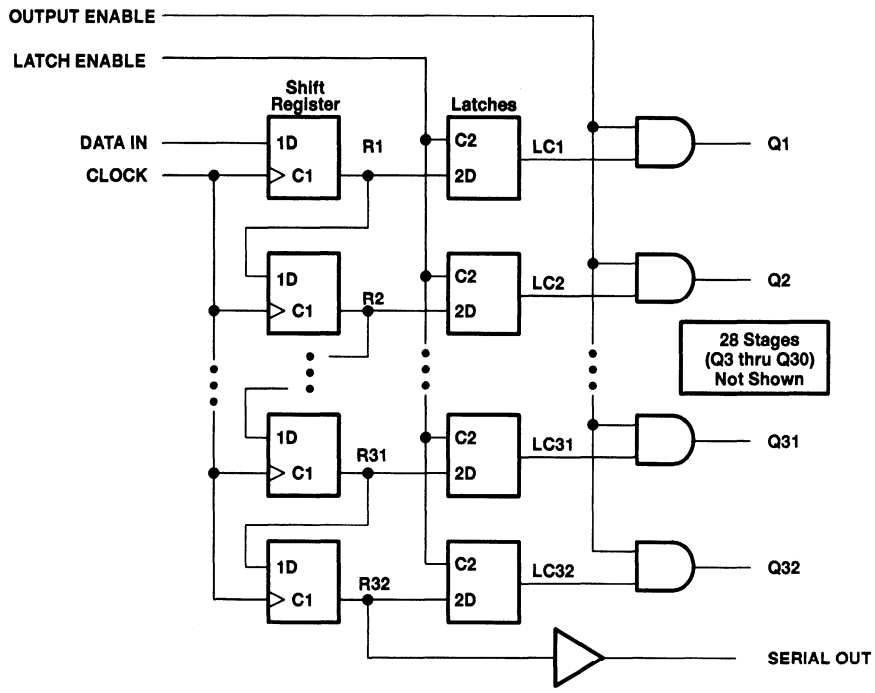
† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



FUNCTION TABLE

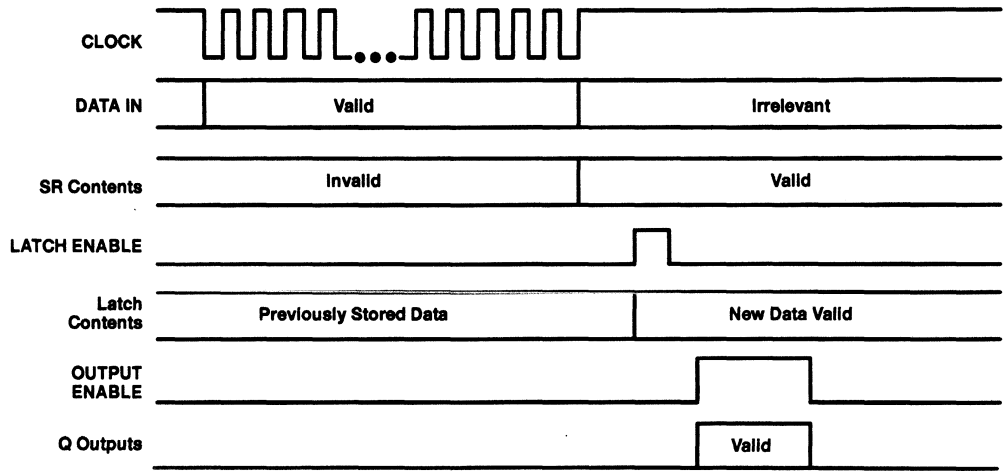
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q22
Load	↑	X	X	Load and shift†	Determined by	R32	Determined by
	No↑	X	X	No change	LATCH ENABLE‡	R32	OUTPUT ENABLE
Latch	X	L	X	As determined above	Stored data	R32	Determined by
	X	H	X		New data	R32	OUTPUT ENABLE
Output Enable	X	X	L	As determined above	Determined by	R32	All L
	X	X	H		LATCH ENABLE‡	R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

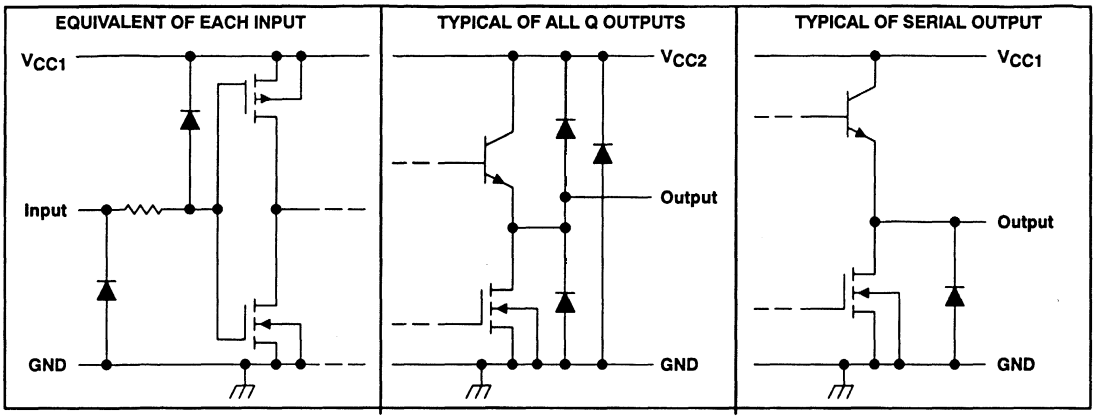
† R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 18 V
Supply voltage, V_{CC2} ..... 70 V
Input voltage, V_I ..... V_{CC1} + 0.3 V
Ground current ..... 700 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1825 mW
Minimum operating free-air temperature ..... −55°C
Operating case temperature ..... 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to network GND.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 14.6 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}	0		60	V
High-level input voltage, V_{IH}	0.75 V_{CC}		V_{CC} +0.3	V
Low-level input voltage, V_{IL}	−0.3		0.25 V_{CC}	V
High-level output current, I_{OH}	−15			mA
Low-level output current, I_{OL}	15			mA
Output clamp current, I_{OK}			±20	mA
Clock frequency, f_{clock}, T_A = 25°C	0		6.25	MHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$, T_A = 25°C	80			ns
Pulse duration, LATCH ENABLE, $t_{w(LE)}$, T_A = 25°C	80			ns
Setup time before CLOCK ↑, t_{su}, T_A = 25°C	20			ns
Hold time after CLOCK ↑, t_h, T_A = 25°C	110			ns
Operating free-air temperature, T_A	−55			°C
Operating case temperature, T_C			125	

electrical characteristics over recommended operating temperature range, V_{CC2} = 12 V, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	55		V
		SERIAL OUT	I_O = −100 μA	10		
V_{OL}	Low-level output voltage	Q outputs	I_O = 15 mA		10	V
		SERIAL OUT	I_O = 100 μA		1.5	
I_{IH}	High-level input current (see Note 3)		V_I = 12 V		5	μA
I_{IL}	Low-level input current (see Note 3)		V_I = 0		−5	μA
I_{CC1}	Supply current from V_{CC1}				7	mA
I_{CC2}	Supply current from V_{CC2}		Outputs high		20	mA
			Outputs low		2	

NOTE 3: I_{IH} and I_{IL} parameters are independent of V_{CC2} and need not be 60 V for this test.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{DLH}	Delay time, CLOCK↑ to SERIAL OUT↑	C_L = 45 pF to GND,	See Figures 1 and 2		200	ns
t_{DHL}	Delay time, CLOCK↑ to SERIAL OUT↓				200	ns
t_{DLH}	Delay time, LE to Q output↑	C_L = 45 pF to GND,	See Figures 1 and 3		1000	ns
t_{DHL}	Delay time, LE to Q output↓				500	μs

PARAMETER MEASUREMENT INFORMATION

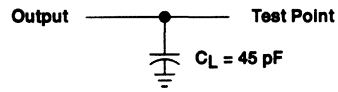


Figure 1. Load Circuit

PARAMETER MEASUREMENT INFORMATION

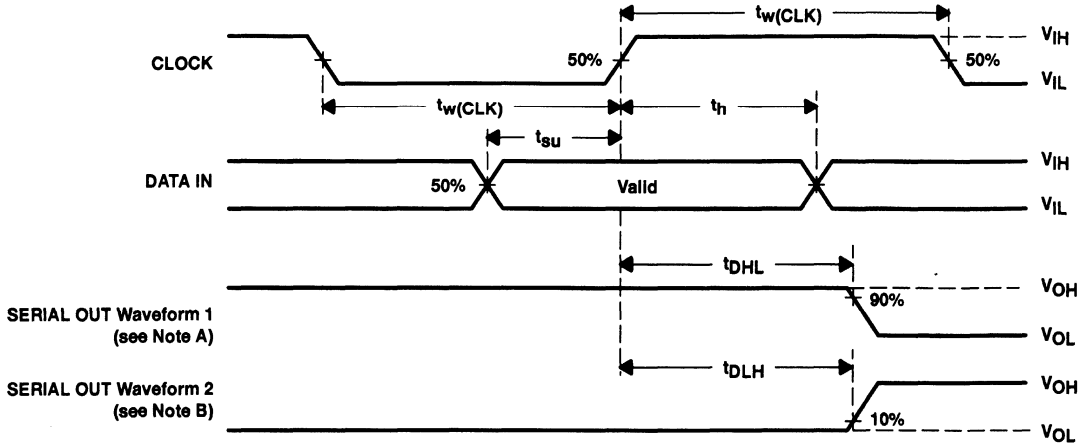


Figure 2. Voltage Waveforms for SERIAL OUT

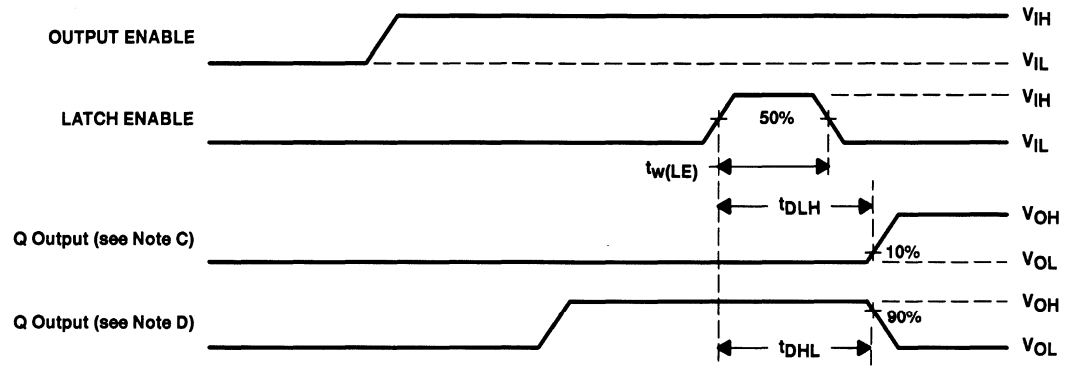


Figure 3. Voltage Waveforms for Q Outputs

NOTES: A. Waveform 1 is for internal conditions such that a low is clocked into R32.
B. Waveform 2 is for internal conditions such that a high is clocked into R32.
C. To measure t_{DLH}, initially a low is stored in the latch and a high is stored in the shift register.
D. To measure t_{DHL}, initially a high is stored in the latch and a low is stored in the shift register.

SGLS030 – D3313, OCTOBER 1989

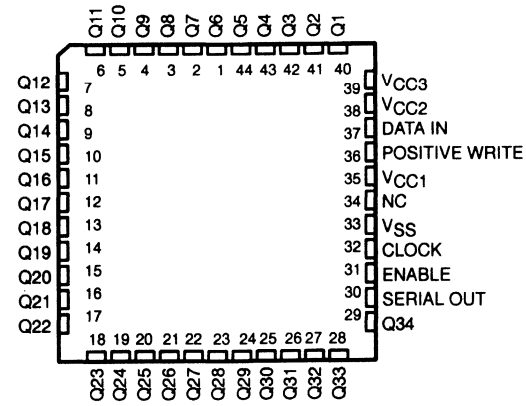
- **Each Device Drives 34 Electrodes**
- **Selectable Open-Source or Open-Drain Output**
- **Outputs Rated at 225 V**
- **Output Current Capability –90 mA to 150 mA**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

description

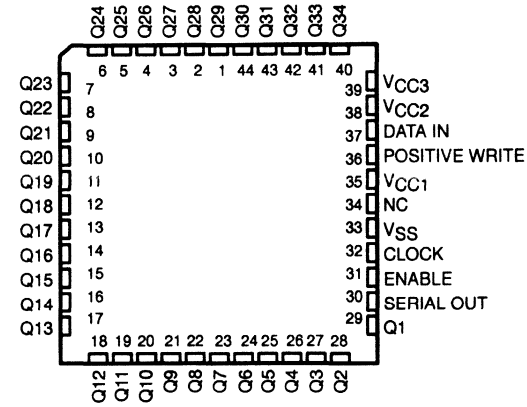
The SN55563A, and SN55564A are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible. If POSITIVE WRITE is high, the Q outputs act like open-source outputs and output data is not inverted with respect to input data. If POSITIVE WRITE is low, the Q outputs act like open-drain outputs and output data is inverted with respect to input data. The SN55564A output sequences are reversed from the SN55563A for ease in printed-circuit-board layout.

Typically, composite V_{CC2}, V_{CC3}, and ground signals are externally generated by a high-voltage switching circuit. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at the ENABLE input allows those outputs with a high in their associated register to be turned on, causing the corresponding row to be connected to V_{CC2} when POSITIVE WRITE is high or to ground when POSITIVE WRITE is low. V_{CC3} may be tied to V_{CC2} or held 5 V to 15 V above V_{CC2} for better V_{OH} characteristics. SERIAL OUTPUT from the shift register may be used to cascade additional devices. This output is not affected by the ENABLE or POSITIVE WRITE inputs.

SN55563A . . . FJ PACKAGE
(TOP VIEW)



SN55564A . . . FJ PACKAGE
(TOP VIEW)



NC – No internal connection

The SN55563A and SN55564A are characterized for operation over the full military operating temperature range of –55°C to 125°C.

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

LOAD FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R34	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
Load	↓	X	X	Load and shift†	R34	Determined by ENABLE and POSITIVE WRITE
	No ↓	X	X	No change	D34	Determined by ENABLE and POSITIVE WRITE

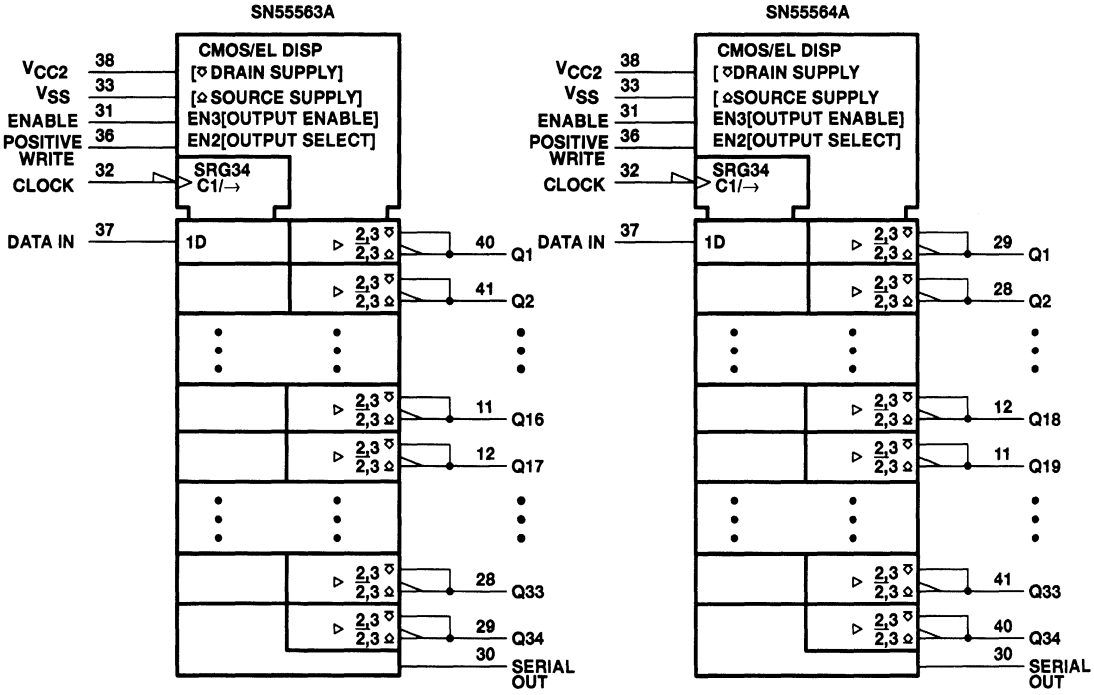
† Register R34 takes on the state of R33, R33 takes on the state of R32, . . . R2 takes on the state of R1, R1 takes on the state of the data input.

OUTPUT CONTROL FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS CONTENTS Rn FOR R1 THRU R34 (Determined Above)	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
Output Control	X	L	X	X	R34	High impedance
	X	H	H	H	R34	H
	X	H	L	H	R34	L
	X	X	X	L	R34	High impedance

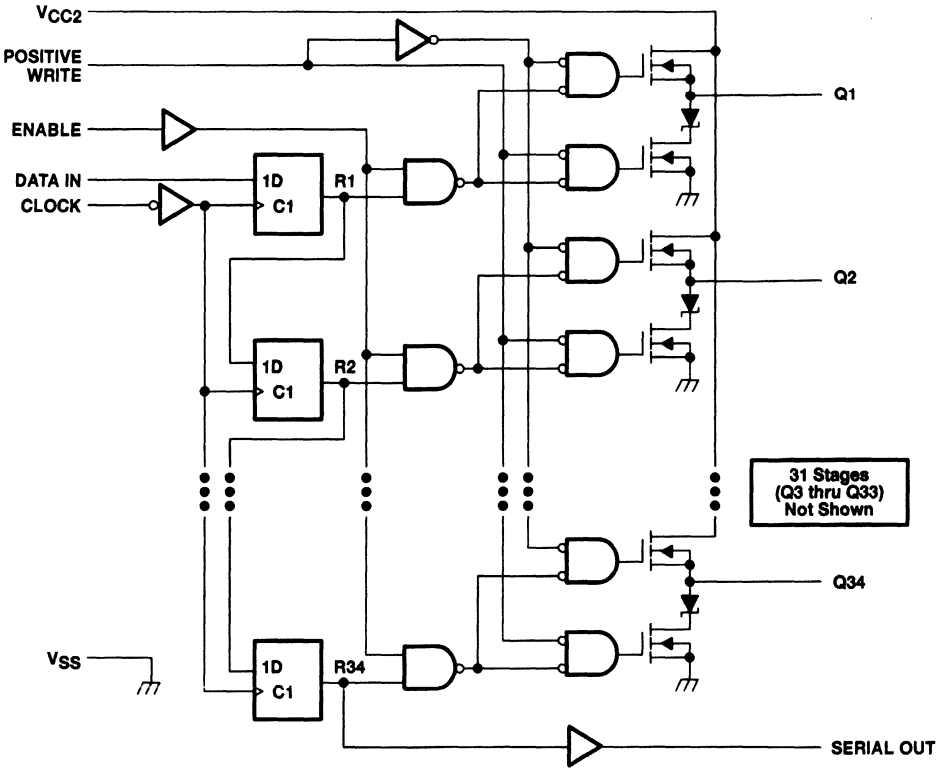
H = high, L = low, X = irrelevant, I = high-to-low transition

logic symbols‡

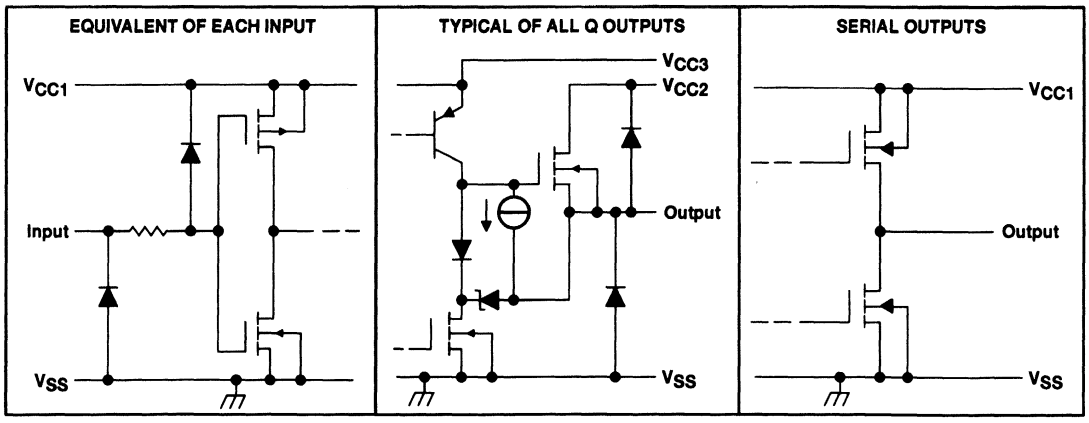


‡ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

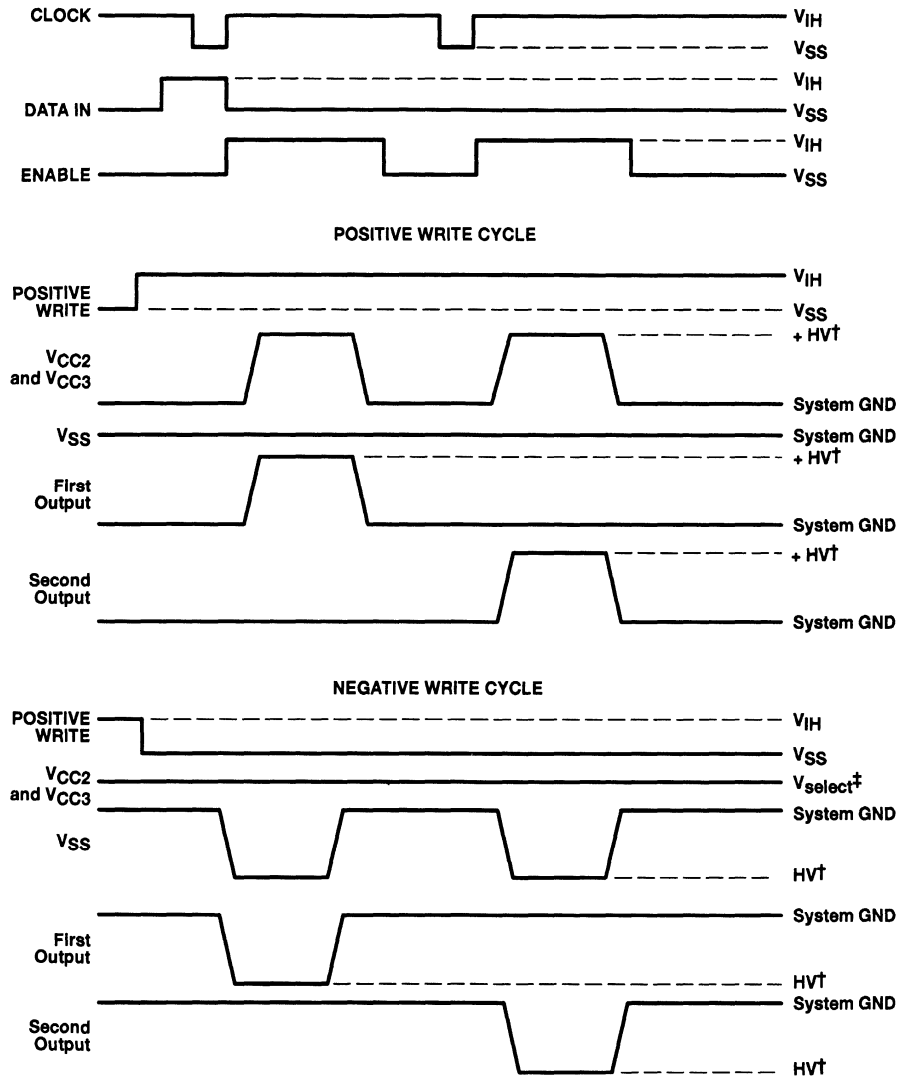
logic diagram (positive logic)



schematics of inputs and outputs



typical operating sequence



† HV = high voltage

‡ V_{SELECT} is a voltage level between V_{CC2} of the column driver and V_{SS}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 15 V
Supply voltage, V_{CC2} ..... 230 V
Supply voltage, V_{CC3} ..... 230 V
Supply voltage, V_{SS} ..... −230 V
Input voltage range, V_I ..... −0.3 V to V_{CC1} + 0.3 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1825 mW
Operating free-air temperature range ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate to 365 mW at 125°C at the rate of 14.6 mW/°C.

recommended operating conditions (see Figures 1 and 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	10.8	12	13.2	V
Supply voltage, V_{CC2}	V_{CC3} −15		V_{CC3}	V
Supply voltage, V_{CC3}	0		225	V
Supply voltage, V_{SS}	0		−225	V
High-level input voltage, V_{IH}	0.75V_{CC1}		V_{CC1}+0.3	V
Low-level input voltage, V_{IL}	−0.3†		0.25V_{CC1}	V
High-level output current, I_{OH}			−90	mA
Low-level output current, I_{OL}			150	mA
Output clamp current, I_{OK}			±150	mA
Clock frequency, f_{clock}			1	MHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$	125			ns
Setup time, DATA IN high or low before CLOCK↓, t_{su1}	100			ns
Setup time, CLOCK low before V_{CC2}↑ or V_{SS}↓, t_{su2}	300‡			ns
Setup time, ENABLE high before V_{CC2}↑ or V_{SS}↓, t_{su3}	300‡			ns
Setup time, POSITIVE WRITE high or low before V_{CC2}↑ or V_{SS}↓, t_{su4}	300‡			ns
Hold time, DATA IN high or low after CLOCK↓, t_{h1}	100			ns
Hold time, CLOCK high after V_{CC2}↓ or V_{SS}↑, t_{h2}	300‡			ns
Hold time, ENABLE high after V_{CC2}↓ or V_{SS}↑, t_{h3}	0‡			ns
Hold time, POSITIVE WRITE after V_{CC2}↓ or V_{SS}↑, t_{h4}	0‡			ns
Hold time, ENABLE low between successive V_{CC2}↑, t_{h5}	12‡			μs
Hold time, ENABLE low between successive V_{SS}↓, t_{h6}	300‡			ns
Operating free-air temperature, T_A	−55		125	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
‡ These minimum recommendations are not tested during manufacturing. Performance is dependent on application voltage and temperature and must be validated by the user.

electrical characteristics over recommended operating ranges of V_{CC1} and free-air temperature range, V_{CC2} = 225 V, V_{CC3} = 225 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −70 mA, V_{CC1} = 12 V	V_{CC2}−40		V
			I_O = −90 mA, V_{CC1} = 12 V	V_{CC2}−45		
		SERIAL OUT	I_O = −100 µA, V_{CC1} = 12 V	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_O = 150 mA		30	V
		SERIAL OUT	I_O = 100 µA		1	
$I_{O(off)}$	Off-state Q output current		V_O = 225 V		150	µA
			V_O = 0		−150	
I_{IH}	High-level input current		V_{IH} = V_{CC1}		100	µA
I_{IL}	Low-level input current		V_{IL} = 0		−100	µA
I_{CC1}	Supply current from V_{CC1}		One Q output high		4	mA
			All Q outputs low or high impedance		2	
I_{CC3}	Supply current from V_{CC3}†		One Q output high, V_{CC1} = 12 V		10	mA
			All Q outputs low or high impedance, V_{CC1} = 12 V		200	µA

† I_{CC3} is measured with V_{CC2} and V_{CC3} shorted together.

switching characteristics over recommended operating range of V_{CC1}, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level SERIAL OUT from CLOCK	C_L = 50 pF to V_{SS}, See Figures 3 and 4		400	ns
t_{PHL}	Propagation delay time, high-to-low level SERIAL OUT from CLOCK			400	ns

PARAMETER MEASUREMENT INFORMATION

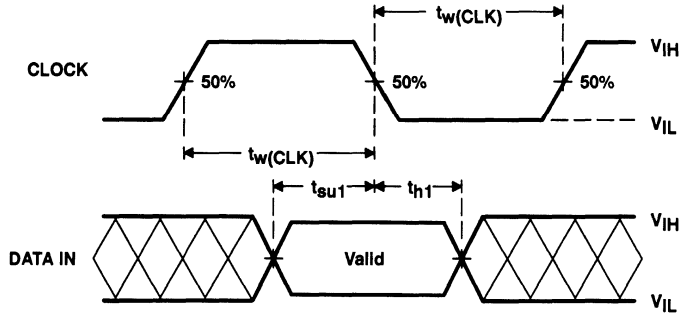
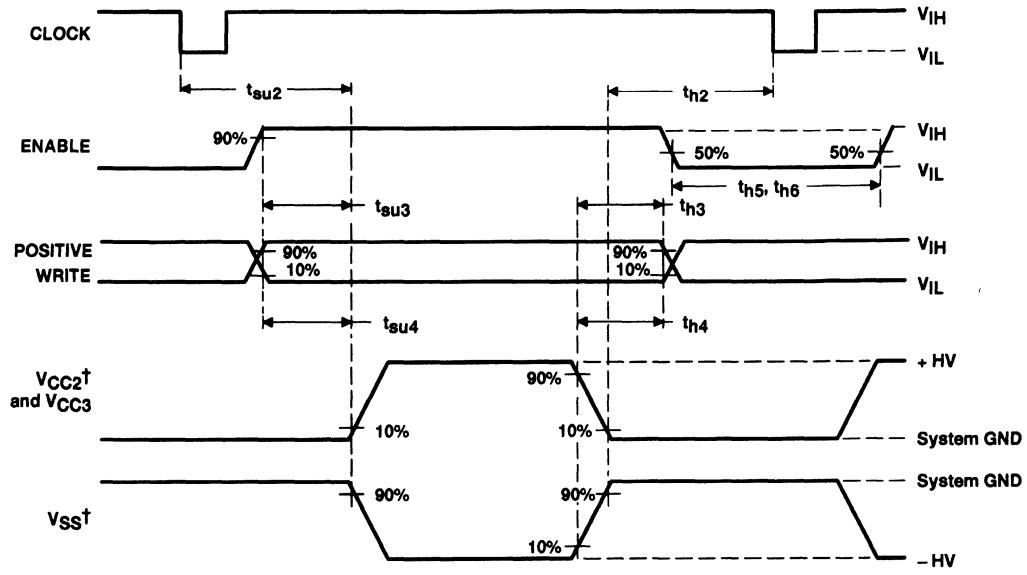


Figure 1. Input Timing Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



† Timing waveforms are with respect to V_{CC2} or V_{SS}, as appropriate.

Figure 2. Control Input Timing Voltage Waveforms

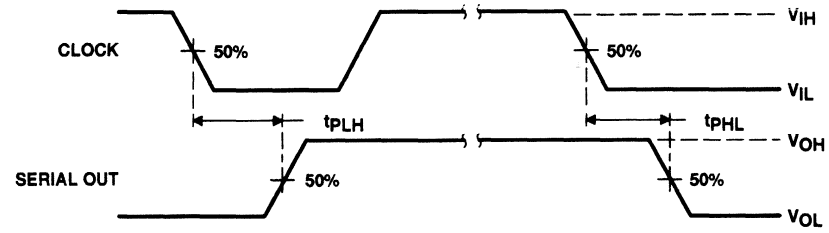
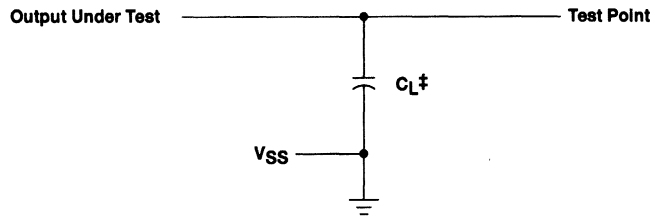


Figure 3. Voltage Waveforms for Propagation Delay Times, CLOCK to SERIAL OUT



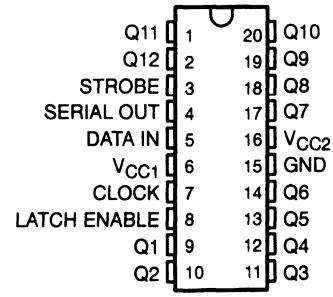
‡ C_L includes probe and jig capacitance.

Figure 4. Load Circuit

SLDS016A – D2654, DECEMBER 1985 – REVISED OCTOBER 1989

- **Each Device Drives 12 Lines**
- **60-V Output Voltage Swing Capability**
- **25-mA Output Source Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **TTL-Compatible Inputs**
- **Latches on All Driver Outputs**

DW OR N PACKAGE
(TOP VIEW)



description

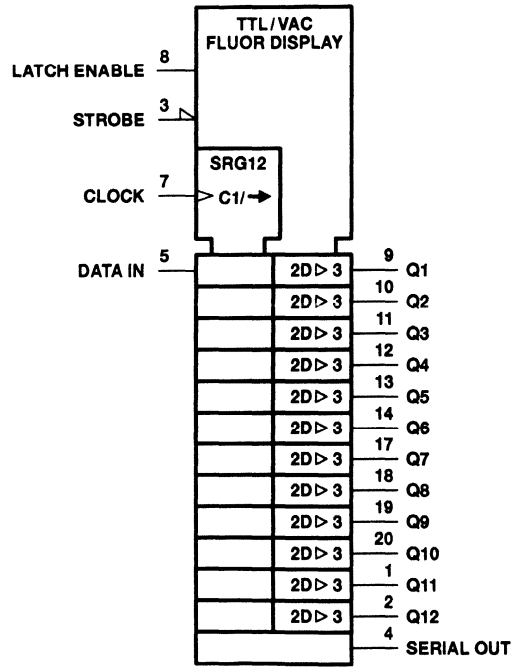
The SN65512B and SN75512B are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped pnp inputs and assume a high logic level when open circuited. The nominal input threshold voltage is 1.5 V. Outputs are totem-pole structures formed by an npn emitter-follower and double-diffused MOS (DMOS) transistors.

The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 12 latches. The active-low STROBE input enables all Q outputs. Serial data output from the shift register can be used to cascade shift registers. This output is not affected by LATCH ENABLE or STROBE.

The SN65512B is characterized for operation from −40°C to 85°C. The SN75512B is characterized for operation from 0°C to 70°C.

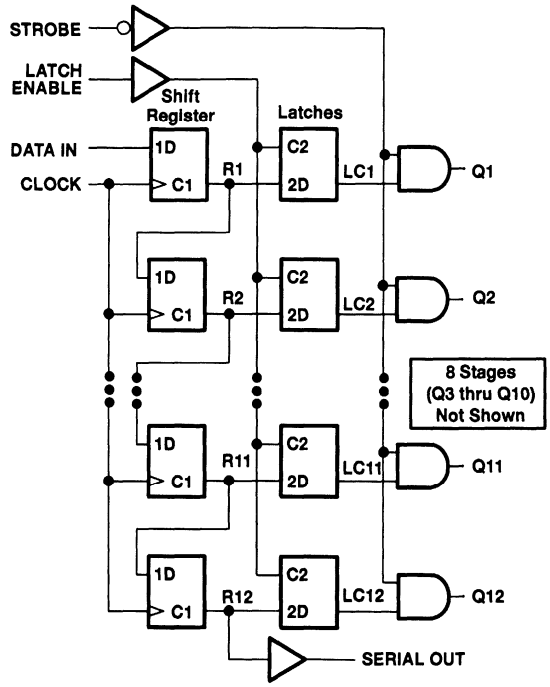
logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic diagram (positive logic)

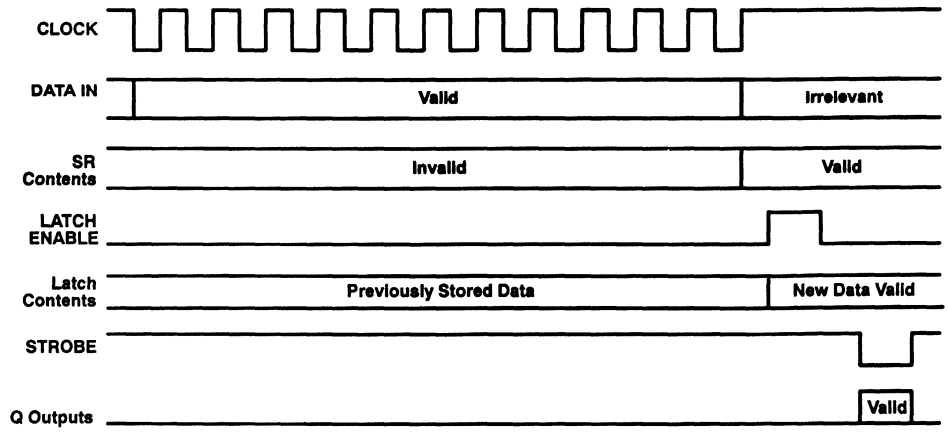


FUNCTION TABLE

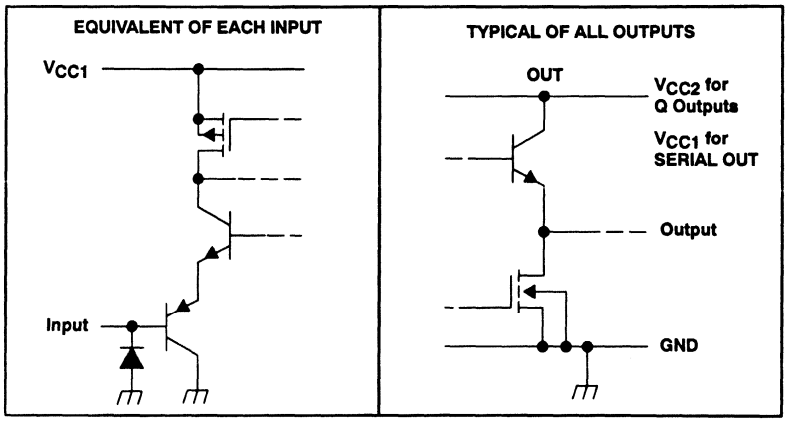
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R12	LATCHES LC1 THRU LC12	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q12
Load	↑ No ↑	X	X	Load and shift† No change	Determined by LATCH ENABLE‡	R12	Determined by STROBE
Latch	X	L H	X	As determined above	Stored data New data	R12	Determined by STROBE
Strobe	X	X	H L	As determined above	Determined by LATCH ENABLE‡	R12	All LC LC1 thru LC12, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition
† R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC1} (see Note 1) ..... 15 V
Supply voltage, V_{CC2} ..... 70 V
Input voltage, V_I ..... V_{CC1}
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65512B ..... −40°C to 85°C
SN75512B ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	589 mW

recommended operating conditions

			SN65512B		SN75512B		UNIT
			MIN	MAX	MIN	MAX	
Supply voltage, V_{CC1}			5	15	5	15	V
Supply voltage, V_{CC2}			0	60	0	60	V
High-level input voltage, V_{IH}			2		2		V
Low-level input voltage, V_{IL}				0.8		0.8	V
High-level output current, I_{OH}				−25		−25	mA
Low-level output current, I_{OL}	V_{CC1} = 10 V			5		5	mA
Clock frequency, f_{clock}	V_{CC1} = 15 V,	T_A = 25°C	0	4	0	4	MHz
	V_{CC1} = 5 V,	T_A = 25°C	0	1	0	1	
Pulse duration, CLOCK high or low, t_w	V_{CC1} = 15 V,	T_A = 25°C	100		100		ns
	V_{CC1} = 5 V,	T_A = 25°C	500		500		
Setup time, DATA IN valid before CLOCK ↑, t_{su} (see Figure 1)	V_{CC1} = 15 V,	T_A = 25°C	100		100		ns
	V_{CC1} = 5 V,	T_A = 25°C	250		250		
Hold time, DATA IN valid after CLOCK ↑, t_h (see Figure 1)	V_{CC1} = 15 V,	T_A = 25°C	50		50		ns
	V_{CC1} = 5 V,	T_A = 25°C	250		250		
Operating free-air temperature, T_A			−40	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA,	V_{CC1} = 10 V	57.5	58		V
		SERIAL OUT	I_{OH} = −200 µA,	V_{CC1} = 10 V	9	9.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 5 mA,	V_{CC1} = 10 V		2.6	5	V
		SERIAL OUT	I_{OL} = 200 µA,	V_{CC1} = 10 V		0.05	0.2	
I_{IH}	High-level input current		V_{CC1} = 15 V,	V_I = 5 V		0.01	1	µA
I_{IL}	Low-level input current		V_{CC1} = 15 V,	V_I = 0.8 V		−25	−150	µA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 15 V	V_I = 5 V		80	500	µA
				V_I = 0.8 V		2	6	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC1} = 15 V	All outputs high		10	100	µA
				STROBE at 2 V		0.8	3	mA

† All typical values are at V_{CC1} = 5 V, T_A = 25°C.

switching characteristics, V_{CC1} = 10 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level output	C_L = 30 pF,	See Figure 2		300	ns
t_{PLH}	Propagation delay time, low-to-high level output				300	ns
t_{THL}	Transition time, high-to-low level output				500	ns
t_{TLH}	Transition time, low-to-high level output				500	ns

PARAMETER MEASUREMENT INFORMATION

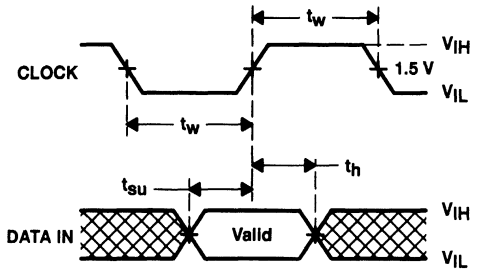


Figure 1. Input Timing Voltage Waveforms

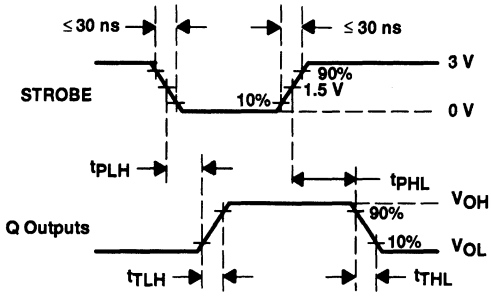
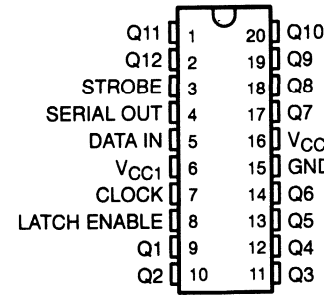


Figure 2. Switching Time Voltage Waveforms

SLDS054 – D3518, MAY 1990

- **Each Device Drives 12 Lines**
- **60-V Output Voltage Swing Capability**
- **25-mA Output Source Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **TTL-Compatible Inputs**
- **Latches on All Driver Outputs**

DW OR N PACKAGE
(TOP VIEW)



description

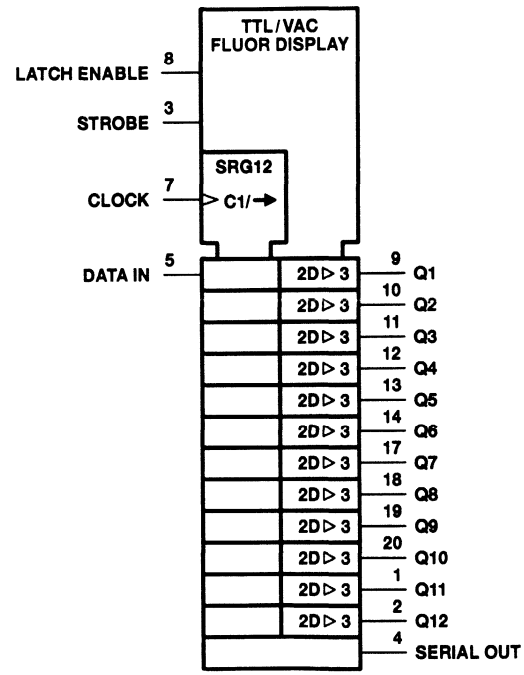
The SN65512C and SN75512C are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped pnp inputs and assume a high logic level when open circuited. The nominal input threshold is 1.5 V. Outputs are totem-pole structures formed by an npn emitter follower and double-diffused MOS (DMOS) transistors.

The device consists of a 12-bit shift register, 12 latches, and 12 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 12 latches. The active-low STROBE input enables all Q outputs. Serial data output from the shift register can be used to cascade shift registers. This output is not affected by LATCH ENABLE or STROBE.

The SN65512C is characterized for operation from −40°C to 85°C. The SN75512C is characterized for operation from 0°C to 70°C.

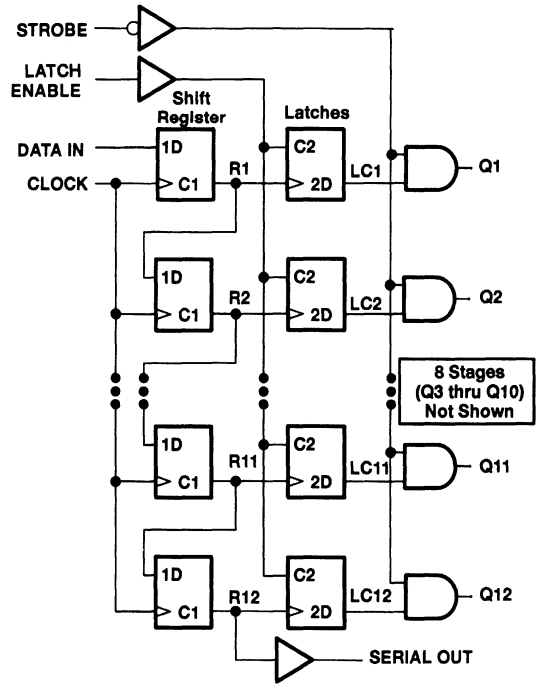
logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic diagram (positive logic)

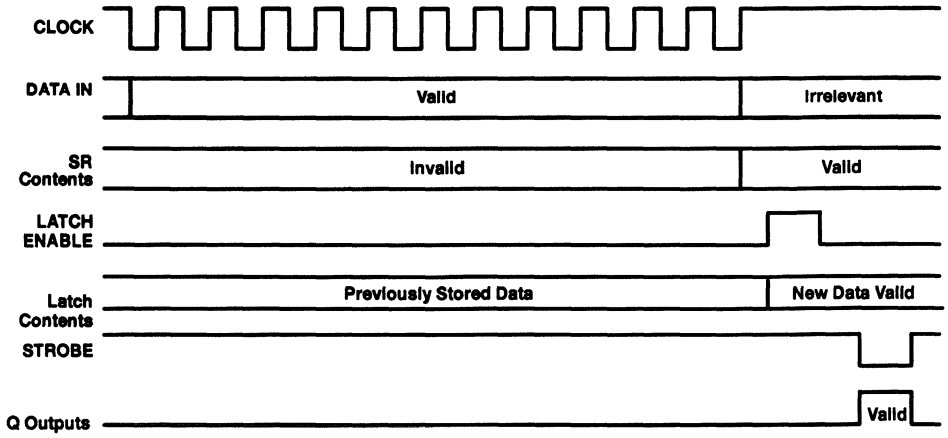


FUNCTION TABLE

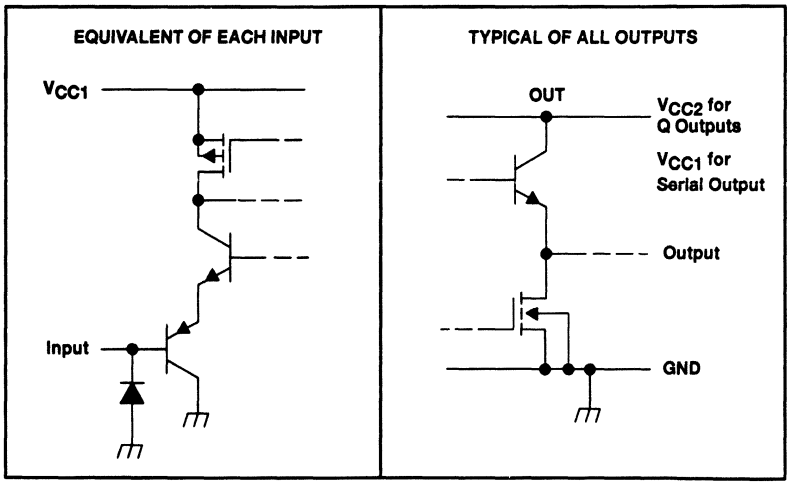
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R12	LATCHES LC1 THRU LC12	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q12
Load	↑ No ↑	X	X	Load and shift† No change	Determined by LATCH ENABLE‡	R12	Determined by STROBE
Latch	X	L H	X	As determined above	Stored data New data	R12	Determined by STROBE
Strobe	X	X	H L	As determined above	Determined by LATCH ENABLE‡	R12	All L LC1 thru LC12, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition
† R12 takes on the state of R11, R11 takes on the state of R10, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.
‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 15 V
Supply voltage, V_{CC2} ..... 70 V
Input voltage, V_I ..... V_{CC1}
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65512C ..... −40°C to 85°C
SN75512C ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

			SN65512C		SN75512C		UNIT
			MIN	MAX	MIN	MAX	
Supply voltage, V_{CC1}			5	15	5	15	V
Supply voltage, V_{CC2}			0	60	0	60	V
High-level input voltage, V_{IH}			2		2		V
Low-level input voltage, V_{IL}				0.8		0.8	V
High-level output current, I_{OH}				−25		−25	mA
Low-level output current, I_{OL}	V_{CC1} = 5 V			5		5	mA
Clock frequency, f_{clock}	V_{CC1} = 15 V,	T_A = 25°C	0	4	0	4	MHz
	V_{CC1} = 5 V,	T_A = 25°C	0	1	0	1	MHz
Pulse duration, CLOCK high or low, t_w	V_{CC1} = 15 V,	T_A = 25°C	100		100		ns
	V_{CC1} = 5 V,	T_A = 25°C	500		500		ns
Setup time, DATA IN before CLOCK ↑, t_{su} (see Figure 1)	V_{CC1} = 15 V,	T_A = 25°C	100		100		ns
	V_{CC1} = 5 V,	T_A = 25°C	250		250		ns
Hold time, DATA IN after CLOCK ↑, t_h (see Figure 1)	V_{CC1} = 15 V,	T_A = 25°C	50		50		ns
	V_{CC1} = 5 V,	T_A = 25°C	250		250		ns
Operating free-air temperature, T_A			−40	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC2} = 60 V

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA,	V_{CC1} = 5 V	57.5	58		V
		SERIAL OUT	I_{OH} = −200 μA,	V_{CC1} = 5 V	4.5	4.7		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA,	V_{CC1} = 5 V		2.8	5	V
		SERIAL OUT	I_{OL} = 200 μA,	V_{CC1} = 5 V		0.05	0.2	
I_{IH}	High-level input current		V_{CC1} = 15 V,	V_I = 5 V		0.01	10	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V,	V_I = 0.8 V		−25	−150	μA
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 15 V	V_I = 5 V		500	800	μA
				V_I = 0.8 V		2	6	mA
I_{CC2}	Supply current from V_{CC2}		V_{CC1} = 15 V	All outputs high		6	12	mA
				STROBE at 2 V		100	500	μA

† All typical values are at V_{CC1} = 5 V, T_A = 25°C.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{DHL}	Delay time, high-to-low level output	C_L = 30 pF, See Figure 2		300	ns
t_{DLH}	Delay time, low-to-high level output			300	ns
t_{THL}	Transition time, high-to-low level output			500	ns
t_{TLH}	Transition time, low-to-high level output			500	ns

PARAMETER MEASUREMENT INFORMATION

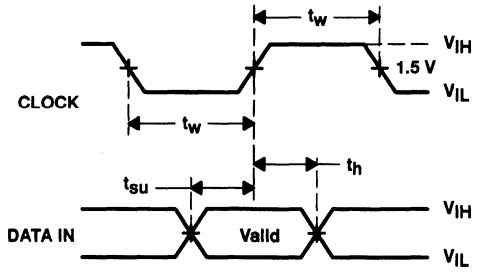


Figure 1. Input Timing Voltage Waveforms

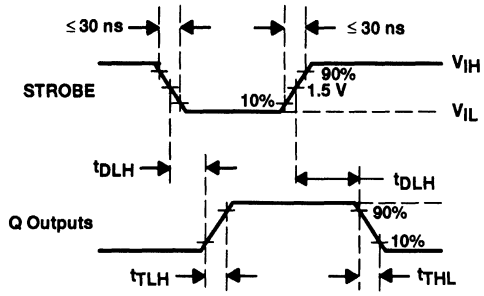


Figure 2. Switching Time Voltage Waveforms

SLDS004B – D2720, MARCH 1983 – REVISED MAY 1990

- **Each Device Drives 32 Lines**
- **60-V Output Voltage Swing Capability**
- **25-mA Output Source Current Capability**
- **High-Speed Serially Shifted Data Input**
- **Latches on All Driver Outputs**

description

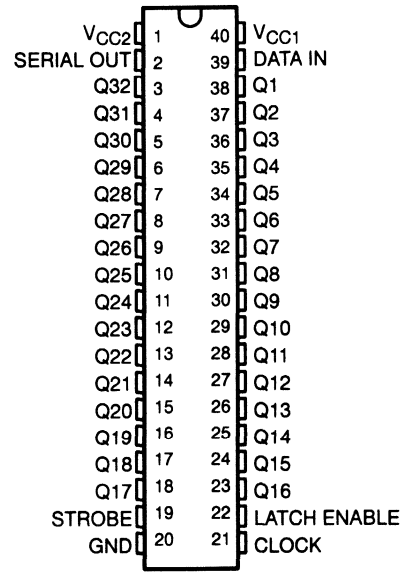
The SN65518 and SN75518 are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

Each device consists of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. While LATCH ENABLE is high, parallel data is transferred to the output buffers through a 32-bit latch. Data present in the latch during the high-to-low transition of LATCH ENABLE is latched. When STROBE is low, all Q outputs are enabled. When STROBE is high, all Q outputs are low.

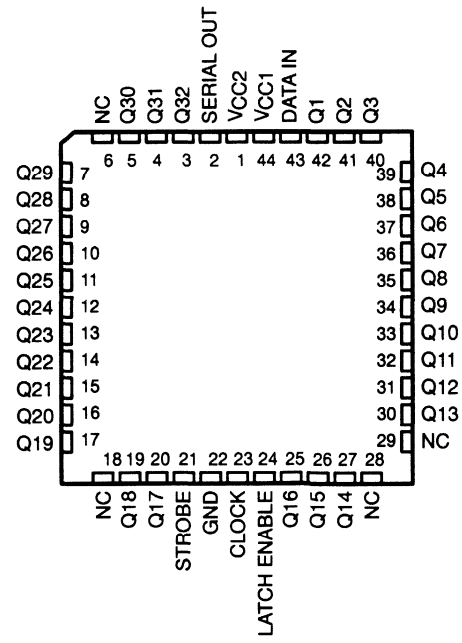
Serial data output from the shift register may be used to cascade additional devices. This output is not affected by LATCH ENABLE or STROBE.

The SN65518 is characterized for operation from −40°C to 85°C. The SN75518 is characterized for operation from 0°C to 70°C.

N PACKAGE
(TOP VIEW)



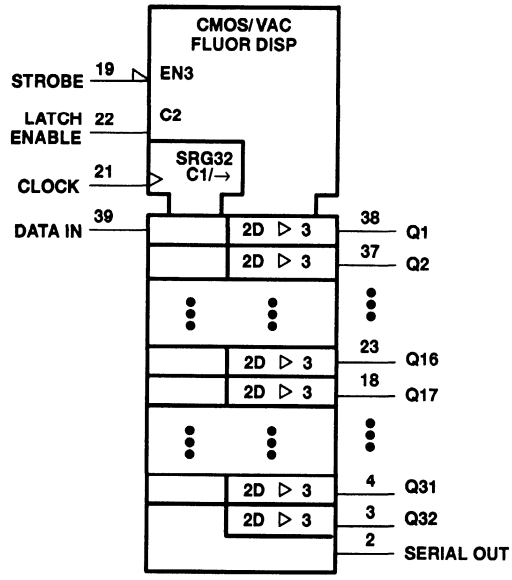
FN PACKAGE
(TOP VIEW)



NC – No internal connection

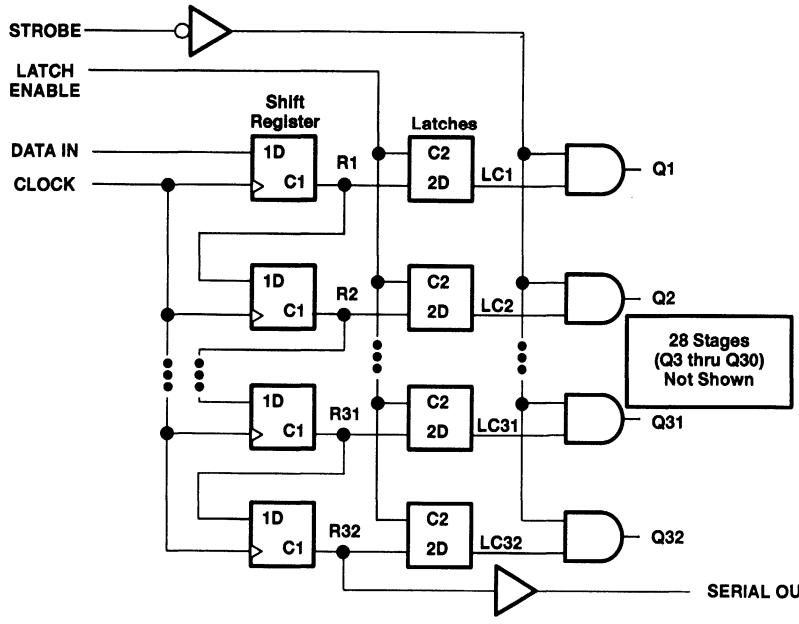
† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



FUNCTION TABLE

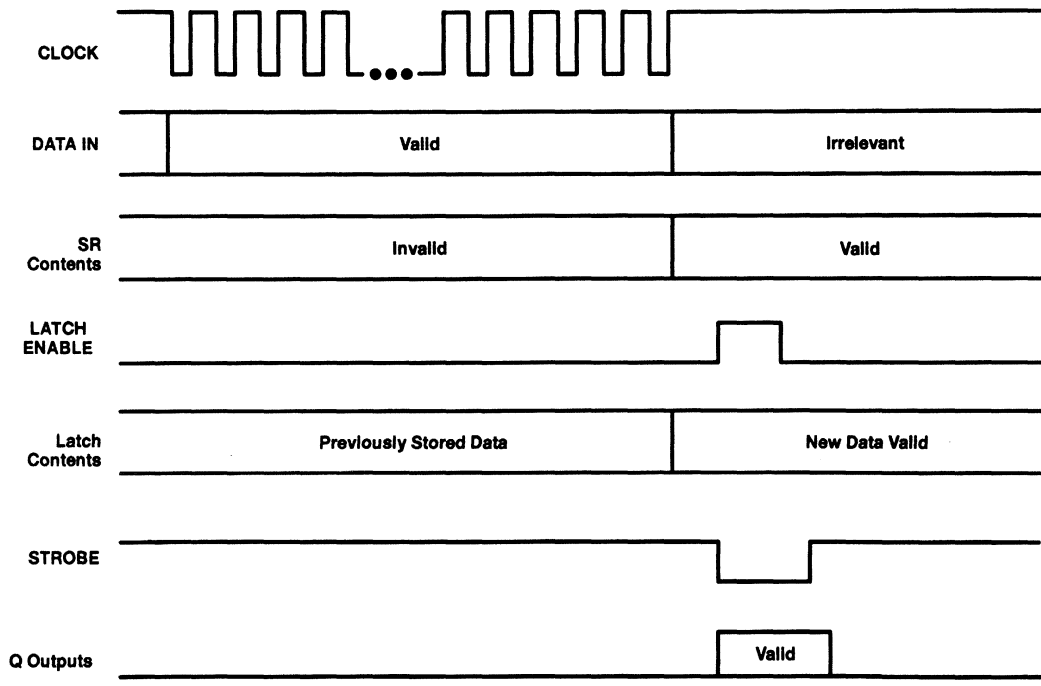
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	STROBE			SERIAL	Q1 THRU Q32
Load	↑ No ↑	X X	X X	Load and shift† No change	Determined by LATCH ENABLE‡	R32	Determined by STROBE
Latch	X X	L H	X X	As determined above	Stored data New data	R32	Determined by STROBE
Strobe	X X	X X	H L	As determined above	Determined by LATCH ENABLE‡	R32	All L LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

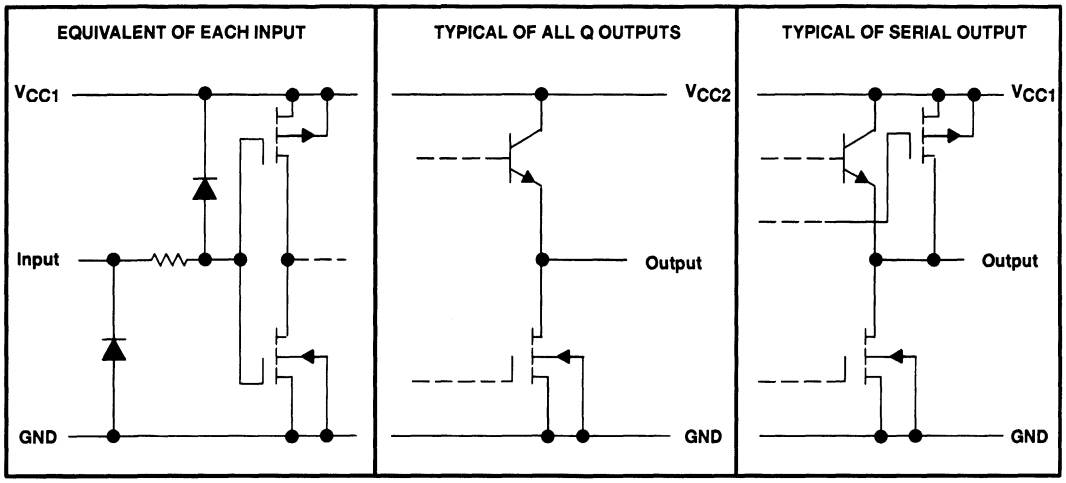
† R32 and the serial output take on the state of R31, R31 takes on the state of R30, ... R2 takes on the state of R1, and R1 takes on the state of the data input.

‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 15 V
Supply voltage, V_{CC2} ..... 70 V
Input voltage, V_I ..... V_{CC1}
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A: SN65518 ..... −40°C to 85°C
SN75518 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions, T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{CC1}		4.5	15	V
Supply voltage, V_{CC2}		0	60	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC1} = 4.5 V	3.5		V
	V_{CC1} = 15 V	12		
Low-level input voltage, V_{IL} (see Figure 1)		−0.3	0.8	V
High-level output current, I_{OH}			−25	mA
Low-level output current, I_{OL}			2	mA
Clock frequency, f_{clock} (see Figure 2)	V_{CC1} = 10 V to 15 V	0	5	MHz
	V_{CC1} = 4.5 V	0	1	
Pulse duration, CLOCK high, $t_{w(CKH)}$	V_{CC1} = 10 V to 15 V	100		ns
	V_{CC1} = 4.5 V	500		
Pulse duration, CLOCK low, $t_{w(CKL)}$	V_{CC1} = 10 V to 15 V	100		ns
	V_{CC1} = 4.5 V	500		
Setup time, DATA IN before CLOCK↑, t_{su}	V_{CC1} = 10 V to 15 V	75		ns
	V_{CC1} = 4.5 V	150		
Hold time, DATA IN after CLOCK↑, t_h	V_{CC1} = 10 V to 15 V	75		ns
	V_{CC1} = 4.5 V	150		
Operating free-air temperature, T_A	SN65518	−40	85	°C
	SN75518	0	70	

electrical characteristics over recommended ranges of operating free-air temperature and V_{CC1}, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA		57.5	58		V
		SERIAL OUT	V_{CC1} = 5 V,	I_{OH} = −20 μA	4.5	4.9	5	
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA				5	V
		SERIAL OUT	I_{OL} = 20 μA			0.06	0.8	
I_{IH}	High-level input current		V_{CC1} = 15 V,	V_I = 15 V		0.1	1	μA
I_{IL}	Low-level input current		V_{CC1} = 15 V,	V_I = 0 V		−0.1	−1	μA
I_{CC1}	Supply current		V_{CC1} = 4.5 V			1.8	4	mA
			V_{CC1} = 15 V			2	5	
I_{CC2}	Supply current	SN65518	Outputs high,	T_A = −40°C			12	mA
		SN65518, SN75518	Outputs high,	T_A = 0°C to MAX		7	10	
			Outputs low			0.01	0.5	

† All typical values are at T_A = 25°C.

switching characteristics, V_{CC2} = 60 V, C_L = 50 pF, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
t_d	Delay time, CLOCK to DATA OUT		V_{CC1} = 4.5 V	C_L = 15 pF, See Figure 4		600	ns
			V_{CC1} = 15 V			150	
t_{DHL}	Delay time, high-to-low-level Q output	From LATCH ENABLE	V_{CC1} = 4.5 V	See Figure 5		1.5	µs
		From STROBE		See Figure 6		1	
		From LATCH ENABLE	V_{CC1} = 15 V	See Figure 5		0.5	
		From STROBE		See Figure 6		0.5	
t_{DLH}	Delay time, low-to-high-level Q output	From LATCH ENABLE	V_{CC1} = 4.5 V	See Figure 5		1.5	µs
		From STROBE		See Figure 6		1	
		From LATCH ENABLE	V_{CC1} = 15 V	See Figure 5		0.25	
		From STROBE		See Figure 6		0.25	
t_{THL}	Transition time, high-to-low-level Q output		V_{CC1} = 4.5 V	See Figure 6		3	µs
			V_{CC1} = 15 V			1.5	
t_{TLH}	Transition time, low-to-high-level Q output		V_{CC1} = 4.5 V	See Figure 6		2.5	µs
			V_{CC1} = 15 V			0.75	

RECOMMENDED OPERATING CONDITIONS

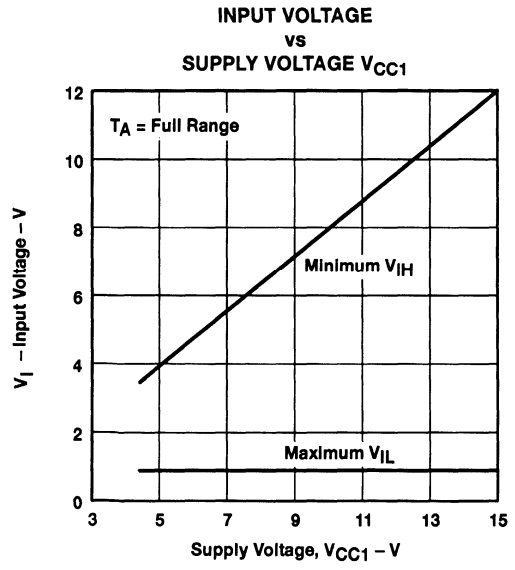


Figure 1

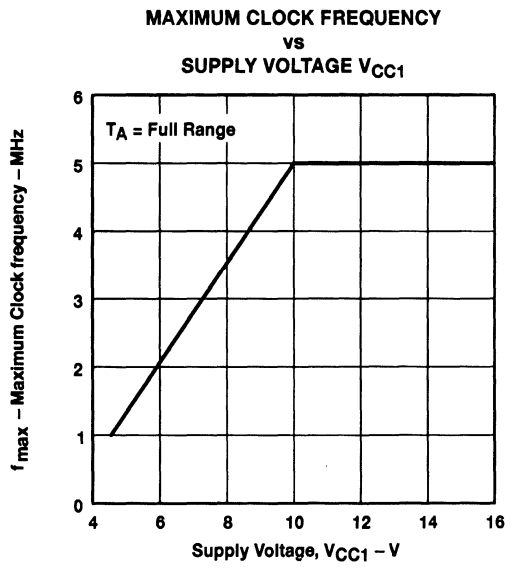


Figure 2

PARAMETER MEASUREMENT INFORMATION†

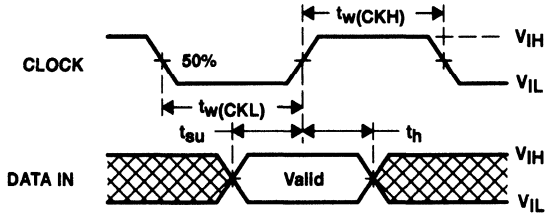


Figure 3. Input Timing Waveforms

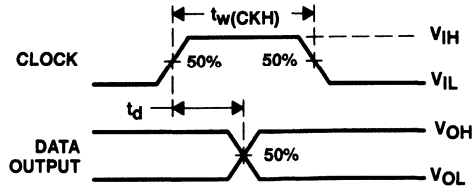


Figure 4. Data Output Switching Times

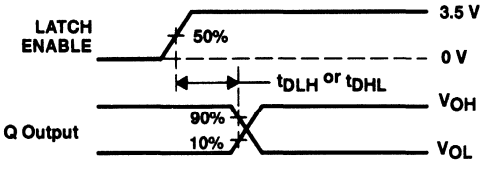


Figure 5. Q Output Switching Times

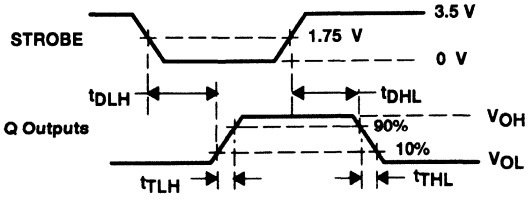


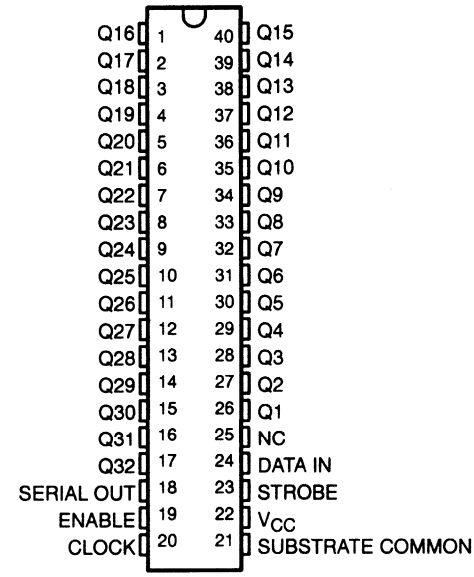
Figure 6. Switching Time Voltage Waveforms

† For testing purposes, all input pulses have maximum rise and fall times of 30 ns.

SLDS023B – D2743, MARCH 1983 – REVISED APRIL 1993

- **Each Device Drives 32 Electrodes**
- **High-Voltage Open-Drain DMOS Outputs**
- **50-mA Output Current Capability**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

SN65551 . . . N PACKAGE
(TOP VIEW)



NC – No internal connection

description

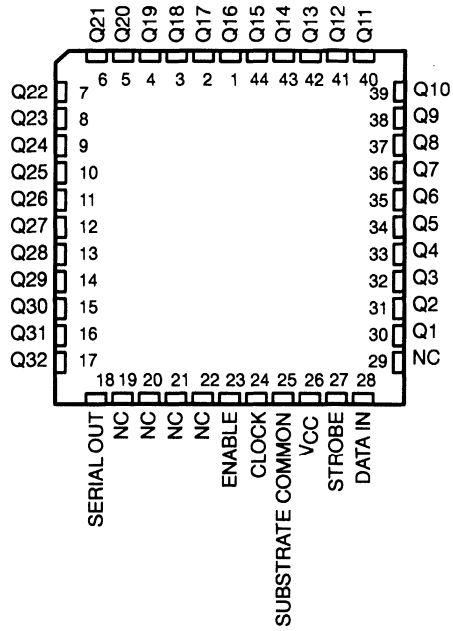
The SN65551, SN65552, SN75551, and SN75552 are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible and all outputs are high-voltage open-drain DMOS transistors. The SN75552 output sequence is reversed from the SN75551 for ease in printed-circuit-board layout.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to SUBSTRATE COMMON. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at ENABLE allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The serial data output (SERIAL OUT) from the shift register can be used to cascade additional devices. This output is not affected by ENABLE or STROBE.

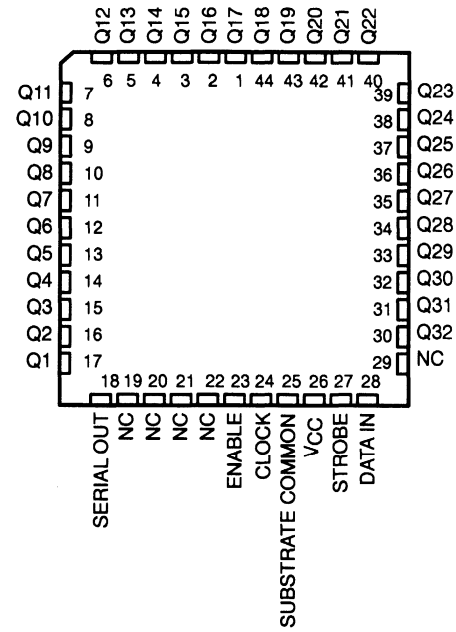
The SN65551 and SN65552 are characterized for operation from −40°C to 85°C. The SN75551 and SN75552 are characterized for operation from 0°C to 70°C.

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

SN65551, SN75551 . . . FN PACKAGE
(TOP VIEW)

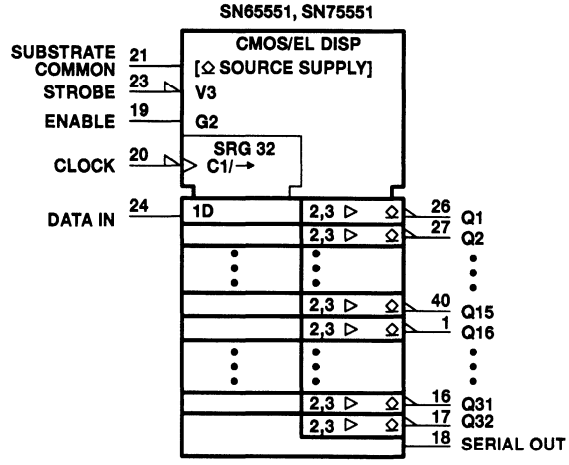


SN65552, SN75552 . . . FN PACKAGE
(TOP VIEW)



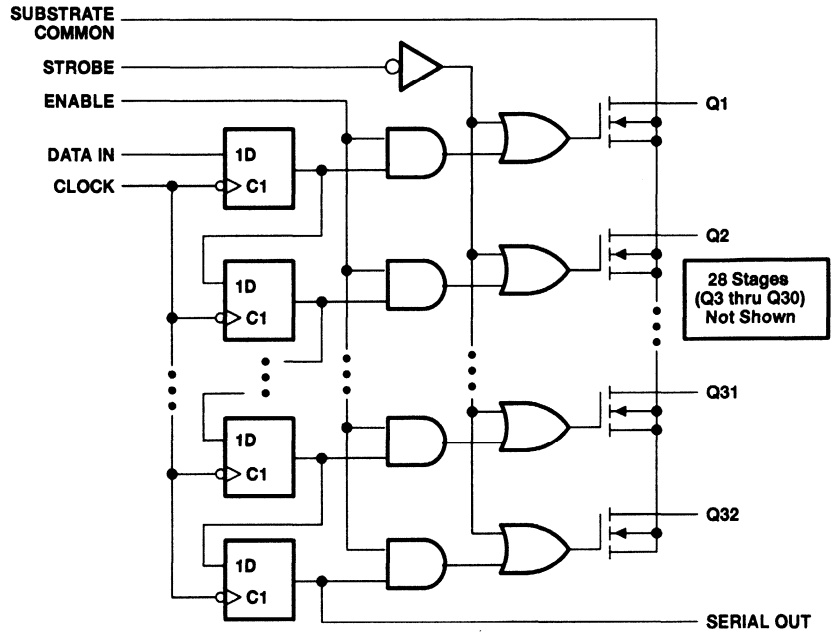
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. The symbol Ω here indicates an n-channel open-drain output.
Pin numbers shown are for the N package.

logic diagram (positive logic)



FUNCTION TABLE

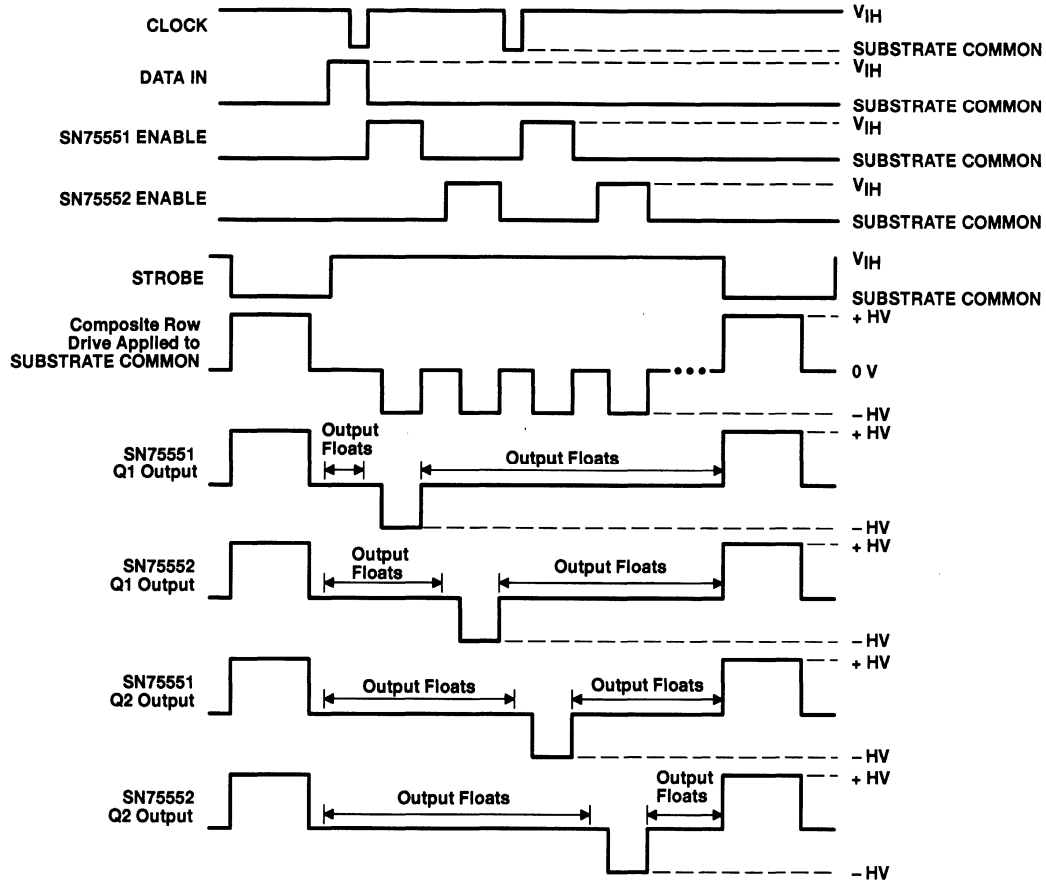
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	ENABLE	STROBE		SERIAL	Q1 THRU Q32
Load	↓	X	X	Load and shift†	R32	Determined by ENABLE and STROBE
	No ↓	X	X	No change	R32	Determined by ENABLE and STROBE
Enable	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
Strobe	X	X	L	As determined above	R32	All Q outputs on

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.

† Register R32 takes on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

SLDS023B – D2743, MARCH 1983 – REVISED APRIL 1993

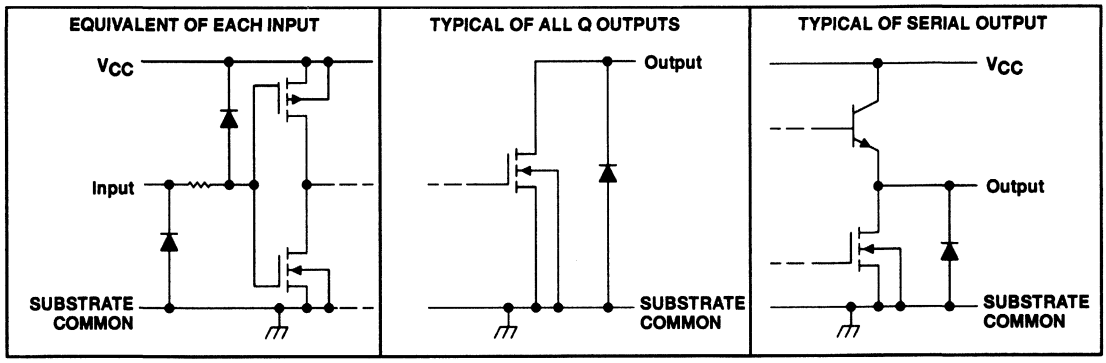
typical operating sequence



HV = high voltage

NOTE: During operation, CLOCK, DATA IN, ENABLE, and STROBE are referenced to the composite row drive signal received at SUBSTRATE COMMON of the device.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 18 V
Off-state Q output voltage, $V_{O(off)}$ ..... 225 V
Input voltage ..... V_{CC} + 0.3 V
Substrate common terminal current (see Note 2) ..... 1.5 A
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65551, SN65552 ..... – 40°C to 85°C
SN75551, SN75552 ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTES: 1. Voltage values are with respect to SUBSTRATE COMMON.
2. Duty cycle is limited by package dissipation.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		10.8	12	15	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC} = 10.8 V	8.1		11.1	V
	V_{CC} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)	V_{CC} = 10.8 V	−0.3		2.7	V
	V_{CC} = 15 V	−0.3		3.75	
Off-state Q output voltage, $V_{O(off)}$		0		200	V
On-state output current, duty cycle ≤ 1%, $I_{O(on)}$ (see Figures 2, 3, and 4)	V_{CC} = 10.8 V, T_A = 25°C			50	mA
	V_{CC} = 15 V, T_A = 25°C			80	
Output clamp current, I_{OK}				−45	mA
Clock frequency, f_{clock}		0		4	MHz
Pulse duration, CLOCK high or low, t_w		125			ns
Setup time, DATA IN before CLOCK, t_{su} (see Figure 5)		50			ns
Hold time, DATA IN after CLOCK, t_h (see Figure 5)		100			ns
Operating free-air temperature, T_A	SN65551, SN65552	−40		85	°C
	SN75551, SN75552	0		70	

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	SERIAL OUT	I_O = −100 µA	V_{CC}−1.5		V
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 50 mA, See Figure 3		30	V
		SERIAL OUT	I_{OL} = 100 µA		1	
$I_{O(off)}$	Off-state Q-output current		V_O = 200 V		10	µA
I_{IH}	High-level input current		$V_I = V_{CC}$		1	µA
I_{IL}	Low-level input current		V_I = 0		−1	µA
I_{CC}	Supply current from V_{CC}				250	mA

switching characteristics, V_{CC} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level, SERIAL OUT from CLOCK	C_L = 20 pF to GND, See Figure 6		200	ns
t_{PLH}	Propagation delay time, low-to-high level, SERIAL OUT from CLOCK			200	ns
$t_{d(on)}$	Turn-on delay time, Q outputs from ENABLE	I_{OL} = 50 mA, STROBE at V_{CC}, R_L = 1.4 kΩ to 100 V, See Figure 7		500	ns

RECOMMENDED OPERATING CONDITIONS

INPUT VOLTAGE LOGIC-LEVEL LIMITS
vs
SUPPLY VOLTAGE V_{CC}

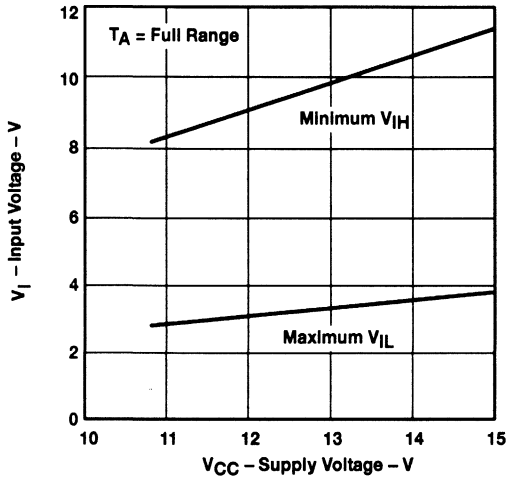


Figure 1

MAXIMUM ON-STATE Q OUTPUT CURRENT
vs
SUPPLY VOLTAGE

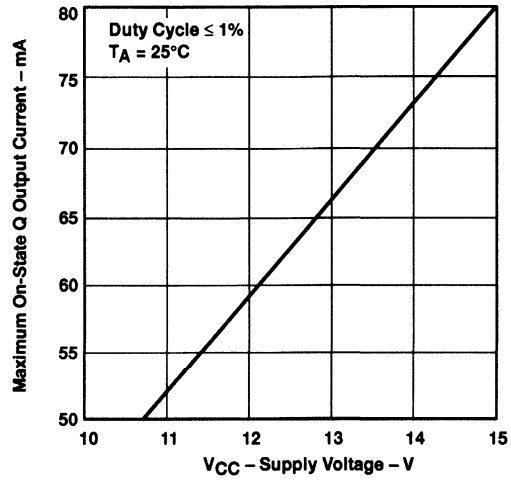
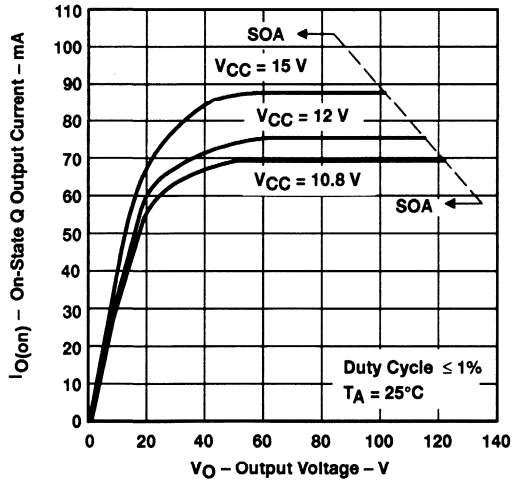


Figure 2

ON-STATE Q OUTPUT CURRENT
vs
OUTPUT VOLTAGE



SOA = Safe Operating Area

Figure 3

OUTPUT SATURATION CURRENT
vs
FREE-AIR TEMPERATURE†

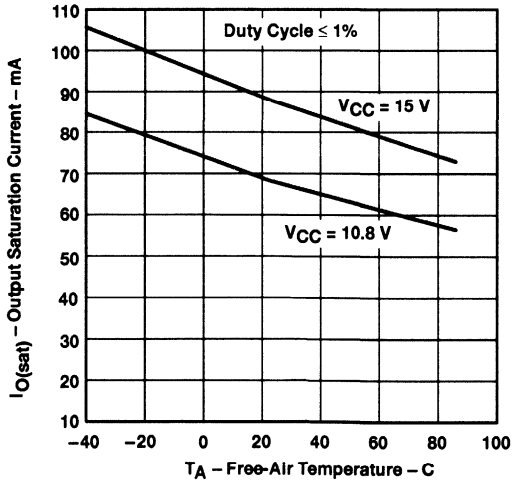


Figure 4

† Data for temperatures between 0°C and 70°C apply only for the SN75551 and SN75552 devices.

PARAMETER MEASUREMENT INFORMATION

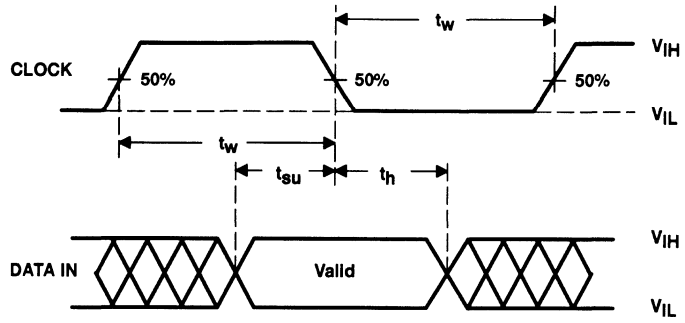


Figure 5. Input Timing Voltage Waveforms

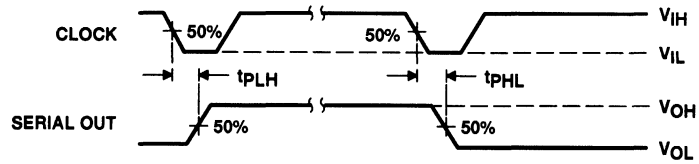


Figure 6. Voltage Waveforms, SERIAL OUT

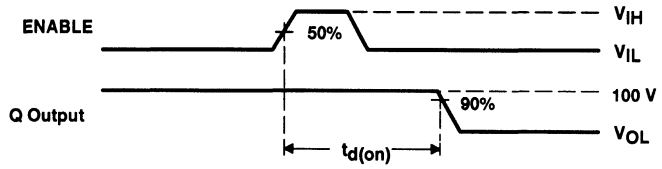


Figure 7. Voltage Waveforms, Q Outputs

SLDS030A – D2744, MARCH 1983 – REVISED MARCH 1993

- **Each Device Drives 32 Electrodes**
- **60-V Output Voltage Swing Capability**
- **15-mA Output Source and Sink Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **Totem-Pole Outputs**
- **Latches on All Driver Outputs**

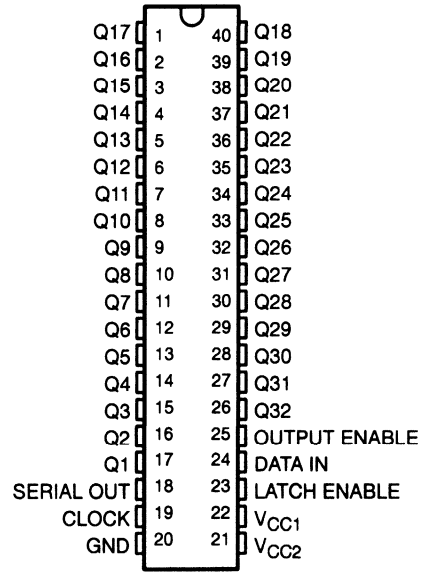
description

The SN65553, SN65554, SN75553, and SN75554 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN65554 and SN75554 output sequence is reversed from the SN65553 and SN75553 for ease in printed-circuit-board layout.

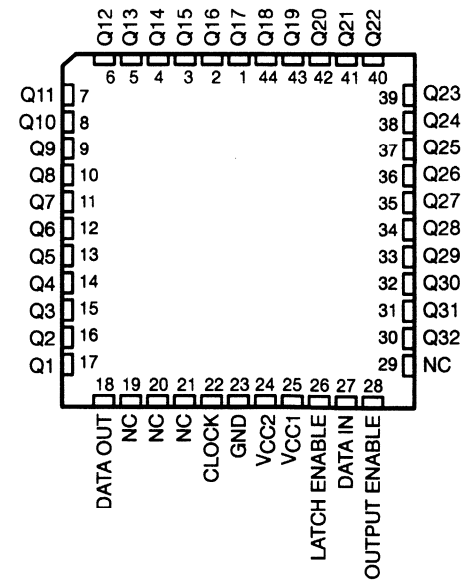
The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Serial data output from the shift register can be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN65553 and SN65554 are characterized for operation from –40°C to 85°C. The SN75553 and SN75554 are characterized for operation from 0°C to 70°C.

SN75553 . . . N PACKAGE
(TOP VIEW)



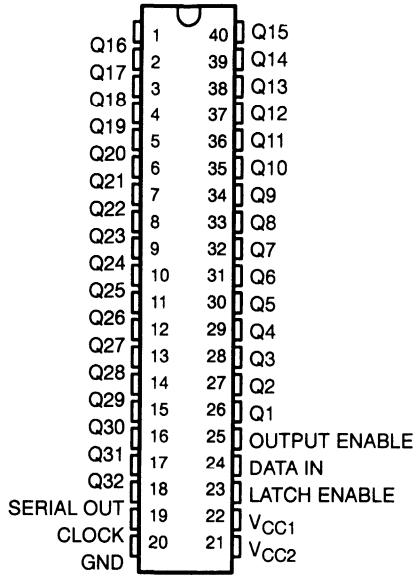
SN65553, SN75553 . . . FN PACKAGE
(TOP VIEW)



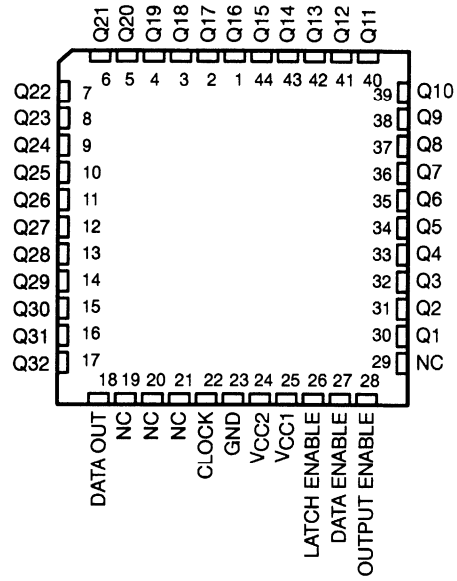
NC – No internal connection

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

SN65554, SN75554 . . . N PACKAGE
(TOP VIEW)



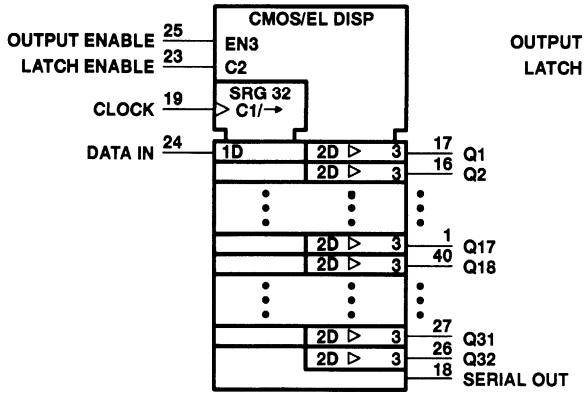
SN65554, SN75554 . . . FN PACKAGE
(TOP VIEW)



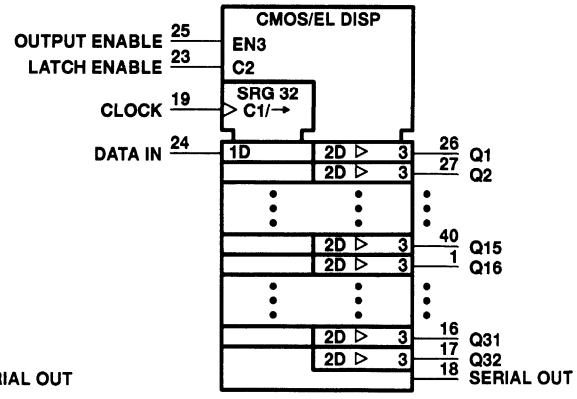
NC – No internal connection

logic symbols†

SN65553, SN75553

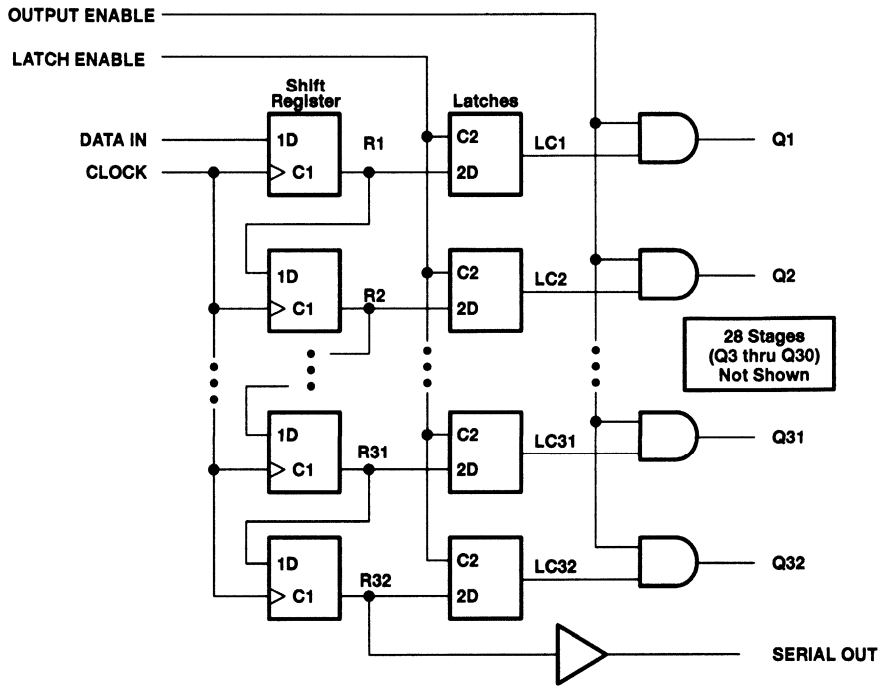


SN65554, SN75554



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for N packages.

logic diagram (positive logic)



FUNCTION TABLE

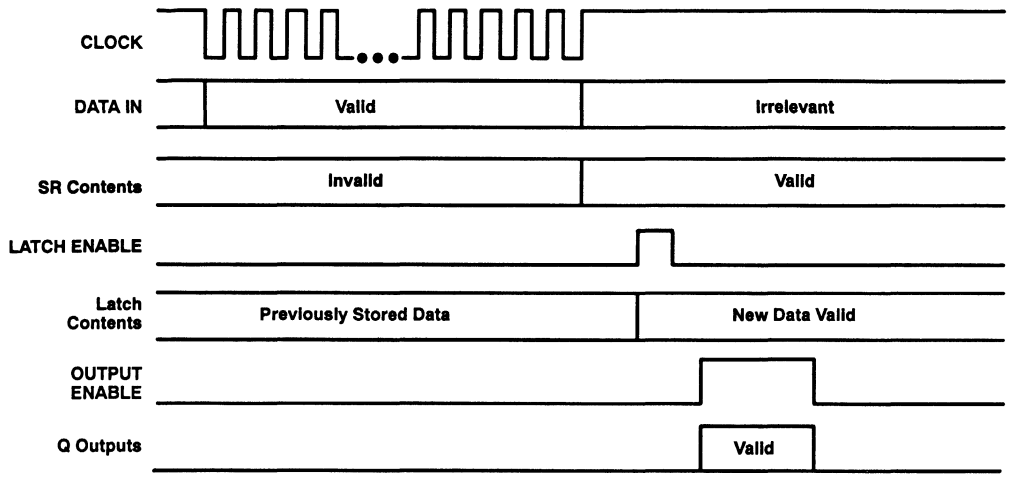
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q22
Load	↑	X	X	Load and shift†	Determined by	R32	Determined by
	No↑	X	X	No change	LATCH ENABLE‡	R32	OUTPUT ENABLE
Latch	X	L	X	As determined above	Stored data	R32	Determined by
	X	H	X		New data	R32	OUTPUT ENABLE
Output Enable	X	X	L	As determined above	Determined by	R32	All L
	X	X	H		LATCH ENABLE‡	R32	LC1 thru LC32, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

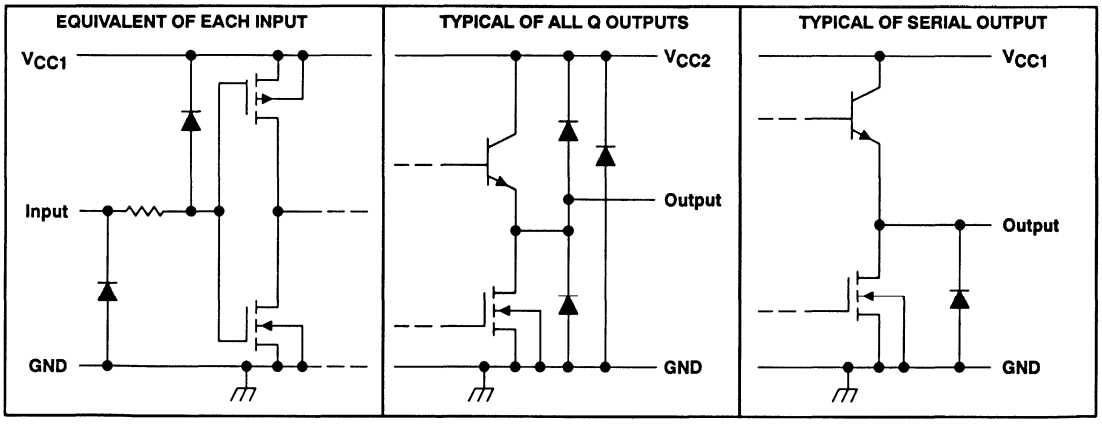
† R32 and the serial output take on the state of R31, R31 takes on the state of R30, . . .R2 takes on the state of R1, and R1 takes on the state of the data input.

‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 18 V
Supply voltage, V_{CC2} ..... 70 V
Input voltage, V_I ..... V_{CC1} + 0.3 V
Ground current ..... 700 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65553, SN65554 ..... −40°C to 85°C
SN75553, SN75554 ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTE 1: Voltage values are with respect to network GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	15	V
Supply voltage, V_{CC2}		0		60	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC1} = 10.8 V	8.1		11.1	V
	V_{CC1} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)	V_{CC1} = 10.8 V	−0.3		2.7	V
	V_{CC1} = 15 V	−0.3		3.75	
High-level output current, I_{OH}		−15			mA
Low-level output current, I_{OL}		15			mA
Output clamp current, I_{OK}				20	mA
Clock frequency, f_{clock}		0		6.25	MHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$ (see Figure 2)		80			ns
Pulse duration, LATCH ENABLE, $t_{w(LE)}$ (see Figure 4)		80			ns
Setup time, DATA IN before CLOCK ↑, t_{su} (see Figure 2)		20			ns
Hold time, DATA IN after CLOCK ↑, t_h (see Figure 2)		80			ns
Operating free-air temperature, T_A	SN65553, SN65554	−40		85	°C
	SN75553, SN75554	0		70	

electrical characteristics over recommended ranges of V_{CC1} and operating free-air temperature, V_{CC2} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = −15 mA	57		V
		SERIAL OUT	I_O = −100 µA	V_{CC1} − 1.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		SERIAL OUT	I_{OL} = 100 µA		1	
I_{IH}	High-level input current		$V_I = V_{CC1}$		1	µA
I_{IL}	Low-level input current		V_I = 0		−1	µA
I_{CC1}	Supply current from V_{CC1}				5	mA
I_{CC2}	Supply current from V_{CC2}	SN65553, SN65554			12	mA
		SN75553, SN75554			10	

switching characteristics, V_{CC1} = 12 V, V_{CC2} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level, SERIAL OUT from CLOCK	C_L = 20 pF to GND, See Figure 3		140	ns
t_{PLH}	Propagation delay time, low-to-high-level, SERIAL OUT from CLOCK			140	ns
t_{DHL}	Delay time, high-to-low-level, Q output from LATCH ENABLE	C_L = 20 pF to GND, See Figure 4		500	ns
t_{DLH}	Delay time, low-to-high-level, Q output from LATCH ENABLE	C_L = 20 pF to GND, See Figure 4		1	µs

RECOMMENDED OPERATING CONDITIONS

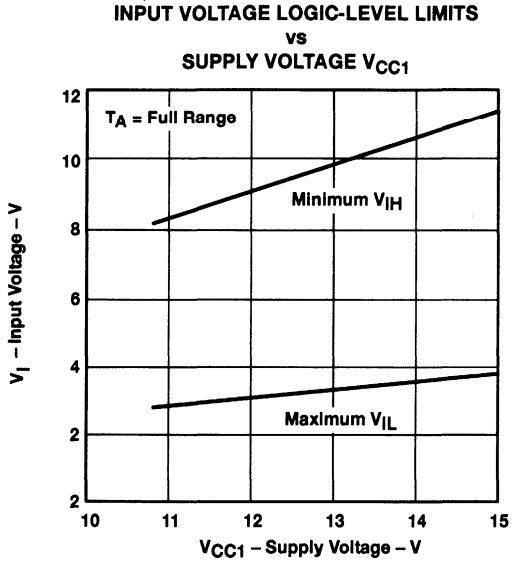


Figure 1

PARAMETER MEASUREMENT INFORMATION

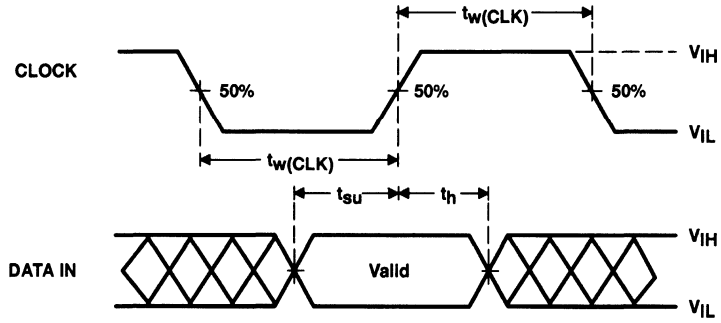


Figure 2. Input Timing Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

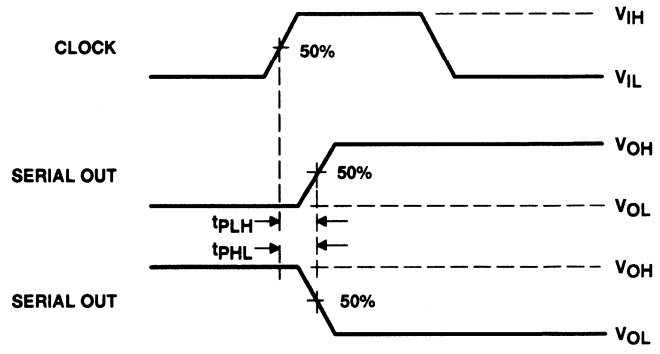


Figure 3. Voltage Waveforms for Propagation Delay Time, CLOCK to SERIAL OUT

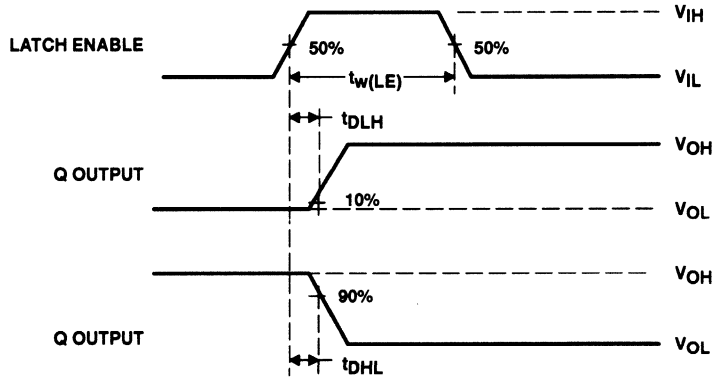


Figure 4. Voltage Waveforms for Delay Times, LATCH ENABLE to Q Outputs

SLDS031A – D2744, APRIL 1985 – REVISED APRIL 1993

- **Each Device Drives 32 Electrodes**
- **90-V Output Voltage Swing Capability Using Ramped Supply**
- **15-mA Output Source and Sink Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **Totem-Pole Outputs**
- **Latches on All Driver Outputs**

description

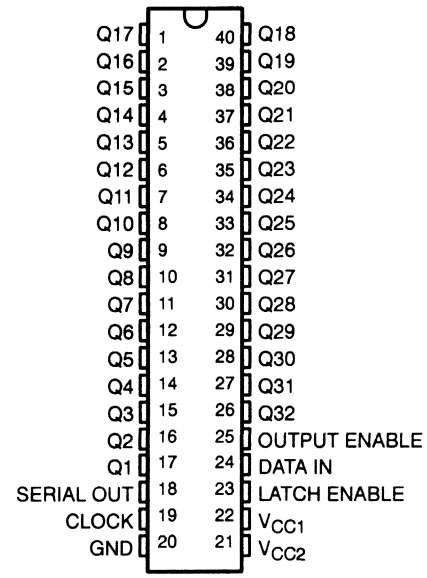
The SN65555, SN75555, SN65556, and SN75556 are monolithic BIDFET† integrated circuits designed to drive the column electrodes of an electroluminescent display. The SN65556 and SN75556 output sequence is reversed from the SN65555 and SN75555 for ease in printed-circuit-board layout.

The devices consist of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. When high, LATCH ENABLE transfers the shift register contents to the outputs of the 32 latches. When OUTPUT ENABLE is high, all Q outputs are enabled. Data must be loaded into the latches and OUTPUT ENABLE must be high before supply voltage V_{CC2} is ramped up.

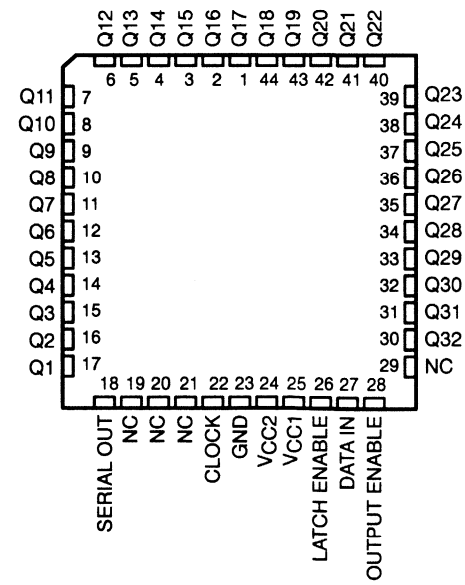
Serial data output from the shift register can be used to cascade shift registers. This output is not affected by LATCH ENABLE or OUTPUT ENABLE.

The SN65555 and SN65556 are characterized for operation from –40°C to 85°C. The SN75555 and SN75556 are characterized for operation from 0°C to 70°C.

SN75555 . . . N PACKAGE
(TOP VIEW)



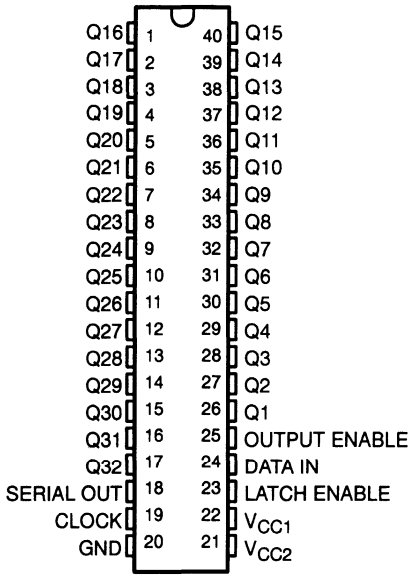
SN65555, SN75555 . . . FN PACKAGE
(TOP VIEW)



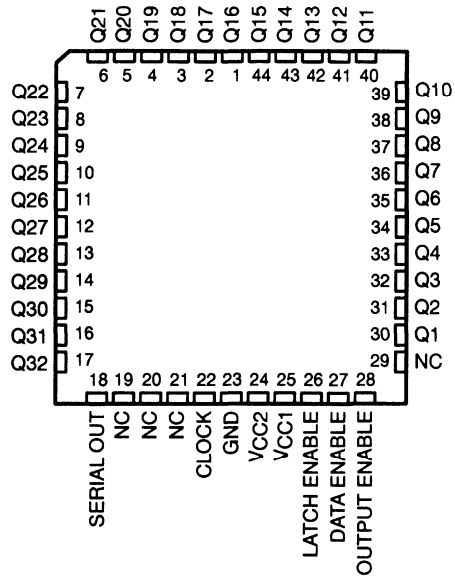
NC – No internal connection

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

SN65556, SN75556
N PACKAGE
(TOP VIEW)



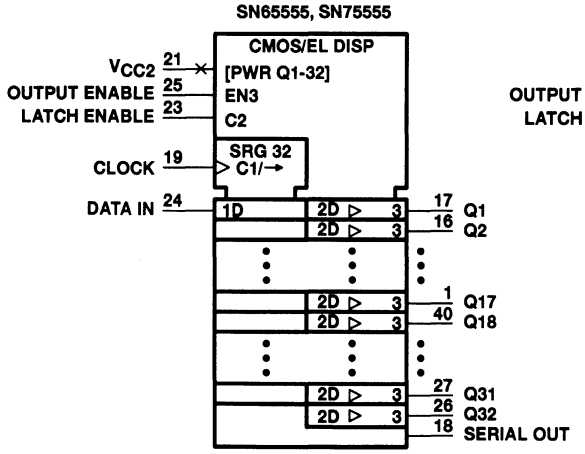
SN65556, SN75556
FN PACKAGE
(TOP VIEW)



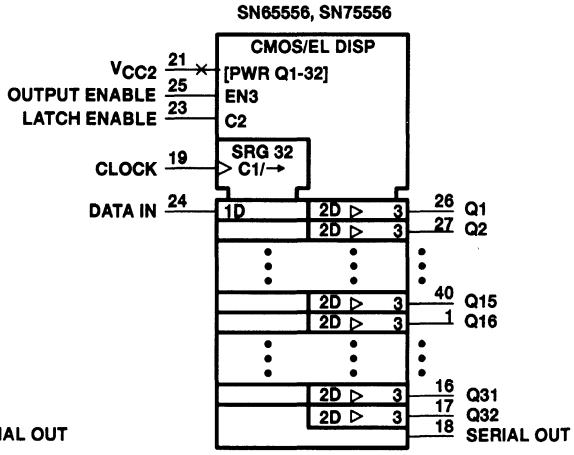
NC – No internal connection

logic symbols†

SN65555, SN75555

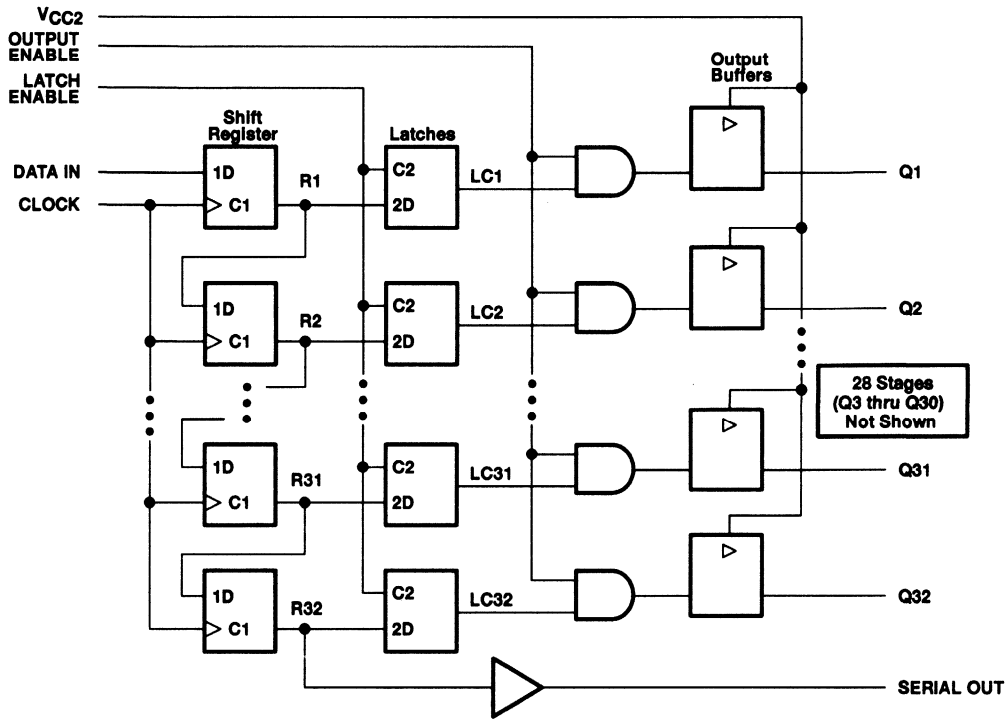


SN65556, SN75556



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for N packages.

logic diagram (positive logic)



FUNCTION TABLE

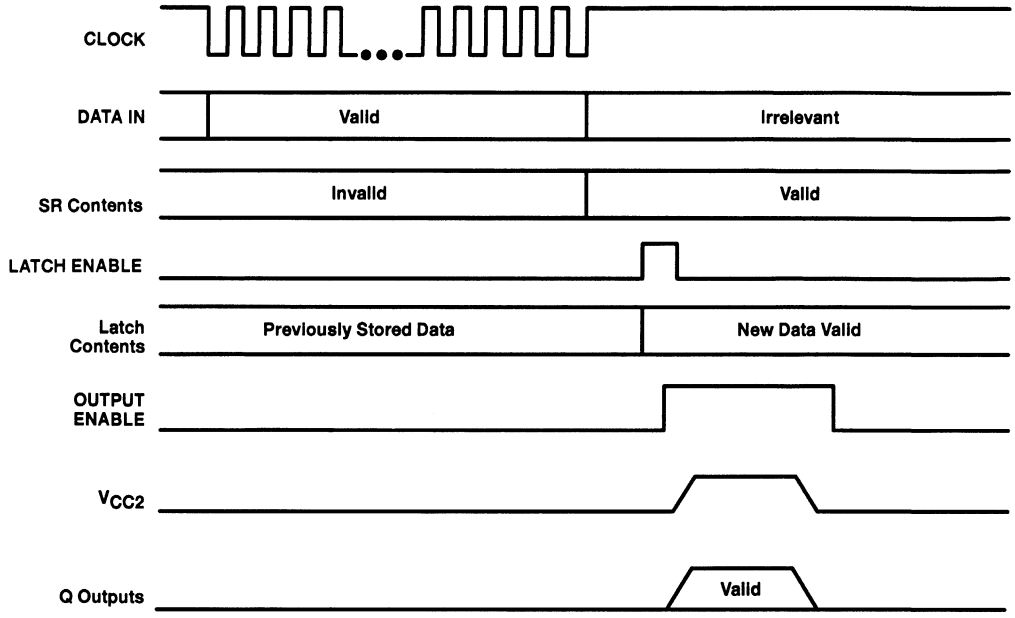
FUNCTION	CONTROL INPUTS			SHIFT REGISTER R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS	
	CLOCK	LATCH ENABLE	OUTPUT ENABLE			SERIAL	Q1 THRU Q32
Load	↑	X	X	Load and shift†	Determined by	R32	Determined by OUTPUT ENABLE
	No↑	X	X	No change	LATCH ENABLE‡	R32	
Latch	X	L	X	As determined above	Stored data	R32	Determined by OUTPUT ENABLE
	X	H	X		New data		
Output Enable	X	X	L	As determined above	Determined by	R32	All L
	X	X	H		LATCH ENABLE‡	R32	LC1 thru LC21, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

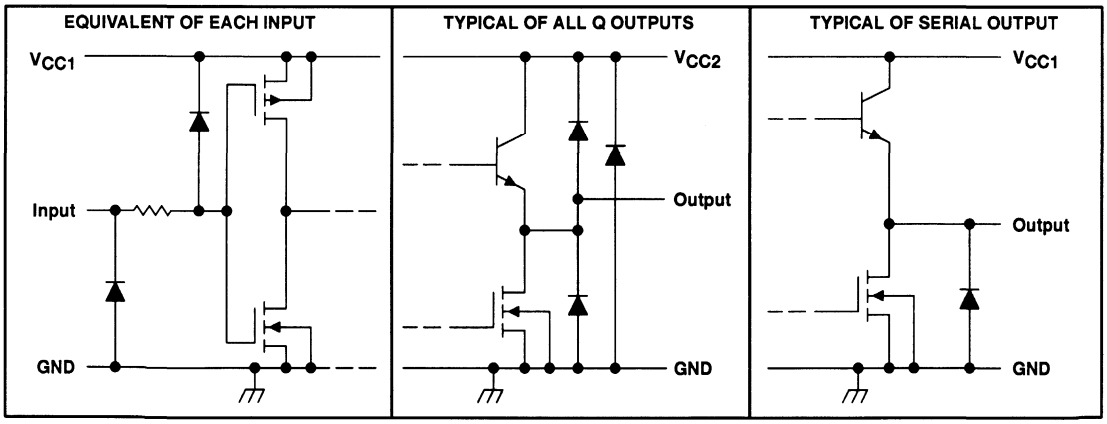
† R32 and the serial output take on the state of R31, R31 takes on the state of R30,. . .R2 takes on the state of R1, and R1 takes on the state of the data input.

‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 18 V
Supply voltage, V_{CC2} (see Note 2) ..... 90 V
Input voltage, V_I ..... V_{CC1} + 0.3 V
Ground current ..... 700 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: SN65555, SN65556 ..... – 40°C to 85°C
SN75555, SN75556 ..... 0°C to 70°C
Storage temperature range ..... –65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTES: 1. Voltage values are with respect to network GND.
2. These devices have been designed to be used in applications in which the high-voltage supply, V_{CC2}, is switched to GND before changing the state of the outputs.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1700 mW	13.6 mW/°C	1088 mW	884 mW
N	1250 mW	10.0 mW/°C	800 mW	650 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	15	V
Supply voltage, V_{CC2}		0		80	V
High-level input voltage, V_{IH} (see Figure 1)	V_{CC1} = 10.8 V	8.1		11.1	V
	V_{CC1} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)	V_{CC1} = 10.8 V	–0.3†		2.7	V
	V_{CC1} = 15 V	–0.3†		3.75	
High-level output current, I_{OH}				–15	mA
Low-level output current, I_{OL}				15	mA
Output clamp current, I_{OK}				20	mA
Clock frequency, f_{clock}		0		6.25	MHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$ (see Figure 2)		80			ns
Pulse duration, LATCH ENABLE, $t_{w(LE)}$		80			ns
Setup time, t_{su}	DATA IN before CLOCK ↑ (see Figure 2)	20			ns
	OUTPUT ENABLE before V_{CC2}↑ (see Figure 4)	500			
Hold time, t_h	DATA IN after CLOCK ↑ (see Figure 2)	80			ns
	OUTPUT ENABLE after V_{CC2}↑ (see Figure 4)	100			
Rate of rise for V_{CC2}, dv/dt				80	V/μs
Operating free-air temperature, T_A	SN65555, SN65556	–40		85	°C
	SN75555, SN75556	0		85	

† The algebraic convention, in which the least positive (most negative) value is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 12 V, V_{CC2} = 80 V

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = –15 mA	77		V
		SERIAL OUT	I_O = –100 µA	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 15 mA		8	V
		SERIAL OUT	I_{OL} = 100 µA		1	
I_{IH}	High-level input current		V_I = 12 V		1	µA
I_{IL}	Low-level input current		V_I = 0		–1	µA
I_{CC1}	Supply current from V_{CC1}				2	mA
I_{CC2}	Supply current from V_{CC2}				5	mA

switching characteristics, V_{CC1} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level, SERIAL OUT from CLOCK	C_L = 20 pF to GND, V_{CC2} = 0, See Figure 3		140	ns
t_{PLH}	Propagation delay time, low-to-high level, SERIAL OUT from CLOCK			140	ns
t_d	Delay time, V_{CC2} to Q outputs	dv/dt = 80 V/µs, See Figure 4		100	ns

RECOMMENDED OPERATING CONDITIONS

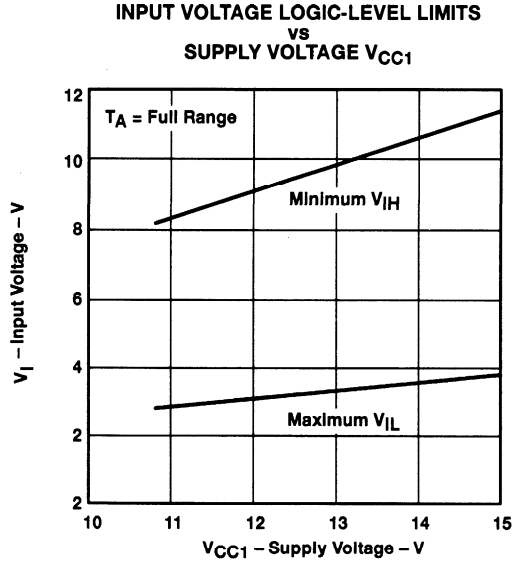


Figure 1

PARAMETER MEASUREMENT INFORMATION

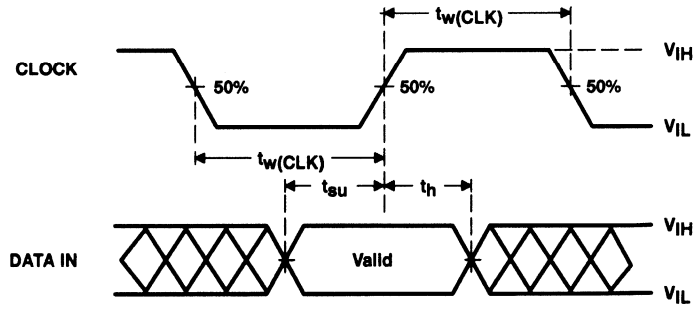


Figure 2. Input Timing Voltage Waveforms

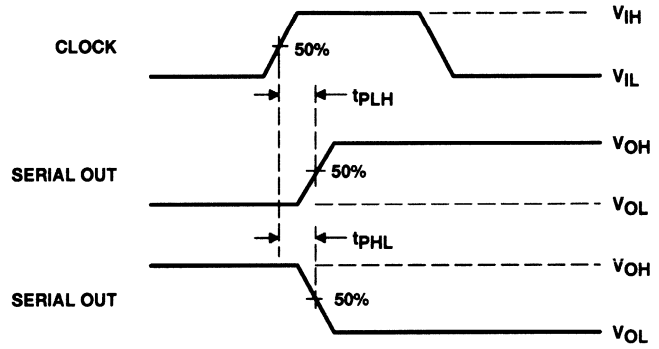


Figure 3. Voltage Waveforms for Propagation Delay Time, CLOCK to SERIAL OUT

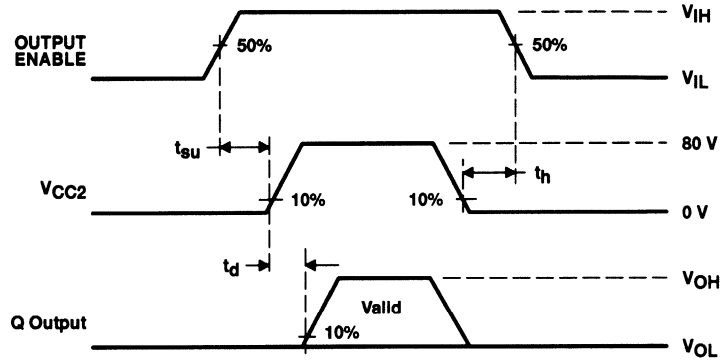


Figure 4. Voltage Waveforms for Delay Times, V_{CC2} to Q Outputs

SLDS018B – D2999, DECEMBER 195 – REVISED APRIL 1993

- **Each Device Drives 32 Electrodes**
- **High-Voltage Open-Collector NPN Outputs Using Ramped Supply**
- **300-mA Output Current Capability**
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

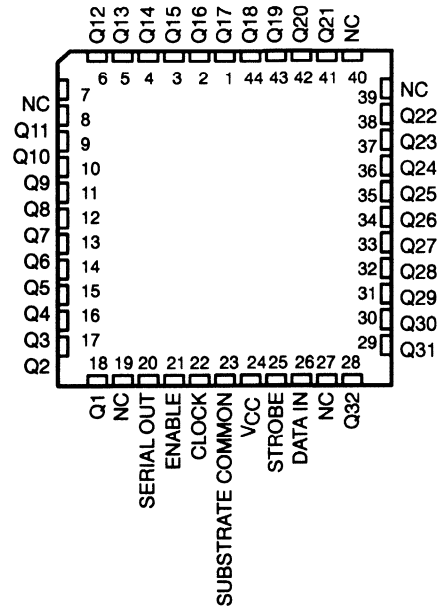
description

These devices are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS-compatible, and all outputs are high-voltage open-collector npn transistors.

The devices consist of a 32-bit shift register, 32 AND gates, and 32 output OR gates. Typically, a composite row drive signal is externally generated by a high-voltage switching circuit and applied to SUBSTRATE COMMON. Serial data is entered into the shift register on the high-to-low transition of the clock input. A high ENABLE allows those outputs with a high in their associated register to be turned on causing the corresponding row to be connected to the composite row drive signal. When STROBE is low, all output transistors are turned on. The serial data output (SERIAL OUT) from the shift register can be used to cascade additional devices. This output is not affected by the ENABLE or STROBE inputs.

The SN65558 is characterized for operation from −40°C to 85°C. The SN75558 is characterized for operation from 0°C to 70°C.

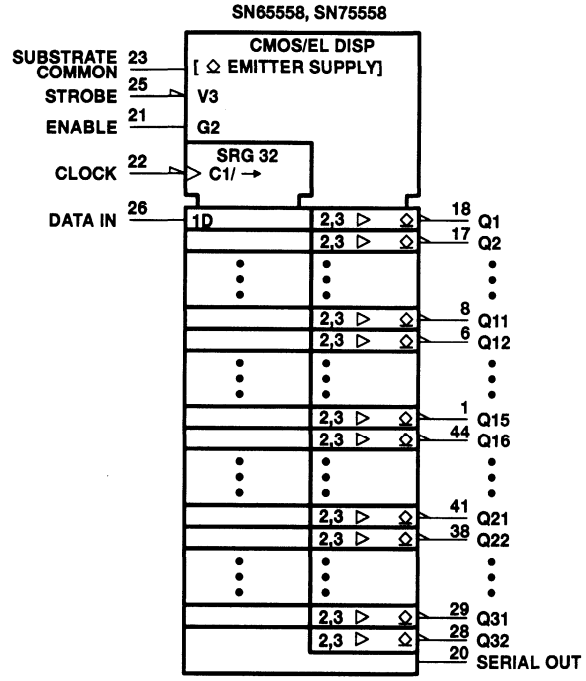
FN PACKAGE
(TOP VIEW)



NC – No internal connection

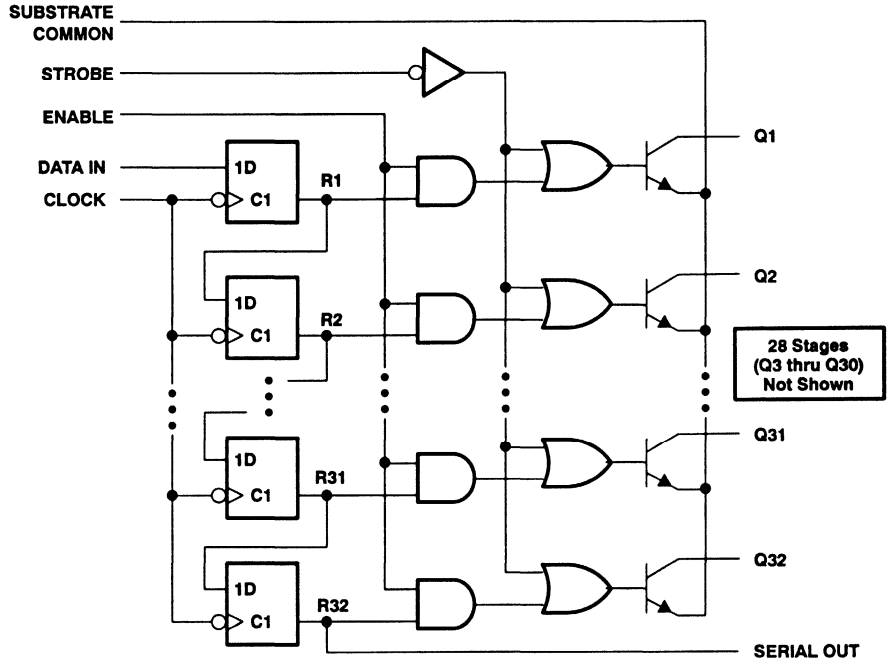
† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



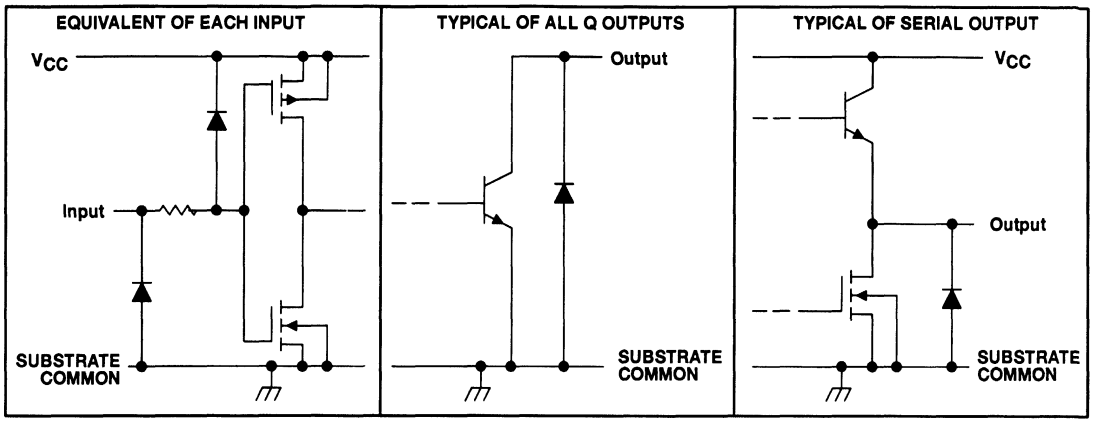
FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	ENABLE	STROBE		SERIAL	Q1 THRU Q32
Load	↓	X	X	Load and shift†	R32	Determined by ENABLE and STROBE
	No ↓	X	X	No change	R32	Determined by ENABLE and STROBE
Enable	X	L	H	As determined above	R32	All Q outputs off
	X	H	H	As determined above	R32	Determined by R1 through R32
Strobe	X	X	L	As determined above	R32	All Q outputs on

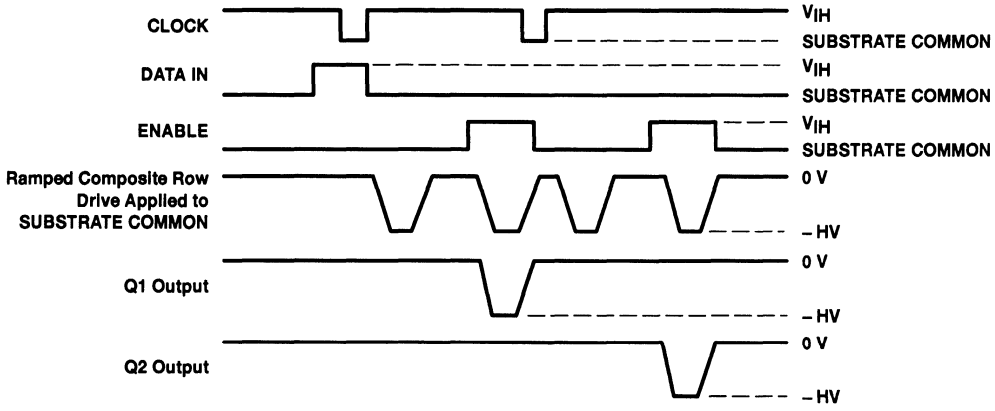
H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition

† Register R32 takes on the state of R31, R31 takes on the state of R30, . . .R2 takes on the state of R1, and R1 takes on the state of the data input.

schematic of inputs and outputs



typical operating sequence



HV = High voltage

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 18 V
Off-state output voltage, $V_{O(off)}$ (see Note 2) ..... 110 V
Input voltage, V_I ..... V_{CC} + 0.3 V
Substrate common terminal current (see Note 3) ..... 750 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 4) ..... 1700 mW
Operating free-air temperature range: SN65558 ..... – 40°C to 85°C
SN75558 ..... 0°C to 70°C
Storage temperature range ..... – 65°C to 150°C
Case temperature for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to SUBSTRATE COMMON.
2. Data must be clocked into the shift register and Q outputs enabled prior to ramping SUBSTRATE COMMON to –HV (see typical operating sequence).
3. Duty cycle is limited by package dissipation.
4. For operation above 25°C free-air temperature, derate linearly to 1088 mW at 70°C, and 884 mW at 85°C at the rate of 13.6 mW/°C.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}			10.8	12	15	V
High-level input voltage, V_{IH} (see Figure 1)		V_{CC} = 10.8 V	8.1		11.1	V
		V_{CC} = 15 V	11.25		15.3	
Low-level input voltage, V_{IL} (see Figure 1)		V_{CC} = 10.8 V	–0.3		2.7	V
		V_{CC} = 15 V	–0.3		3.75	
Off-state Q output voltage, $V_{O(off)}$			–0.3		100	V
On-state Q output current, $I_{O(on)}$, duty cycle ≤ 1%, V_{CC} = 15 V					300	mA
Rate of rise for SUBSTRATE COMMON, dv/dt					100	V/μs
Clock frequency, f_{clock}			0		4	MHz
Pulse duration, CLOCK high or low, t_w			125			ns
Setup time, t_{su}	DATA IN before CLOCK↓ (see Figure 2)		50			ns
	ENABLE before SUBSTRATE COMMON ↓ (see Figure 4)		500			
Hold time, DATA IN after CLOCK↓, t_h (see Figure 2)			100			ns
Operating free-air temperature, T_A		SN65558	–40		85	°C
		SN75558	0		70	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 12 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN65558		SN75558		UNIT
				MIN	MAX	MIN	MAX	
$I_{O(off)}$	Off-state Q output current		V_O = 100 V		20		10	μA
V_{OH}	High-level output voltage	SERIAL OUT	I_O = –100 μA	10.5		10.5		V
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 300 mA		20		10	V
		SERIAL OUT	I_{OL} = 100 μA		1		1	
I_{IH}	High-level input current		V_I = 12 V		1		1	μA
I_{IL}	Low-level input current		V_I = 0		–1		–1	μA
I_{CC}	Supply current from V_{CC}				250		250	μA

switching characteristics, V_{CC} = 12 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level, SERIAL OUT from CLOCK	C_L = 20 pF to SUBSTRATE COMMON, (see Figure 3)		200	ns
t_{PLH}	Propagation delay time, low-to-high-level, SERIAL OUT from CLOCK			200	ns
$t_{d(on)}$	Turn-on delay time, Q outputs from ENABLE	dv/dt = 100 V/µs, STROBE at V_{CC}, R_L = 2 kΩ to 60 V (see Figure 4)		500	ns

RECOMMENDED OPERATING CONDITIONS

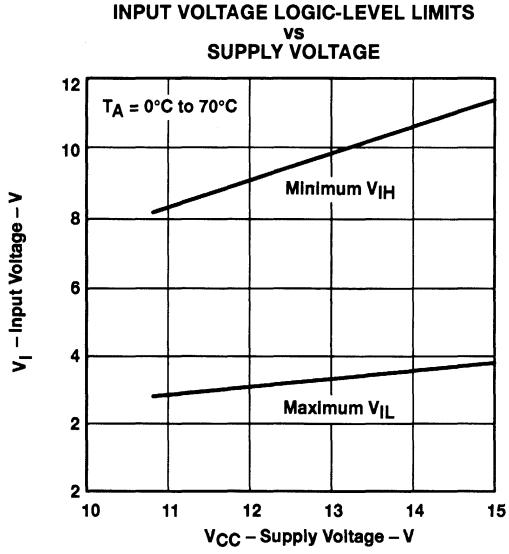


Figure 1

PARAMETER MEASUREMENT INFORMATION

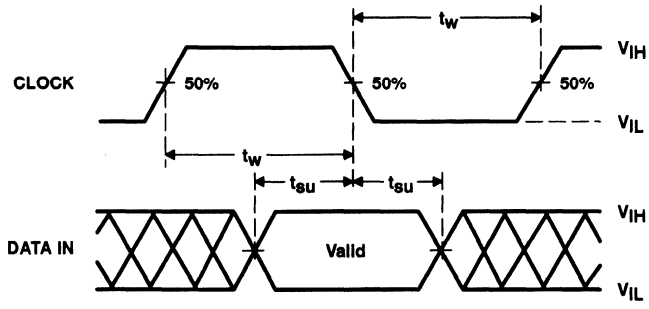


Figure 2. Input-Timing Voltage Waveforms

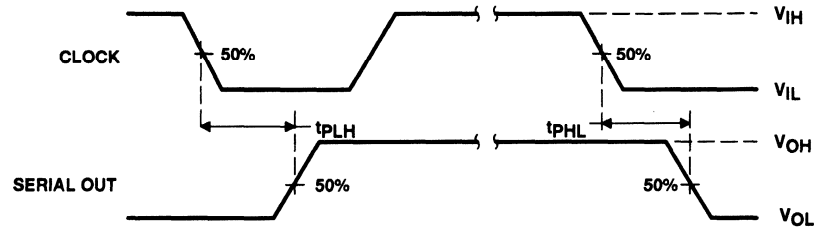


Figure 3. Voltage Waveforms for Propagation Delay Time, CLOCK to SERIAL OUT

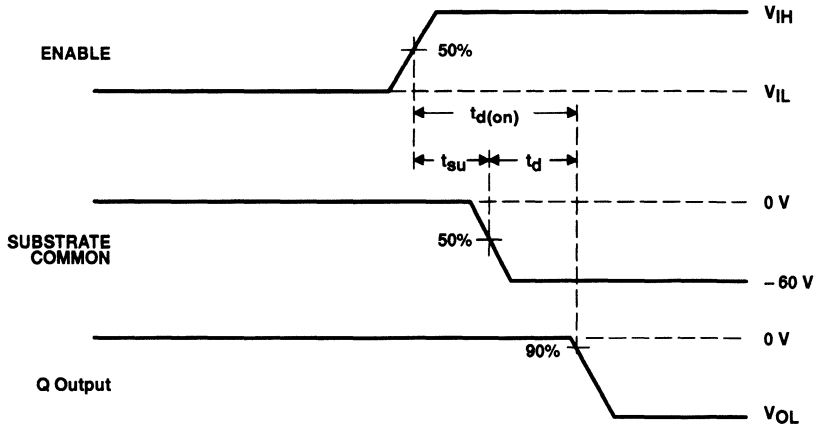


Figure 4. Voltage Waveforms for Turn-On Delay Time, SUBSTRATE COMMON to Q Output

TYPICAL CHARACTERISTICS

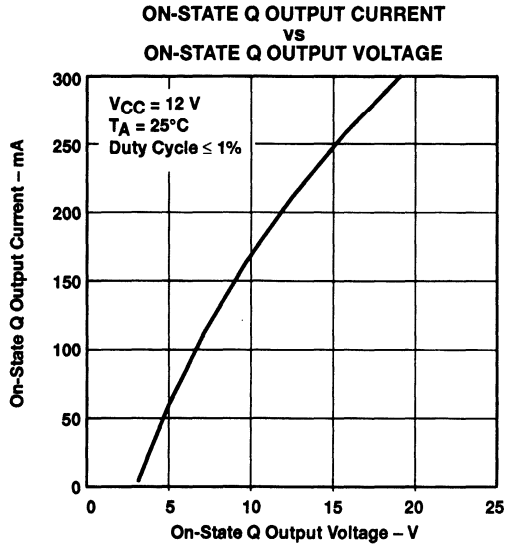
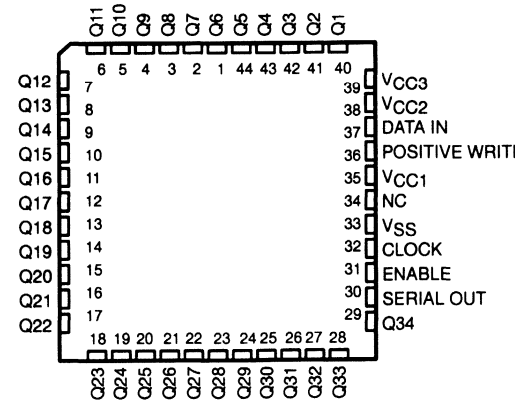


Figure 5

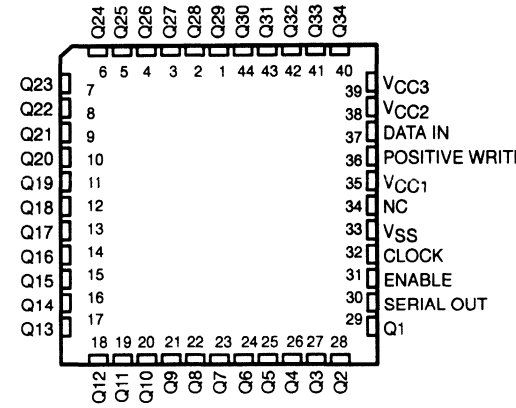
SLDS019D – D3223, MAY 1986 – REVISED DECEMBER 1989

- **Each Device Drives 34 Electrodes**
- **Selectable Open-Source or Open-Drain Output**
- **Outputs Rated at 240 V**
- **Output Current Capability:**
  –150 mA to 100 mA (SN65')
  –150 mA to 120 mA (SN75')
- **CMOS-Compatible Inputs**
- **Very Low Steady-State Power Consumption**

SN65563A, SN75563A . . . FN PACKAGE
(TOP VIEW)



SN65564A, SN75564A . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN65563A, SN65564A, SN75563A, and SN75564A are monolithic BIDFET† integrated circuits designed to drive the row electrodes of an electroluminescent display. All inputs are CMOS compatible. If POSITIVE WRITE is high, the Q outputs act like open-source outputs and output data is not inverted with respect to input data. If POSITIVE WRITE is low, the Q outputs act like open-drain outputs and output data is inverted with respect to input data. The SN65564A and SN75564A output sequences are reversed from the SN65563A and SN75563A for ease in printed-circuit-board layout.

Typically, composite V_{CC2}, V_{CC3}, and ground signals are externally generated by a high-voltage switching circuit. Serial data is entered into the shift register on the high-to-low transition of CLOCK. A high at the ENABLE input allows those outputs with a high in their associated register to be turned on, causing the corresponding row to be connected to V_{CC2} when POSITIVE WRITE is high or to ground when POSITIVE WRITE is low. V_{CC3} may be tied to V_{CC2} or held 5 V to 15 V above V_{CC2} for better V_{OH} characteristics. SERIAL OUT from the shift register can be used to cascade additional devices. This output is not affected by the ENABLE or POSITIVE WRITE inputs.

The SN65563A and SN65564A are characterized for operation over the full automotive operating temperature range of –40°C to 85°C. The SN75563A and SN75564A are characterized for operation from 0°C to 70°C.

†BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

LOAD FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R34	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
Load	↓	X	X	Load and shift†	R34	Determined by ENABLE and POSITIVE WRITE
	No ↓	X	X	No change	D34	Determined by ENABLE and POSITIVE WRITE

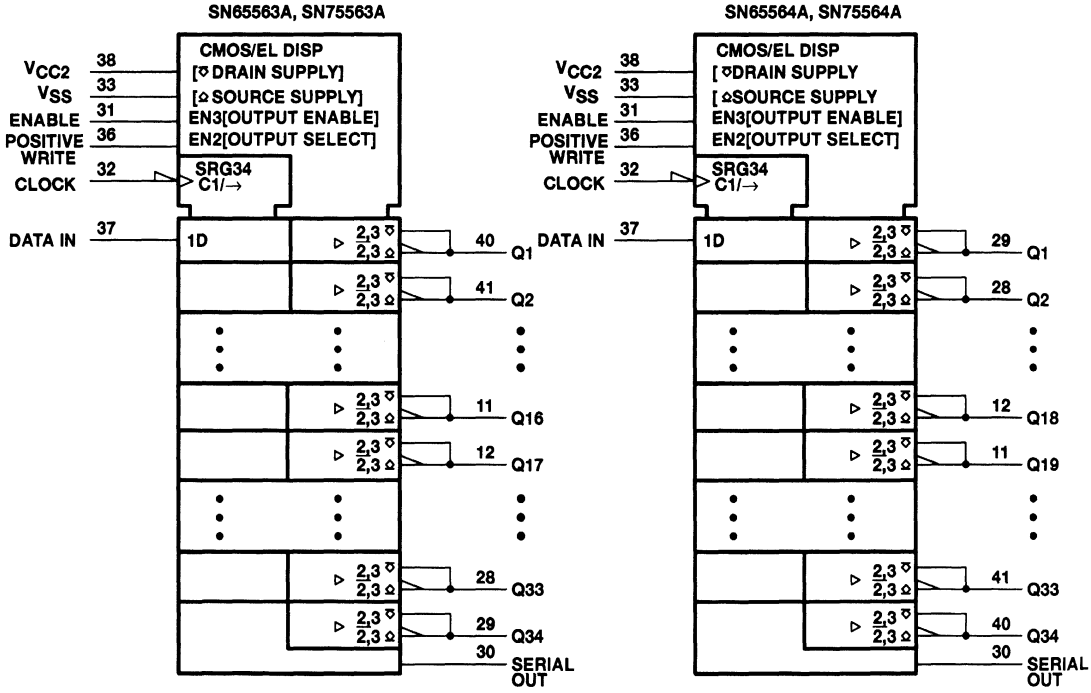
† Register R34 takes on the state of R33, R33 takes on the state of R32, . . . R2 takes on the state of R1, R1 takes on the state of the data input.

OUTPUT CONTROL FUNCTION TABLE

FUNCTION	CONTROL INPUTS			SHIFT REGISTERS CONTENTS Rn FOR R1 THRU R34 (Determined Above)	OUTPUTS	
	CLOCK	ENABLE	POSITIVE WRITE		SERIAL	Q1 THRU Q34
Output Control	X	L	X	X	R34	High impedance
	X	H	H	H	R34	H
	X	H	L	H	R34	L
	X	X	X	L	R34	High impedance

H = high, L = low, X = irrelevant, I = high-to-low transition

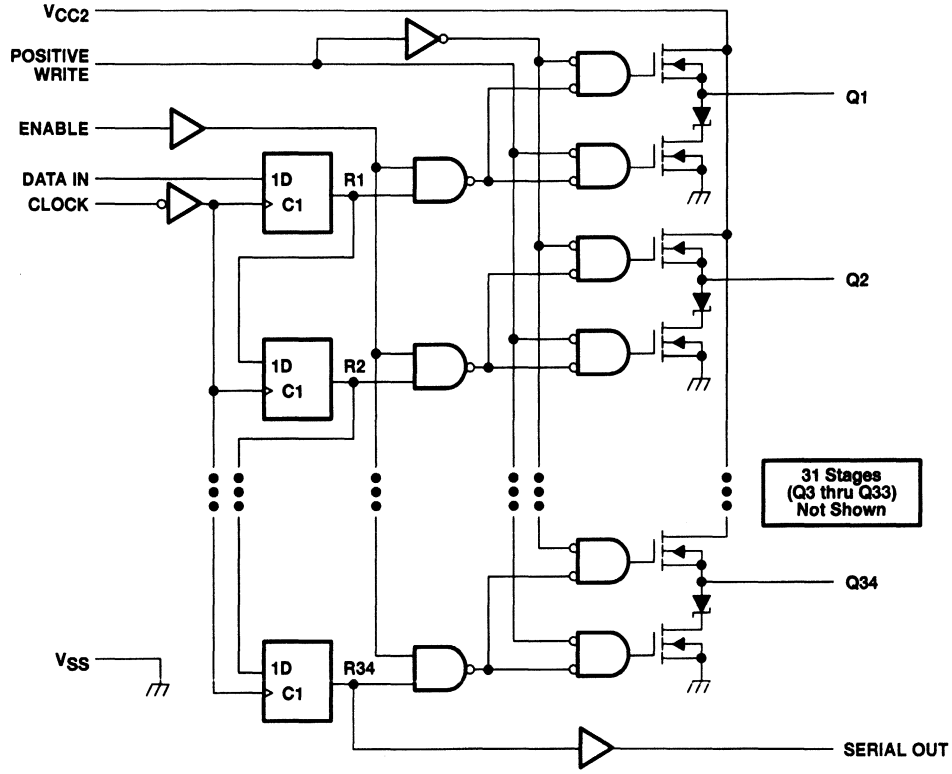
logic symbols‡



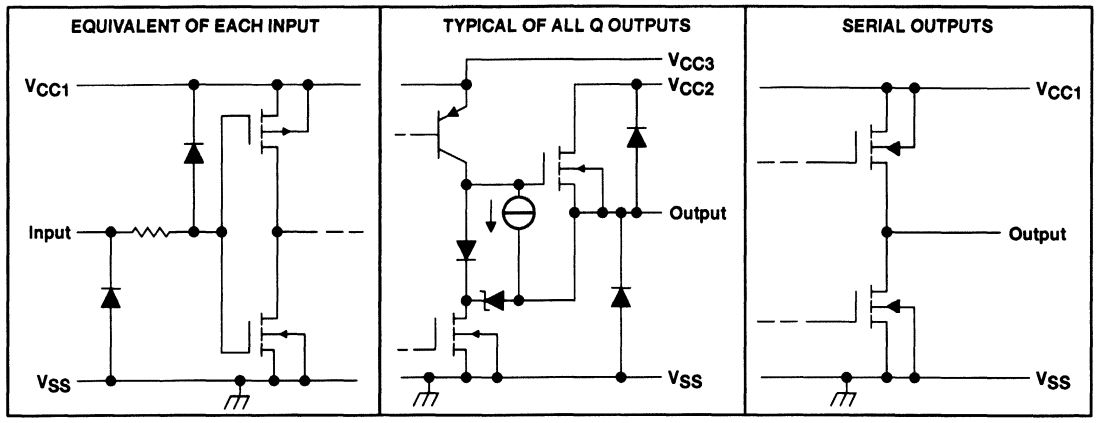
‡ These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SLDS019D – D3223, MAY 1986 – REVISED DECEMBER 1989

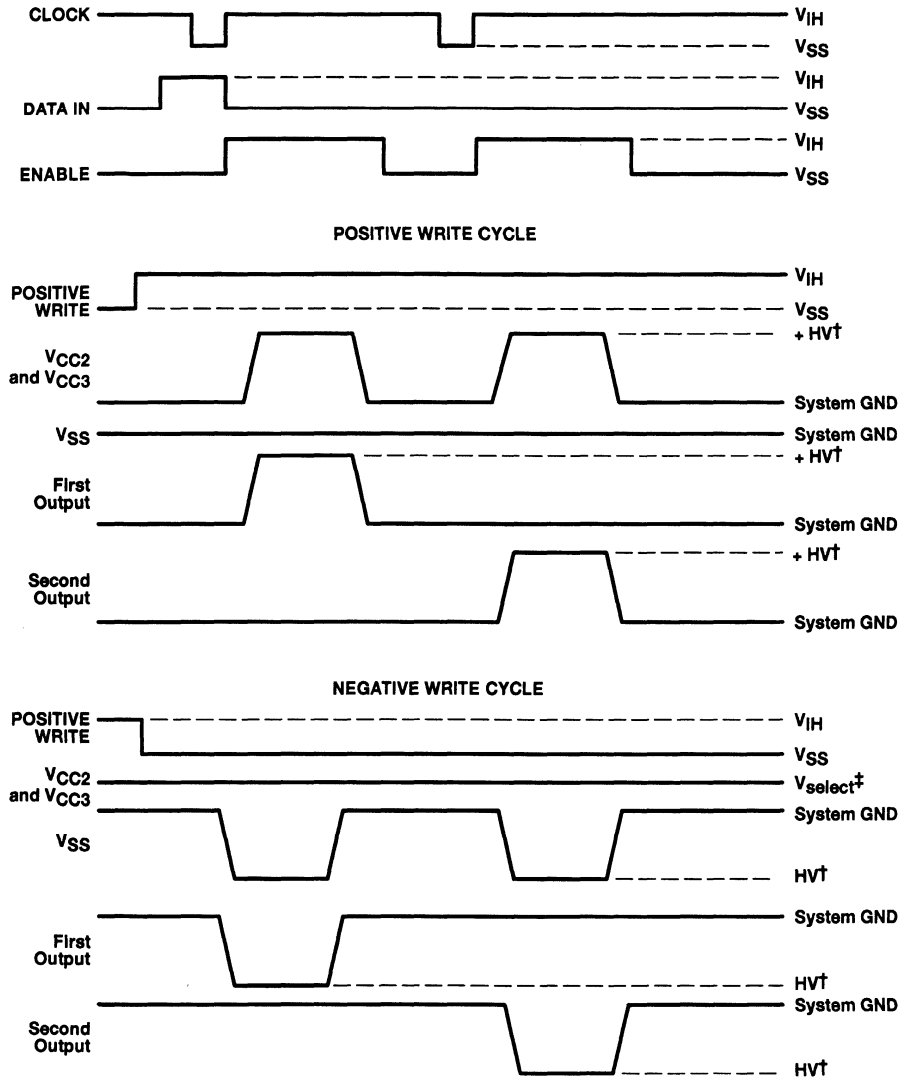
logic diagram (positive logic)



schematics of inputs and outputs



typical operating sequence



† HV = high voltage

‡ During the negative write cycle, the V_{CC2} and V_{CC3} supplies are in a high-impedance state.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 15 V
Supply voltage, V_{CC2} ..... 240 V
Supply voltage, V_{CC3} ..... 240 V
Supply voltage, V_{SS} ..... −240 V
Input voltage range, V_I ..... −0.3 V to V_{CC1} + 0.3 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1700 mW
Operating free-air temperature range: SN65563A, SN65564A ..... −40°C to 85°C
SN75563A, SN75564A ..... 0°C to 70°C
Storage temperature range ..... −40°C to 125°C
Case temperature for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate to 1088 mW at 70°C or 884 mW at 85°C at the rate of 13.6 mW/°C.

recommended operating conditions (see Note 1 and Figures 1 and 2)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		7.5	12	13.2	V
Supply voltage, V_{CC2}		$V_{CC3}-15$		V_{CC3}	V
Supply voltage, V_{CC3}		0		235	V
Supply voltage, V_{SS}		0		−235	V
High-level input voltage, V_{IH}		$0.75V_{CC1}$		$V_{CC1}+0.3$	V
Low-level input voltage, V_{IL}		−0.3†		$0.25V_{CC1}$	V
High-level output current, I_{OH}	SN65563A, SN65564A			−100	mA
	SN75563A, SN75564A			−120	
Low-level output current, I_{OL}				150	mA
Output clamp current, I_{OK}				±150	mA
Clock frequency, f_{clock}				4	MHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$		125			ns
Setup time, DATA IN high or low before CLOCK↓, t_{su1}		100			ns
Setup time, CLOCK low before V_{CC2}↑ or V_{SS}↓, t_{su2}		300			ns
Setup time, ENABLE high before V_{CC2}↑ or V_{SS}↓, t_{su3}		300			ns
Setup time, POSITIVE WRITE high or low before V_{CC2}↑ or V_{SS}↓, t_{su4}		300			ns
Hold time, DATA IN high or low after CLOCK↓, t_{h1}		100			ns
Hold time, CLOCK high after V_{CC2}↓ or V_{SS}↑, t_{h2}		300			ns
Hold time, ENABLE high after V_{CC2}↓ or V_{SS}↑, t_{h3}		0			ns
Hold time, POSITIVE WRITE after V_{CC2}↓ or V_{SS}↑, t_{h4}		0			ns
Hold time, ENABLE low between successive V_{CC2}↑, t_{h5}	SN65563A, SN65564A	12			μs
	SN75563A, SN75564A	10			
Hold time, ENABLE low between successive V_{SS}↓, t_{h6}		300			ns
Operating free-air temperature, T_A	SN65563A, SN65564A	−40		85	°C
	SN75563A, SN75564A	0		70	

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating ranges of V_{CC1} and free-air temperature range, V_{CC2} = 235 V, V_{CC3} = 235 V, V_{SS} = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_O = –70 mA	V_{CC2}–30		V
		SERIAL OUT	I_O = –100 µA	10.5		
V_{OL}	Low-level output voltage	Q outputs	I_O = 150 mA		30	V
		SERIAL OUT	I_O = 100 µA		1	
$I_{O(off)}$	Off-state Q output current		V_O = 235 V		50	µA
			V_O = 0		–50	
I_{IH}	High-level input current		V_{IH} = V_{CC1}		100	µA
I_{IL}	Low-level input current		V_{IL} = 0		–100	µA
I_{CC1}	Supply current from V_{CC1}		One Q output high		4	mA
			All Q outputs low or high impedance		2	
I_{CC3}	Supply current from V_{CC3}		One Q output high		10	mA
			All Q outputs low or high impedance		200	µA

switching characteristics over recommended operating range of V_{CC1}, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level serial output from clock	C_L = 50 pF to V_{SS}, See Figures 3 and 4		400	ns
t_{PHL}	Propagation delay time, high-to-low level serial output from clock			400	ns

PARAMETER MEASUREMENT INFORMATION

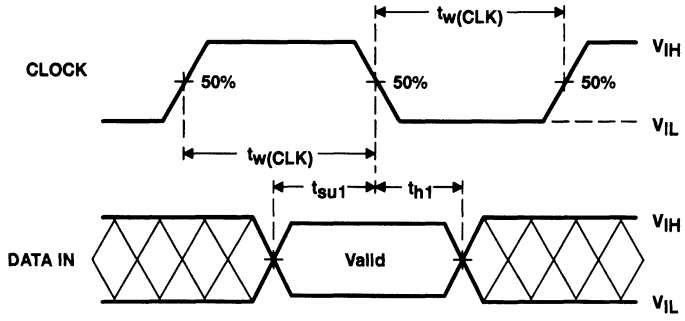
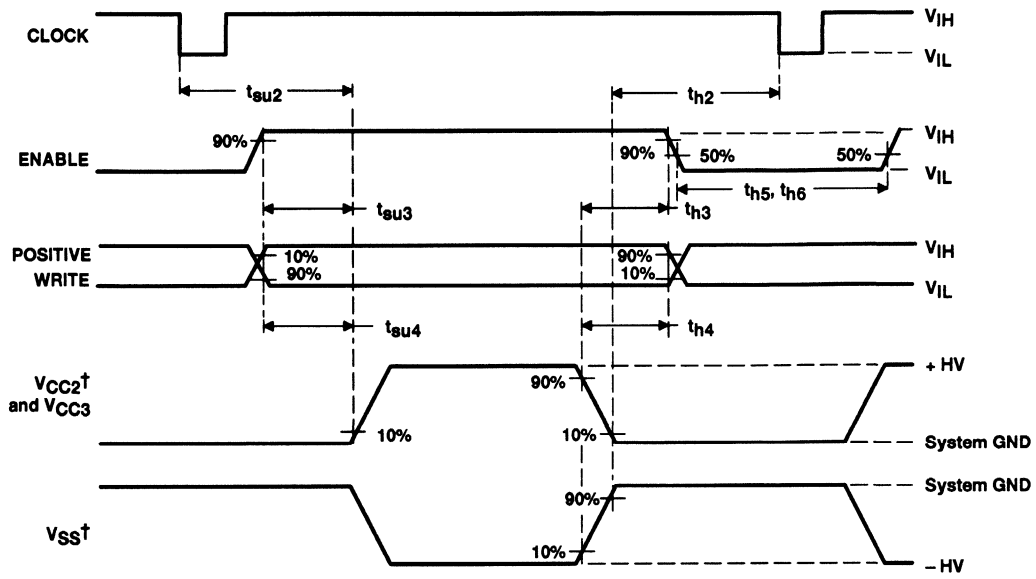


Figure 1. Input Timing Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



† Timing waveforms are with respect to V_{CC2} or V_{SS}, as appropriate.

Figure 2. Control Input Timing Voltage Waveforms

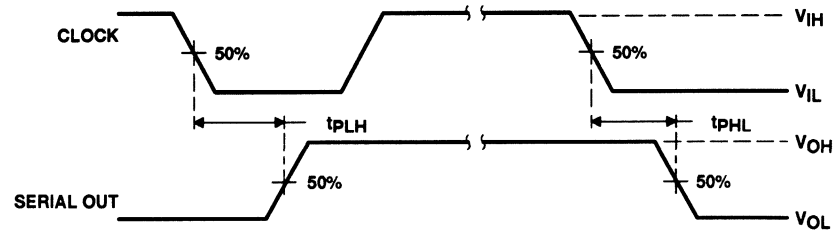
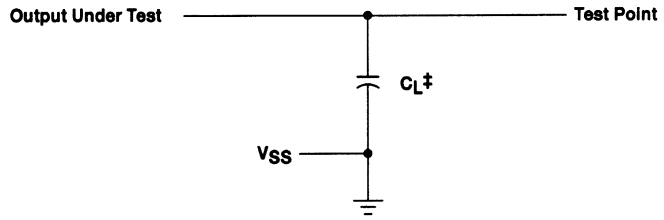


Figure 3. Voltage Waveforms for Propagation Delay Time, CLOCK to SERIAL OUT



‡ C_L includes probe and jig capacitance.

Figure 4. Load Circuit

SLDS034 – D3005, DECEMBER 1986 – REVISED JULY 1989

- **Each Device Drives 32 Lines**
- **180-V Open-Drain Parallel Outputs**
- **220-mA Parallel Output Sink Current Capability**
- **CMOS-Compatible Inputs**
- **Strobe Input Provided**
- **Serial Data Output for Cascade Operation**
- **Inputs Have Built-In Electrostatic Discharge Protection**

description

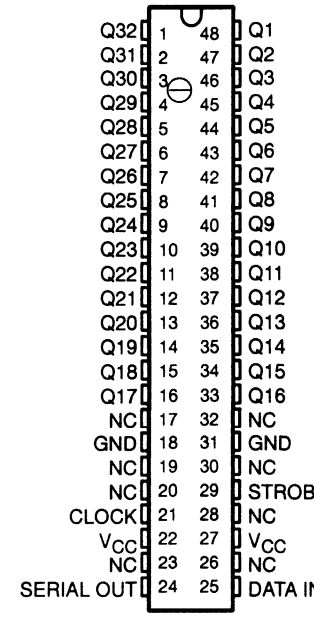
The SN751506 and the SN751516 are monolithic integrated circuits designed to drive the scan lines of a dc plasma panel display. The SN751516 pin sequence is reversed from the SN751506 for ease in printed-circuit-board layout.

Each device consists of a 32-bit shift register and 32 OR gates. Serial data is entered into the shift register on the high-to-low transition of the clock input. When STROBE is low, all Q outputs are in the off state. Outputs are open-drain JFET transistors with a breakdown voltage in excess of 180 V. The outputs have a 220-mA sink current capability in the on state. Only one Q output should be allowed to be in the on state at a time.

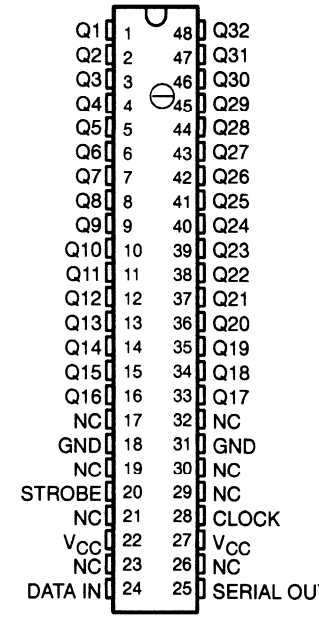
SERIAL OUT from the shift register can be used to cascade shift registers. This output is not affected by the STROBE input. All inputs are CMOS compatible with ESD protection built in.

The SN751506 and SN751516 are characterized for operation from 0°C to 70°C.

SN751506 . . . FT PACKAGE
(TOP VIEW)

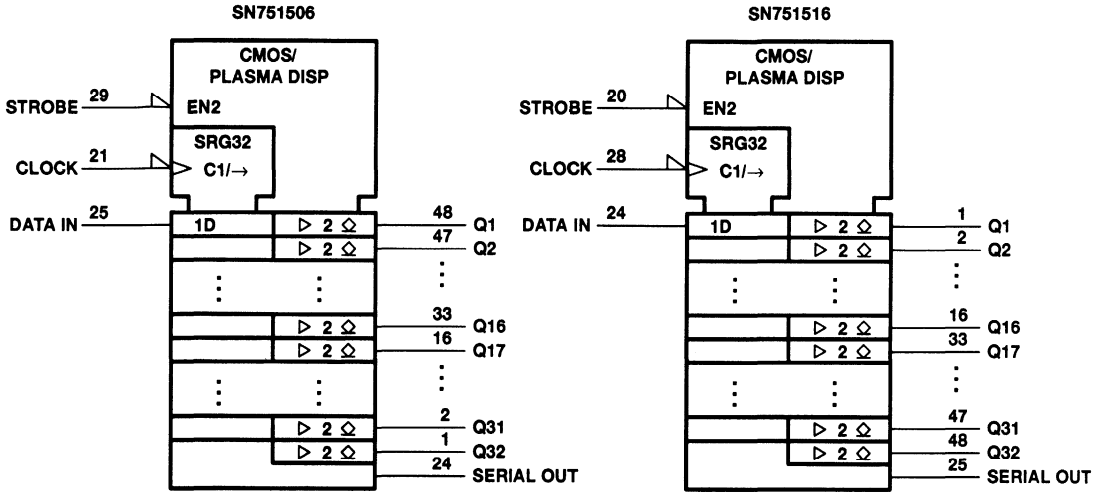


SN751516 . . . FT PACKAGE
(TOP VIEW)



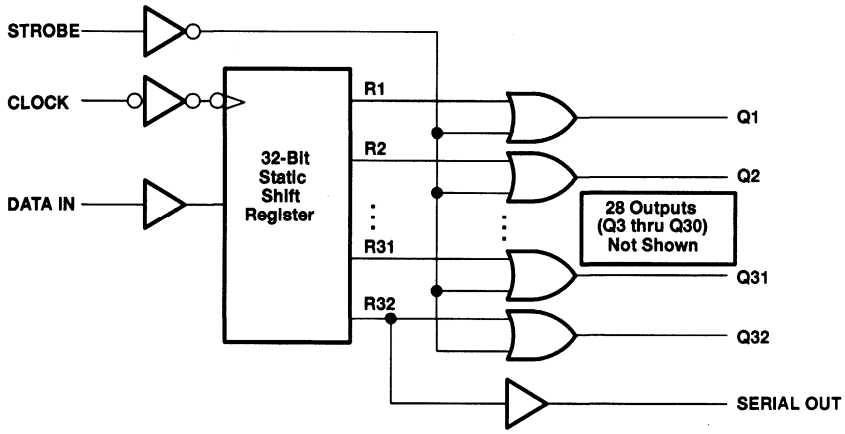
NC – No internal connection

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



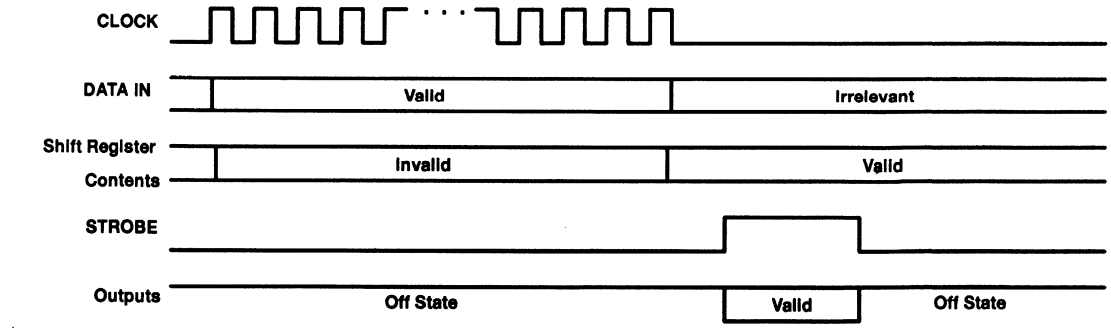
FUNCTION TABLE

FUNCTION	CONTROL INPUTS		SHIFT REGISTERS R1 THRU R32	OUTPUTS	
	CLOCK	STROBE		SERIAL	QI THRU Q32
Load	↓	X	Load and shift‡	R32	Determined by STROBE
	No ↓	X	No change	R32	
Strobe	X	L	As determined above	R32	All high impedance
	X	H		R32	R1 through R32

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition.

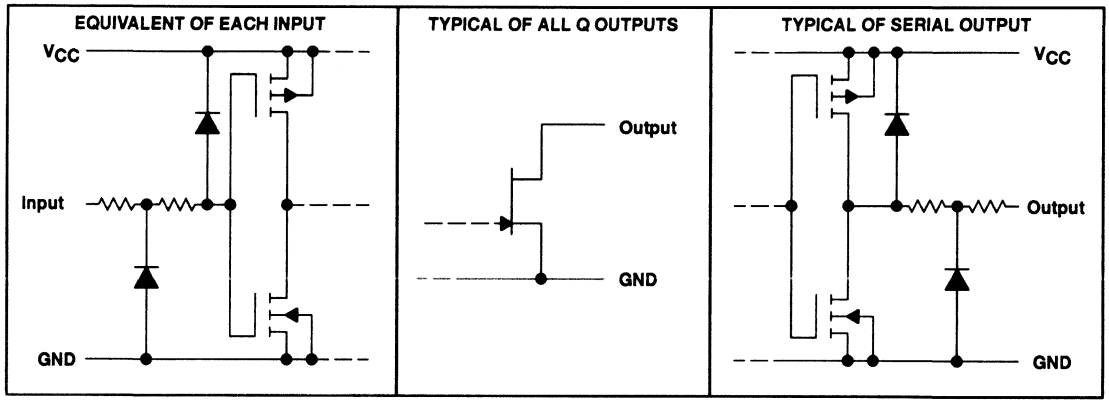
‡ R32 takes on the state of R31, R31 takes on the state of R30, . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



† Only 1 bit in 32 should be low in the input data.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.4 V to 7 V
On-state Q output voltage range, V_O ..... −0.4 V to 125 V
Off-state Q output voltage range, V_O ..... −0.4 V to 180 V
Input voltage range, V_I ..... −0.4 V to V_{CC} + 0.4 V
Serial output voltage range ..... −0.4 V to V_{CC} + 0.4 V
Q output on-state time duration (see Note 2) ..... 100 µs
Q output duty cycle (see Note 2) 1/200
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 3) ..... 1025 mW
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltage values are with respect to GND.
2. Only one Q output should be on at a time.
3. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4	5	6	V
Peak on-state Q output voltage, $V_{O(on)}$				110	V
High-level input voltage, V_{IH}	V_{CC} = 4 V	3.2			V
	V_{CC} = 6 V	4.8			
Low-level input voltage, V_{IL}	V_{CC} = 4 V			0.8	V
	V_{CC} = 6 V			1.2	
Output current, I_O (T_A = 25°C)				220	mA
Clock frequency, f_{clock}				200	kHz
Pulse duration, CLOCK high or low, $t_{w(CLK)}$		1.5†			µs
Pulse duration, DATA, t_{wD}		5			µs
Pulse duration, STROBE, $t_{w(STRB)}$		2			µs
Setup time, DATA IN before CLOCK ↓, t_{su}		1			µs
Hold time, DATA IN after CLOCK↓, t_h		1.2			µs
Operating free-air temperature, T_A		0		70	°C

† The minimum clock period is 5 µs.

electrical characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	SERIAL OUT	I_{OH} = −0.1 mA	4.5			V
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 180 mA		6	10	V
		SERIAL OUT	I_{OL} = 0.1 mA			0.5	
$I_{O(off)}$	Off-state output current	Q outputs	V_{OH} = 110 V			1	µA
I_{OL}	Low-level output current	Q outputs	V_{OL} = 1.6 V	220			mA
I_{IH}	High-level input current		V_I = V_{CC}			1	µA
I_{IL}	Low-level input current		V_I = 0			−1	µA
C_i	Input capacitance					15	pF
I_{CC}	Supply current		All Q outputs off			1	mA
			One Q output on		20	40	

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, CLOCK to SERIAL OUT	C_L = 15 pF		0.2	0.5	µs
t_{DHL}	Delay time, high-to-low-level Q output from STROBE or CLOCK inputs	C_L = 150 pF, R_L = 470 Ω, See Figures 2 and 3		0.2‡	0.6	µs
t_{DLH}	Delay time, low-to-high-level Q output from STROBE or CLOCK inputs			0.35‡	1	µs
t_{THL}	Transition time, high-to-low-level Q output			0.1	0.3	µs
t_{TLH}	Transition time, low-to-high-level Q output			0.35	1	µs

‡ Typical values are for clock Inputs. Typical values from STROBE will be less.

PARAMETER MEASUREMENT INFORMATION

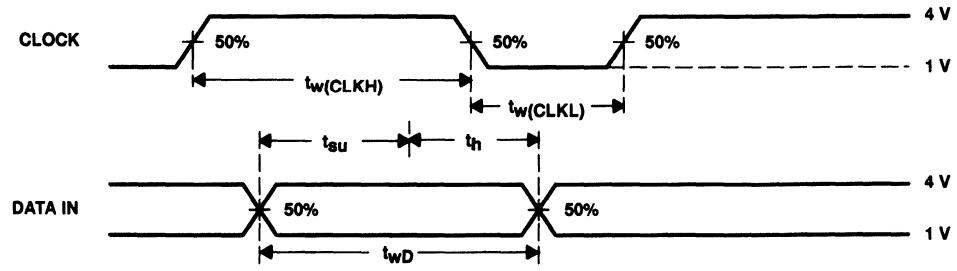


Figure 1. Input Timing Voltage Waveforms

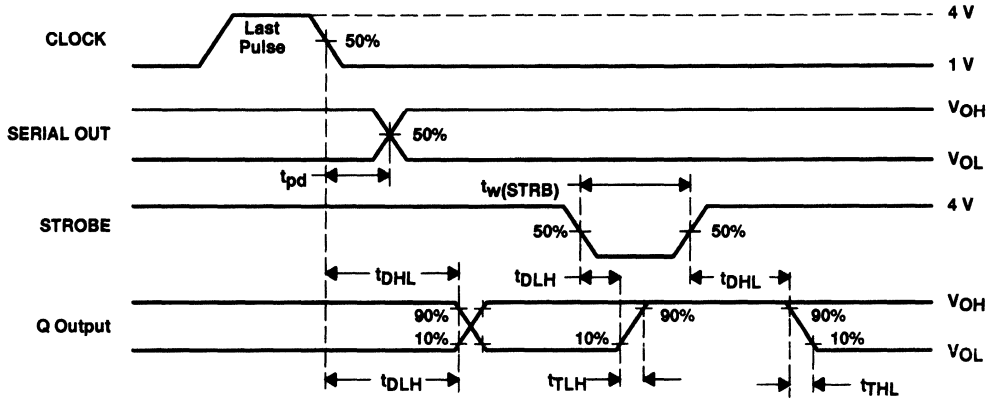
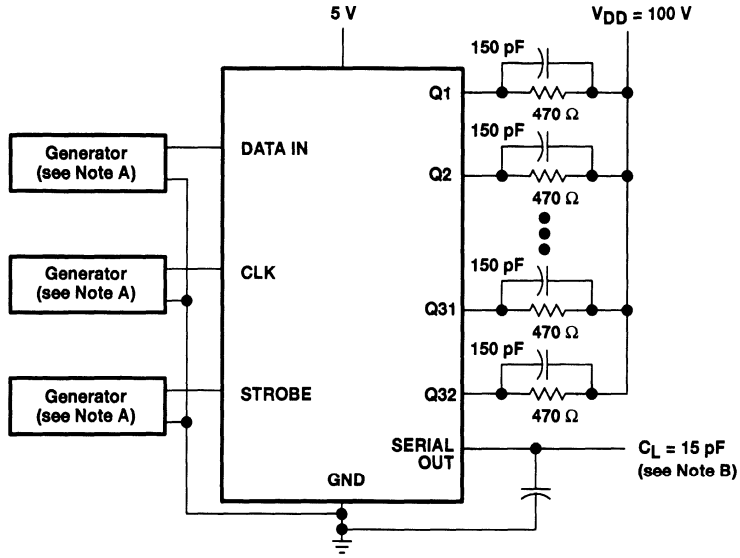


Figure 2. Switching Characteristics

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: t_w = 1.25 μs, PRR ≤ 200 kHz, t_r ≤ 30 ns, t_f ≤ 30 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit

TYPICAL CHARACTERISTICS

LOW-LEVEL Q OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

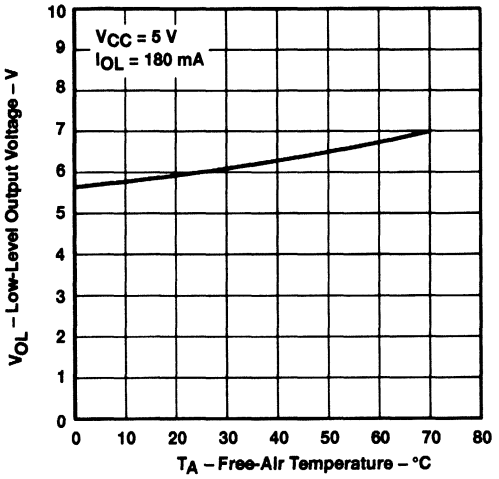


Figure 4

LOW-LEVEL Q OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

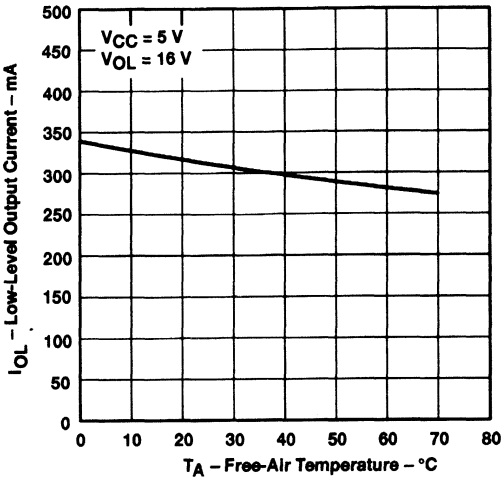


Figure 5

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

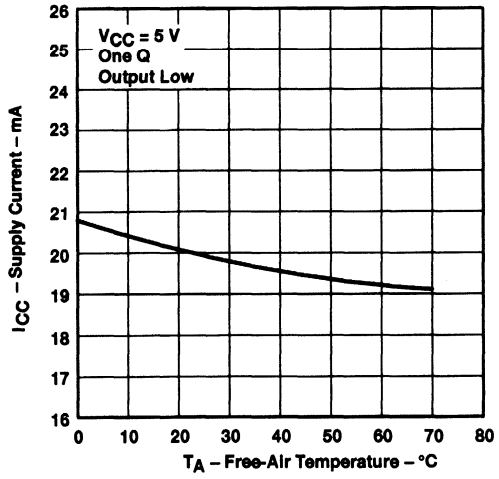


Figure 6

PROPAGATION DELAY TIME,
CLOCK TO SERIAL OUT
vs
FREE-AIR TEMPERATURE

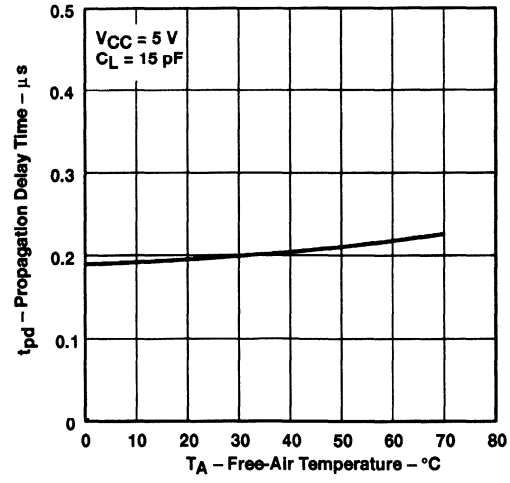


Figure 7

TYPICAL CHARACTERISTICS

DELAY TIME,
HIGH-TO-LOW-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

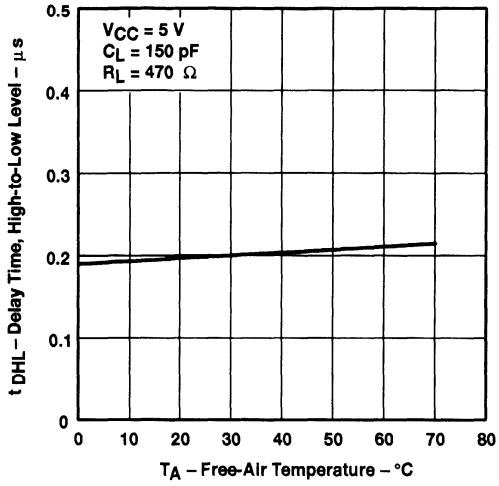


Figure 8

DELAY TIME,
LOW-TO-HIGH-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

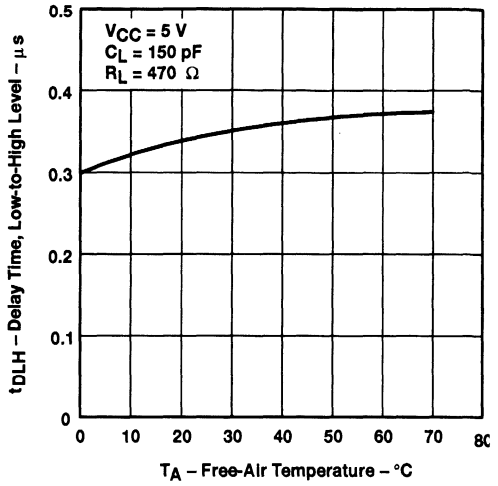


Figure 9

TRANSITION TIME,
HIGH-TO-LOW-LEVEL
vs
FREE-AIR TEMPERATURE

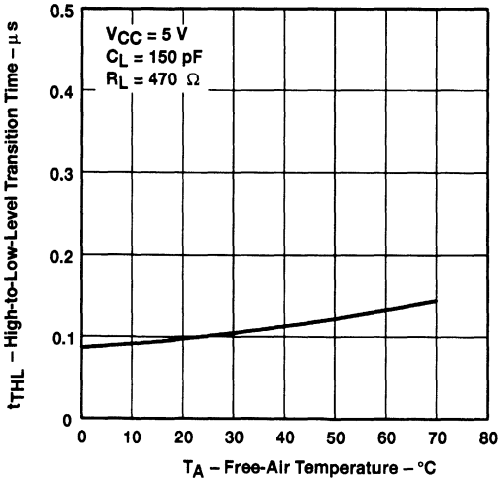


Figure 10

TRANSITION TIME,
LOW-TO-HIGH-LEVEL Q OUTPUT
vs
FREE-AIR TEMPERATURE

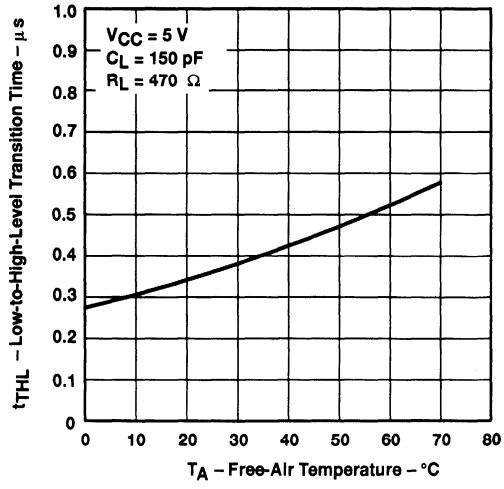


Figure 11

SLDS035 – D2984, JANUARY 1987 – REVISED NOVEMBER 1989

- **Each Device Drives 32 Lines**
- **–120-V PNP Open-Collector Parallel Outputs**
- **High-Speed Serially Shifted Data Inputs**
- **CMOS-Compatible Inputs**
- **Strobe and Sustain Inputs Provided**
- **Serial Data Output for Cascade Operation**

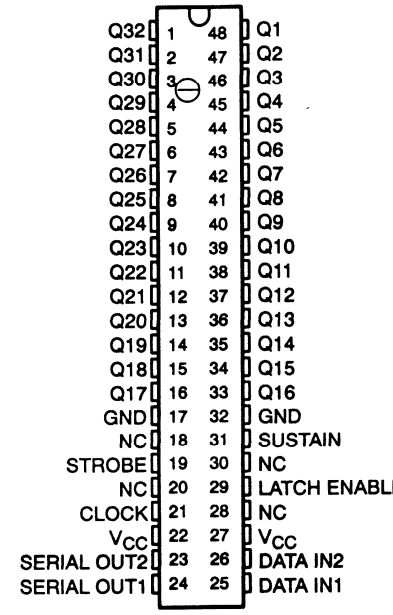
description

The SN751508 and SN751518 are monolithic integrated circuits designed to drive the data lines of a dc plasma panel display. The SN751518 pin sequence is reversed from the SN751508 for ease in printed-circuit-board layout.

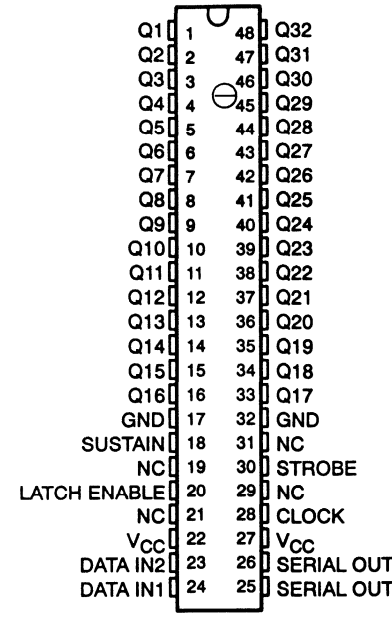
Each device consists of two 16-bit shift registers, 32 latches, 32 OR gates, and 32 pnp open-collector output AND gates. Typically, a 32-bit data string is split into two 16-bit data strings externally and then entered in parallel into the shift registers on the high-to-low transition of the clock signal. A high LATCH ENABLE transfers the data from the shift registers to the inputs of 32 OR gates through the latches. Data present in the latch during the high-to-low transition of LATCH ENABLE is stored. When STROBE is high, the latch is masked and a high is placed on the data input of the output AND gates. When STROBE is low and SUSTAIN is high, data from the latches is reflected at the outputs. When low, SUSTAIN forces all outputs to their off state. Drivers can be cascaded via the serial data outputs of the static shift registers. These outputs are not affected by LATCH ENABLE, STROBE, or SUSTAIN.

The SN751508 and the SN751518 are characterized from 0°C to 70°C.

SN751508 . . . FT PACKAGE
(TOP VIEW)

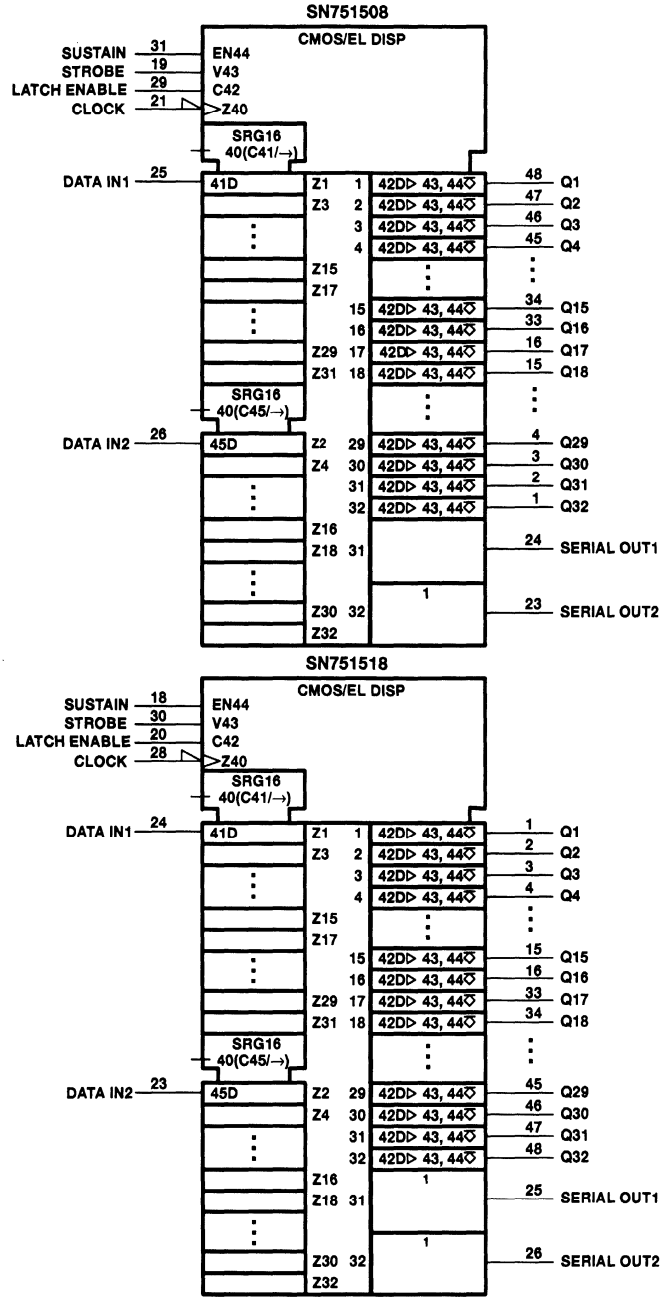


SN751518 . . . FT PACKAGE
(TOP VIEW)



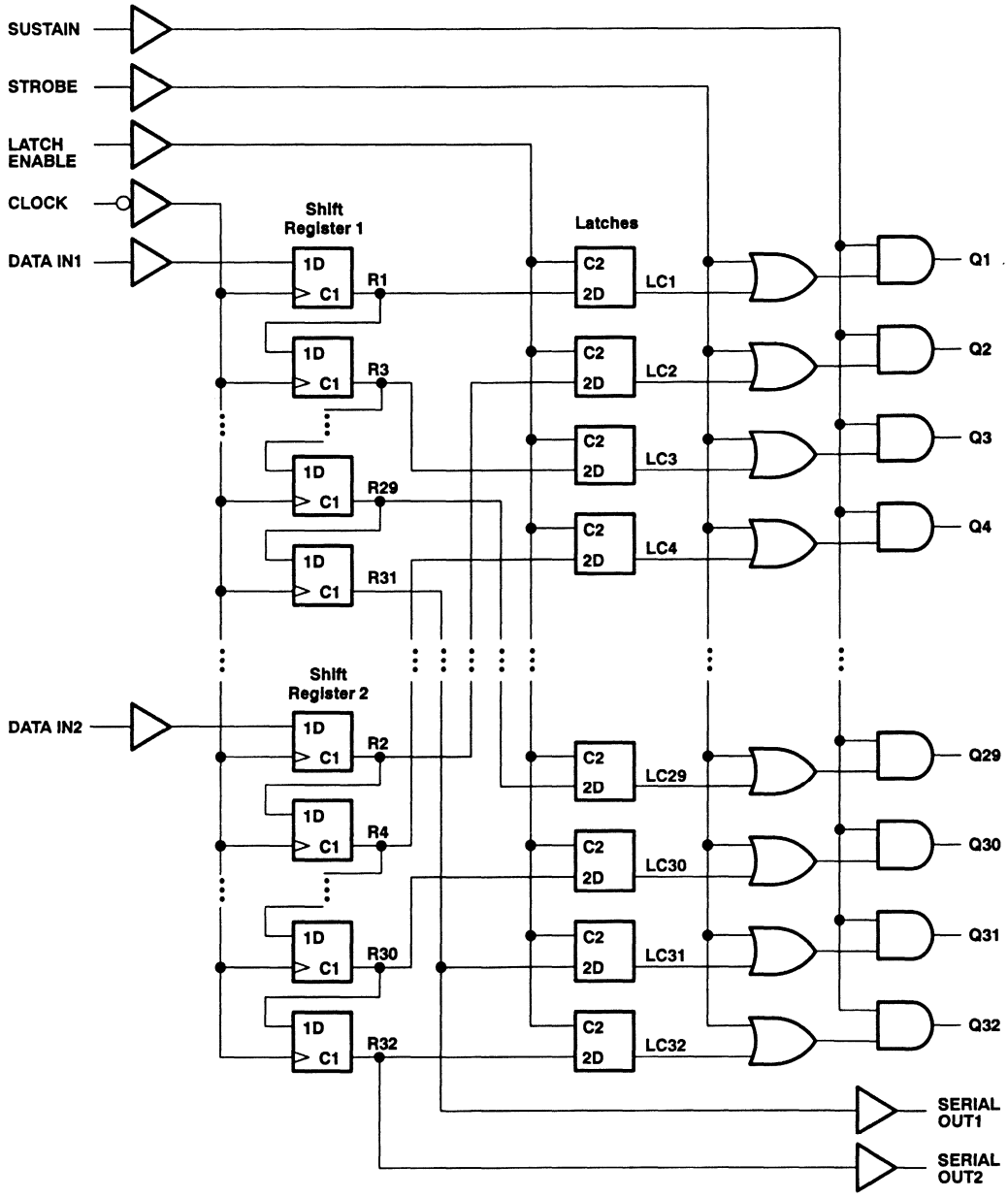
NC – No internal connection

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



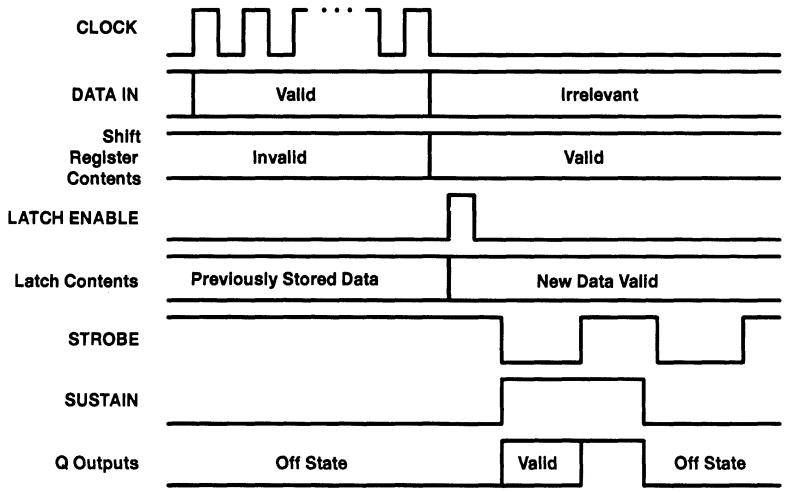
FUNCTION	CONTROL INPUTS				SHIFT REGISTERS R1 THRU R32	LATCHES LC1 THRU LC32	OUTPUTS		
	CLOCK	LATCH ENABLE	STROBE	SUSTAIN			SERIAL		Q1 THRU Q32
							S01	S02	
Load	↓ No ↓	X X	X X	X X	Load and shift† No change	Determined by LATCH ENABLE‡	R31	R32	Determined by SUSTAIN and STROBE
Latch Enable	X X	L H	X X	X X	As determined above	Stored data New data	R31	R32	Determined by SUSTAIN and STROBE
Strobe	X X	X X	L H	H H	As determined above	Determined by LATCH ENABLE‡	R31	R32	LC1 thru LC32 All on (high)
Sustain	X	X	X	L	As determined above	Determined by LATCH ENABLE‡	R31	R32	All off

H = high level, L = low level, X = irrelevant, ↓ = high-to-low transition

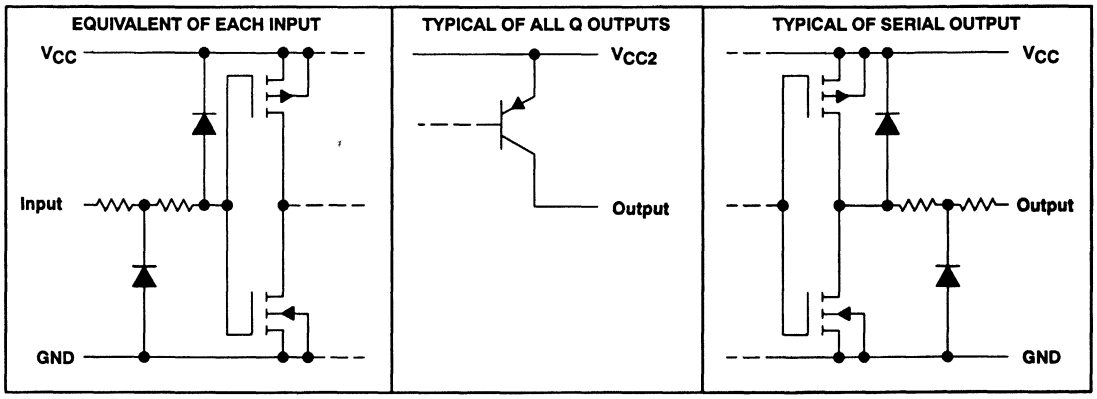
† Each even-numbered shift register stage takes on the state of the next-lower even-numbered stage, and likewise each odd-numbered shift register stage takes on the state of the next-lower odd-numbered stage; i.e., R32 takes on the state of R30, R30 takes on the state of R28, ... R4 takes on the state of R2, R2 takes on the state of DATA IN2, R31 takes on the state of R29, R29 takes on the state of R27, ... R3 takes on the state of R1, and R1 takes on the state on DATA IN1.

‡ New data enters the latches while LATCH ENABLE is high. This data is stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.4 to 7 V
On-state Q output voltage range, V_O ..... −120 V to V_{CC} + 0.4 V
Input voltage range, V_I ..... −0.4 V to V_{CC} + 0.4 V
Serial output voltage range ..... −0.4 V to V_{CC} + 0.4 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) ..... 1025 mW
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTES: 1. Voltages values are with respect to GND.
2. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Output voltage, V_O				−75	V
High-level input voltage, V_{IH}	V_{CC} = 4.5 V	3.6			V
	V_{CC} = 5.5 V	4.4			
Low-level input voltage, V_{IL}	V_{CC} = 4.5 V			0.9	V
	V_{CC} = 5.5 V			1	
Output current, I_O (T_A = 25°C)				−1.2	mA
Clock frequency, f_{clock}				5	MHz
Pulse duration, t_w (see Figure 1)	CLOCK	75			ns
	DATA IN	160			
	LATCH ENABLE	90			
	STROBE	2			µs
	SUSTAIN	2			
Setup time, t_{su} (see Figure 1)	DATA IN before CLOCK↓	20			ns
	CLOCK low before LATCH ENABLE↑	50			
	LATCH ENABLE low before CLOCK↓	0			
	LATCH ENABLE high before STROBE↓	0			
	LATCH ENABLE high before SUSTAIN↑	0			
Hold time, DATA IN after CLOCK↓, t_h (see Figure 1)		50			µs
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over operating free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −0.5 mA		4	4.5		V
		SERIAL OUT 1, 2	V_{CC} = 5.5 V	I_{OH} = −100 µA	4.3	4.6		
				I_{OH} = −20 µA	4.4			
			V_{CC} = 4.5 V	I_{OH} = −100 µA	3.4	3.6		
				I_{OH} = −20 µA	3.6			
V_{OL}	Low-level output voltage	SERIAL OUT 1, 2	V_{CC} = 5.5 V	I_{OL} = 100 µA		0.9	1.2	V
				I_{OL} = 20 µA			1.1	
			V_{CC} = 4.5 V	I_{OL} = 100 µA		0.9	1.1	
				I_{OL} = 20 µA			0.9	
I_{OH}	High-level Q output current		T_A= 25°C,	V_O = 3 V	−1.2			mA
I_{OL}	Low-level Q output current		T_A= 25°C,	V_O = −75 V			−500	µA
I_{IH}	High-level input current		T_A= 25°C,	V_I = V_{CC}			1	µA
I_{IL}	Low-level input current		T_A= 25°C,	V_I = 0			−1	µA
I_{CC}	Supply current		All Q outputs high,	V_{CC} = 5.5 V		17	25	mA
			All Q outputs low				3	
C_i	Input capacitance						15	pF

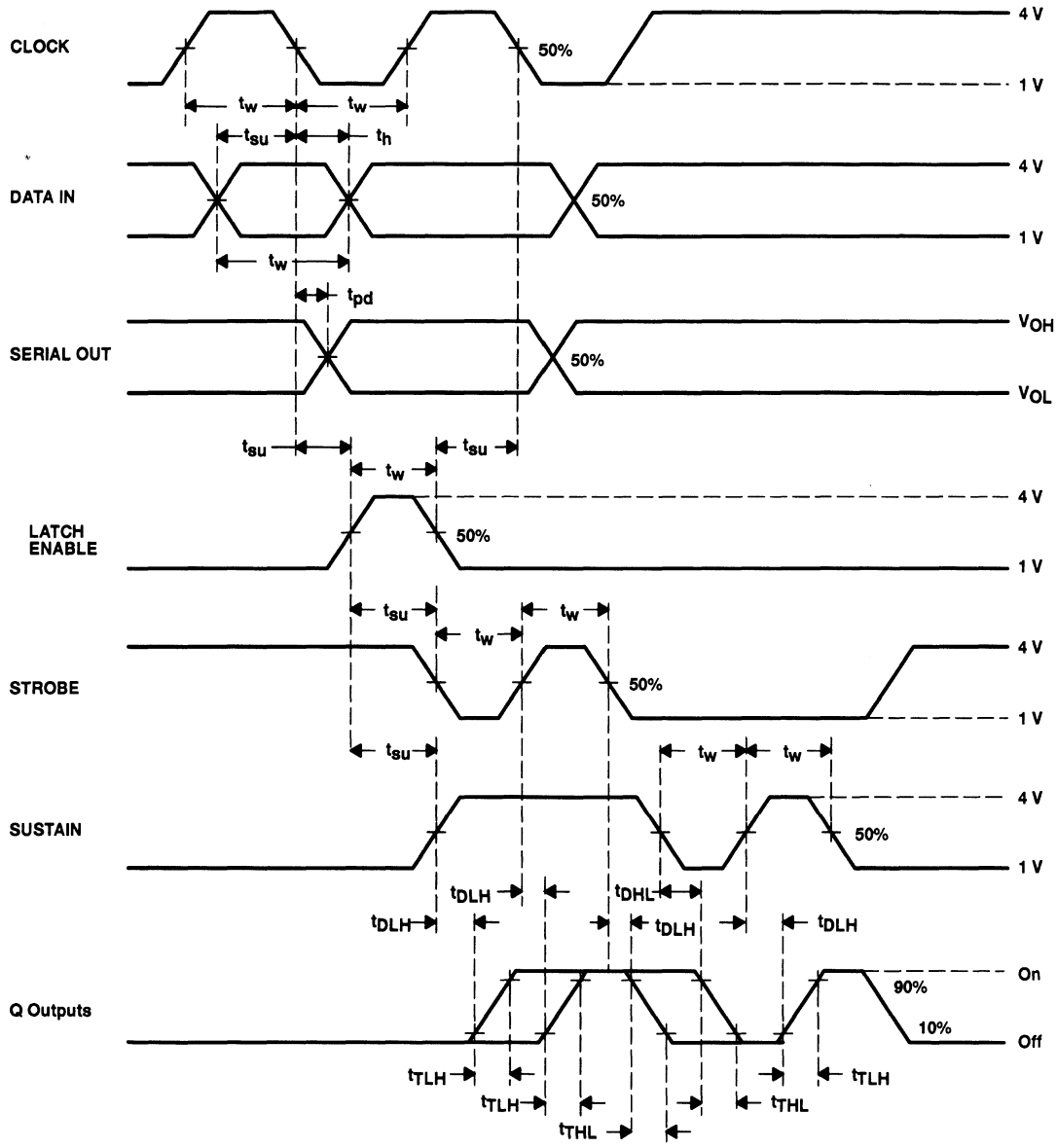
† All typical values are at T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, CLOCK to SERIAL OUT			100	150	ns
t_{DLH}	Delay time, low-to-high-level Q output from SUSTAIN or STROBE	R_L = 91 kΩ, See Figures 1 and 2		0.3‡	1	µs
t_{DHL}	Delay time, high-to-low-level Q output from SUSTAIN or STROBE			1‡	2.5	µs
t_{TLH}	Transition time, low-to-high-level Q output			2	5	µs
t_{THL}	Transition time, high-to-low-level Q output			11	18	µs

‡ Typical values for delay times are measured from SUSTAIN.

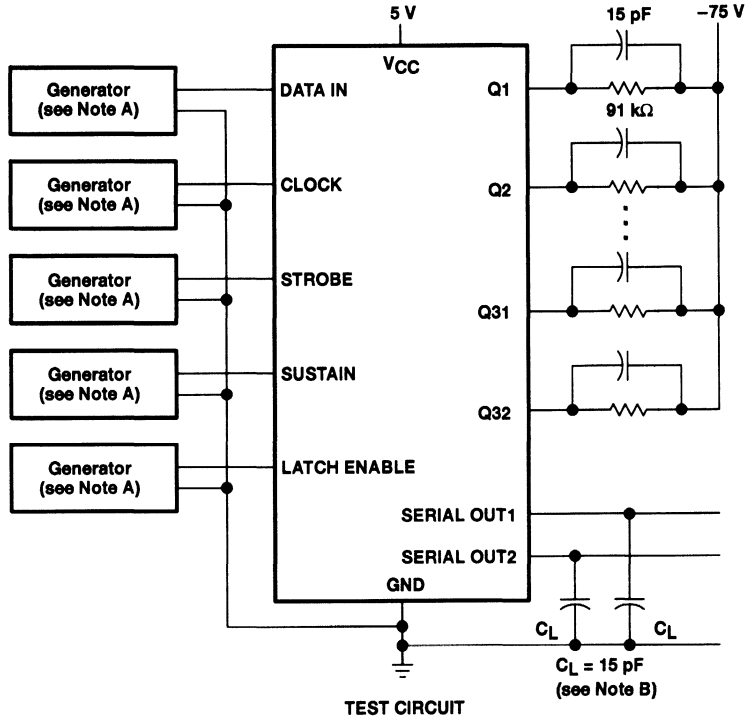
PARAMETER MEASUREMENT INFORMATION



NOTE: Input t_r and t_f are less than or equal to 10 ns.

Figure 1. Input Timing and Switching Time Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTES: A. Input pulses are supplied by generators having the following characteristics: t_w = 100 ns, PRR ≤ 5 MHz, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

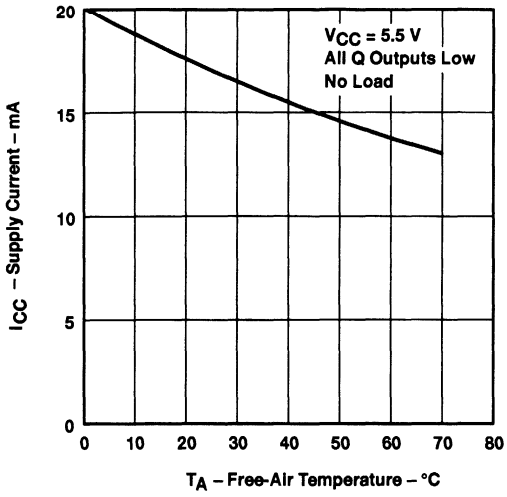


Figure 3

PROPAGATION DELAY TIME,
CLOCK TO SERIAL OUT
vs
FREE-AIR TEMPERATURE

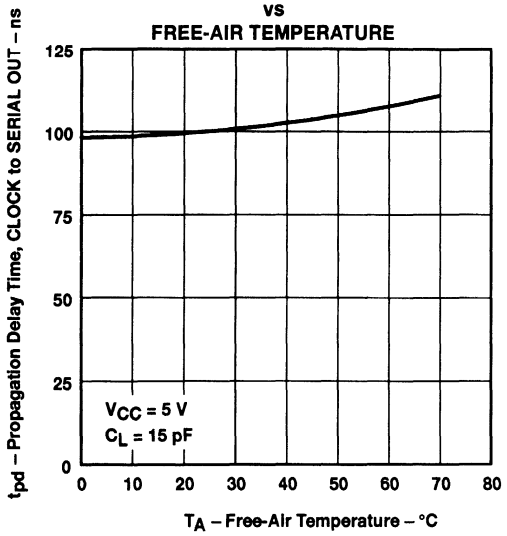


Figure 4

DELAY TIME, SUSTAIN INPUT TO Q OUTPUT
LOW TO HIGH
vs
FREE-AIR TEMPERATURE

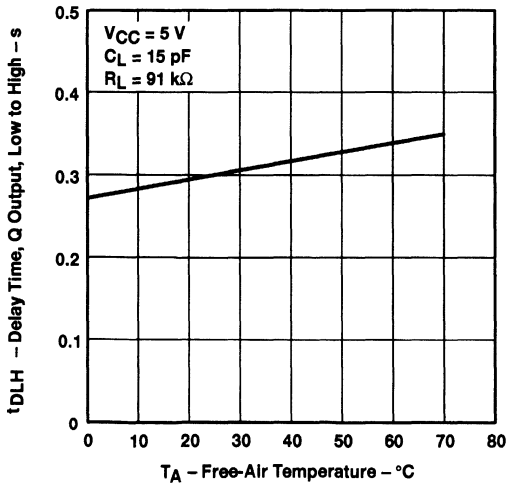


Figure 5

DELAY TIME, SUSTAIN INPUT TO Q OUTPUT
HIGH TO LOW
vs
FREE-AIR TEMPERATURE

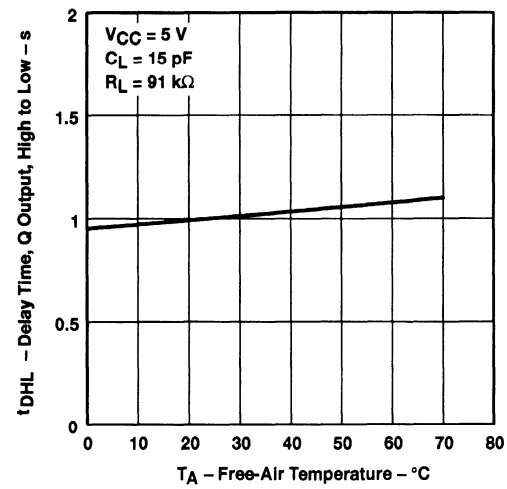


Figure 6

TYPICAL CHARACTERISTICS

TRANSITION TIME, Q OUTPUT,
LOW TO HIGH
vs
FREE-AIR TEMPERATURE

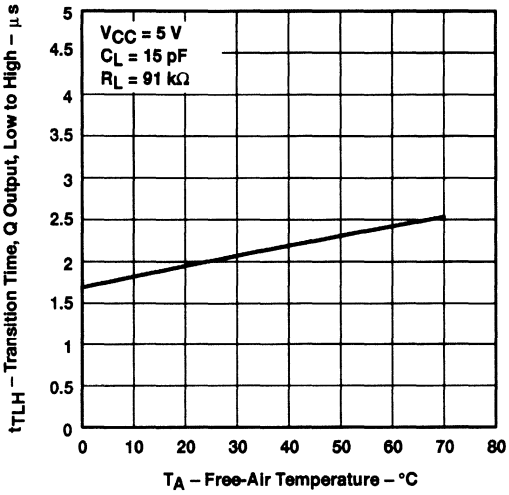


Figure 7

TRANSITION TIME, Q OUTPUT,
HIGH TO LOW
vs
FREE-AIR TEMPERATURE

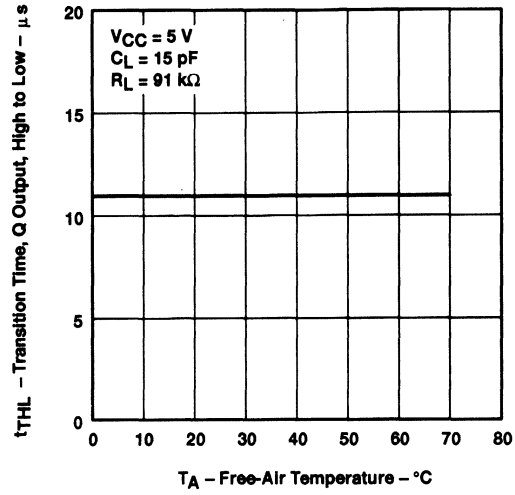


Figure 8

SLDS006C – D2715, DECEMBER 1984 – REVISED MAY 1993

- **Each Device Drives Ten Lines**
- **60-V Output Voltage Rating**
- **40-mA Output Source Current**
- **High-Speed Serially-Shifted Data Input**
- **CMOS-Compatible Inputs**
- **Latches on All Driver Outputs**
- **Improved Direct Replacement for UCN4810A and TL4810A**

description

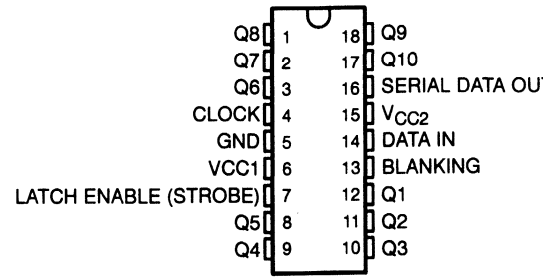
The TL4810B and TL4810BI are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). These devices feature a serial data output to cascade additional devices for large display arrays.

A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while LATCH ENABLE is high and is latched when LATCH ENABLE is low. When BLANKING is high, all outputs are low.

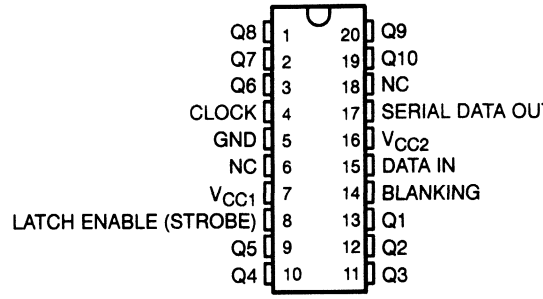
Outputs are totem-pole structures formed by npn emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 V and 40-mA source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pullup resistor to V_{CC1} when driven by TTL logic.

The TL4810B is characterized for operation from 0°C to 70°C. The TL4810BI is characterized for operation from –40°C to 85°C.

N PACKAGE
(TOP VIEW)



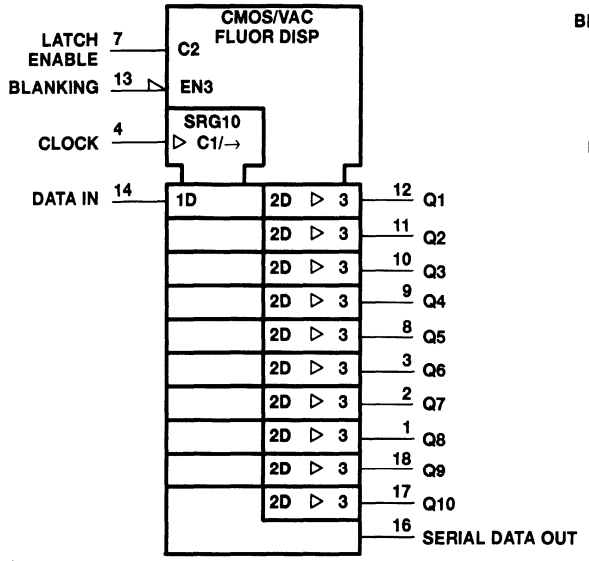
DW PACKAGE
(TOP VIEW)



NC – No internal connection

† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

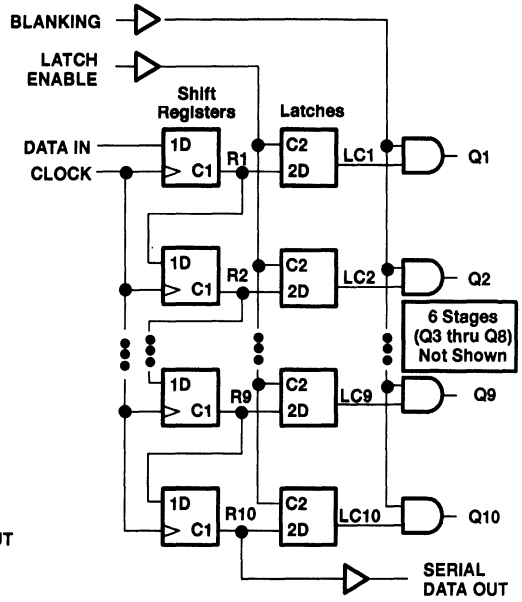
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the N package.

logic diagram (positive logic)



FUNCTION TABLE

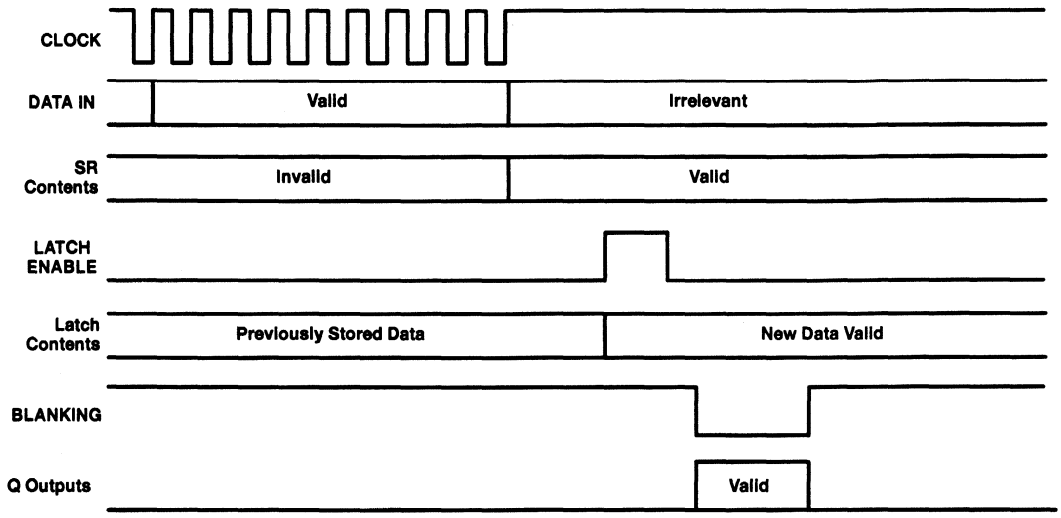
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R10‡	LATCHES LC1 THRU LC10	SERIAL	OUTPUTS Q1 THRU Q10
	CLOCK	LATCH ENABLE	BLANKING				
Load	↑	X	X	Load and shift‡	Determined by LATCH ENABLE§	R10	Determined by BLANKING
	No↑	X	X	No change			
Latch	X	L	X	As determined above	Stored data	R10	Determined by BLANKING
	X	H	X		New data		
Blank	X	X	H	As determined above	Determined by LATCH ENABLE§	R10	All L
	X	X	L				LC1 thru LC10, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.

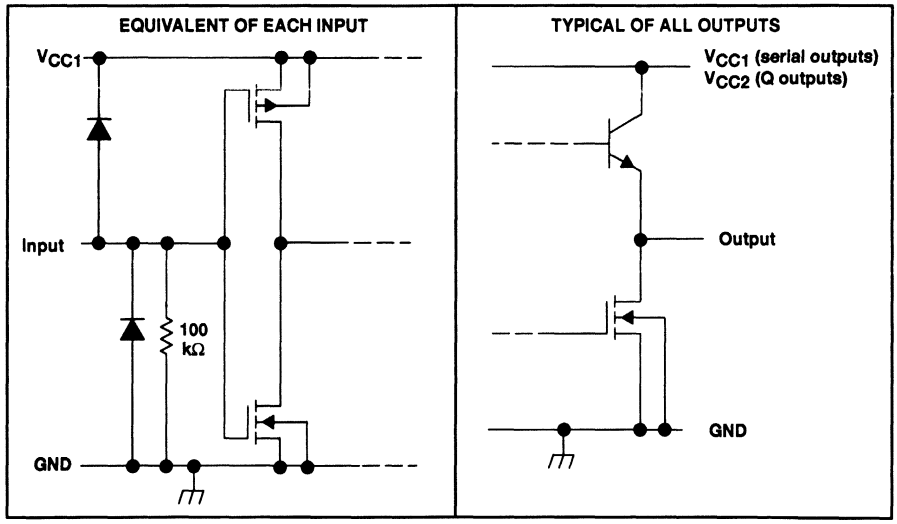
‡ Register R10 takes on the state of R9, R9 takes on the state of R8...R2 takes on the state of R1, and R1 takes on the state of the data input.

§ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1} (see Note 1) ..... 18 V
Driver supply voltage, V_{CC2} ..... 70 V
Output voltage, V_O ..... 70 V
Input voltage range, V_I ..... −0.3 V to V_{CC1} + 0.3 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TL4810B ..... 0°C to 70°C
TL4810BI ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

NOTE 1: Voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	585 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

PARAMETER		TL4810B			TL4810BI			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC1}		4.75		15.75	4.75		15.75	V
Supply voltage, V_{CC2}		5		60	5		60	V
High-level input voltage, V_{IH}	V_{CC1} = 5 V	3.5		5.3	3.5		5.3	V
	V_{CC1} = 15 V	13.5		15.3	13.5		15.3	
Low-level input voltage, V_{IL}		−0.3†		0.8	−0.3†		0.8	V
Continuous high-level output current, I_{OH}				−25			−25	mA
Operating free-air temperature, T_A		0		70	−40		85	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltages only.

electrical characteristics over recommended operating free-air temperature range, V_{CC1} = 5 V to 15 V, V_{CC2} = 60 V, GND = 0 (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TL4810B			TL4810BI			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	Q outputs	I_{OH} = −25 mA		57.5	58		57.5	58		V
		SERIAL DATA OUT	V_{CC1} = 5 V,	I_{OH} = −100 µA	4	4.5		4	4.5		
			V_{CC1} = 15 V,	I_{OH} = −100 µA	14	14.7		14	14.7		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 µA,	BLANKING at V_{CC1}		0.5	1		0.5	1	V
		SERIAL DATA OUT	V_{CC1} = 5 V,	I_{OL} = 100 µA		0.05	0.1		0.05	0.1	
			V_{CC1} = 15 V,	I_{OL} = 100 µA		0.02	0.1		0.02	0.1	
I_{OL}	Low-level Q output current (pulldown current)		V_O = 60 V, T_A = MIN to 70°C	BLANKING at V_{CC1},	2.5	3.7		2.5	3.7		mA
			V_O = 60 V, T_A = 85°C	BLANKING at V_{CC1},				2			
$I_{O(off)}$	Off-state output current		V_O = 0, T_A = MAX	BLANKING at V_{CC1},		−1	−15		−1	−15	µA
I_H	High-level input current		V_I = V_{CC1}			30	50		30	50	µA
I_{CC1}	Supply current from V_{CC1}		All inputs at 0 V, One Q output high	V_{CC1} = 5 V		10	50		10	50	µA
				V_{CC1} = 15 V		10	100		10	100	
			All inputs at 0 V, All outputs low	V_{CC1} = 5 V		10	50		10	50	
				V_{CC1} = 15 V		10	100		10	100	
I_{CC2}	Supply current from V_{CC2}		All outputs low			0.5	1		0.5	1	mA
			All outputs high, T_A = 0°C to MAX			2.7	4		2.7	4	
			All outputs high, T_A = −40°C							5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C, except for I_O.

timing requirements over recommended operating free-air temperature range

		V_{CC1} = 5 V		V_{CC1} = 15 V		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(CKH)}$	Pulse duration, CLOCK high	250		50		ns
$t_{w(LEH)}$	Pulse duration, LATCH ENABLE high	250		50		ns
$t_{su(D)}$	Setup time, DATA IN before CLOCK↑	125		25		ns
$t_{h(D)}$	Hold time, DATA IN after CLOCK↑	125		25		ns
$t_{d(CKH-LEH)}$	Delay time, CLOCK↑ to LATCH ENABLE high	125		25		ns

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, LATCH ENABLE to Q outputs	V_{CC1} = 5 V		1		µs
		V_{CC1} = 15 V		0.5		

PARAMETER MEASUREMENT INFORMATION

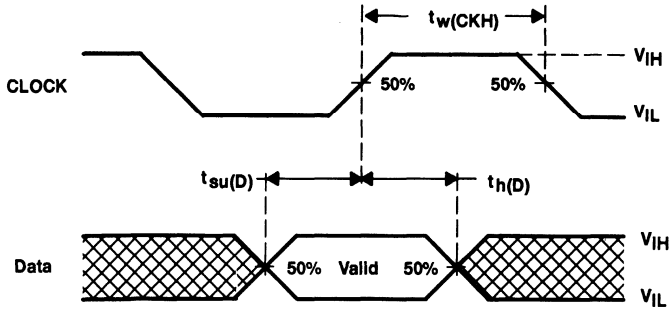


Figure 1. Input Timing

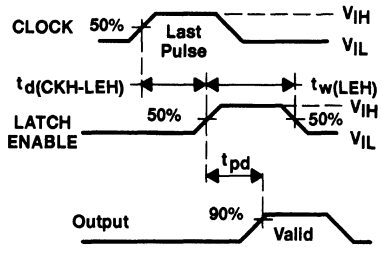


Figure 2. Output Switching Times

THERMAL INFORMATION

DW PACKAGE DUTY CYCLE
vs
FREE-AIR TEMPERATURE

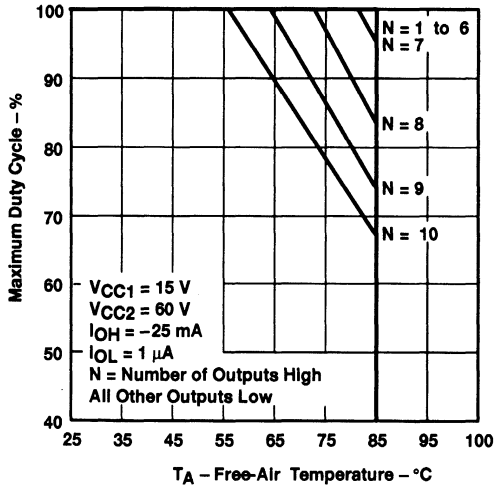


Figure 3

N PACKAGE DUTY CYCLE
vs
FREE-AIR TEMPERATURE

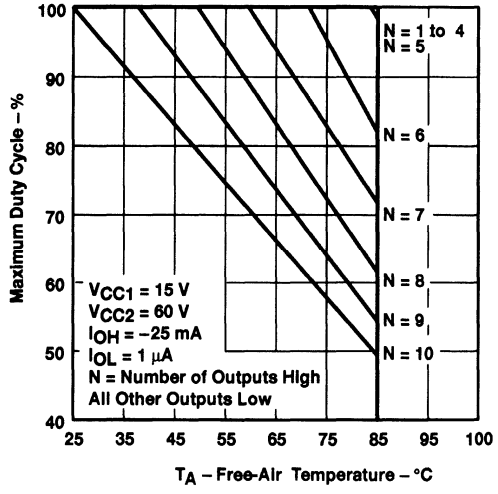


Figure 4

SLDS011B – D2914, OCTOBER 1985 – REVISED MAY 1993

- **Drives up to 20 Lines**
- **70-V Output Voltage Swing Capability**
- **40-mA Output Source Current Capability**
- **High-Speed Serially-Shifted Data Input**
- **CMOS-Compatible Inputs**
- **Direct Replacement for Sprague UCN5812A**

description

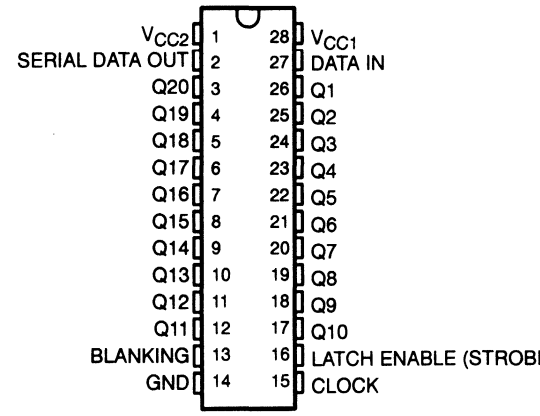
The TL5812 and TL5812I are monolithic BIDFET† integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). Each device features a serial data output to cascade additional devices for large display arrays.

A 20-bit data word is serially loaded into the shift register on the low-to-high transition of CLOCK. Parallel data is transferred to the output buffers through a 20-bit D-type latch while LATCH ENABLE is high and is latched when LATCH ENABLE is low. When BLANKING is high, all outputs are low.

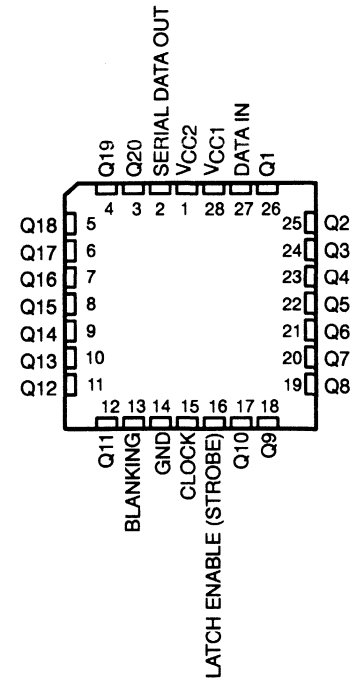
The outputs are totem-pole structures formed by npn emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 70 V and a source-current capability of 40 mA. All inputs are CMOS compatible.

The TL5812 is characterized for operation from 0°C to 70°C. The TL5812I is characterized for operation from –40°C to 85°C.

N PACKAGE
(TOP VIEW)

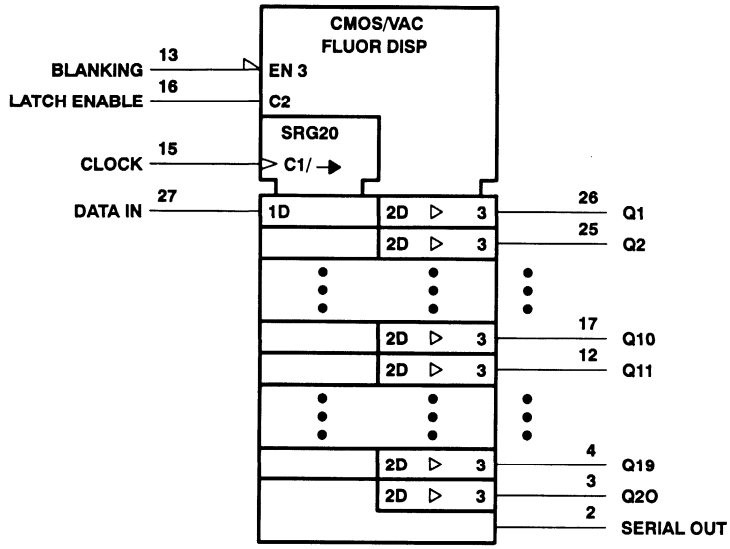


FN PACKAGE
(TOP VIEW)



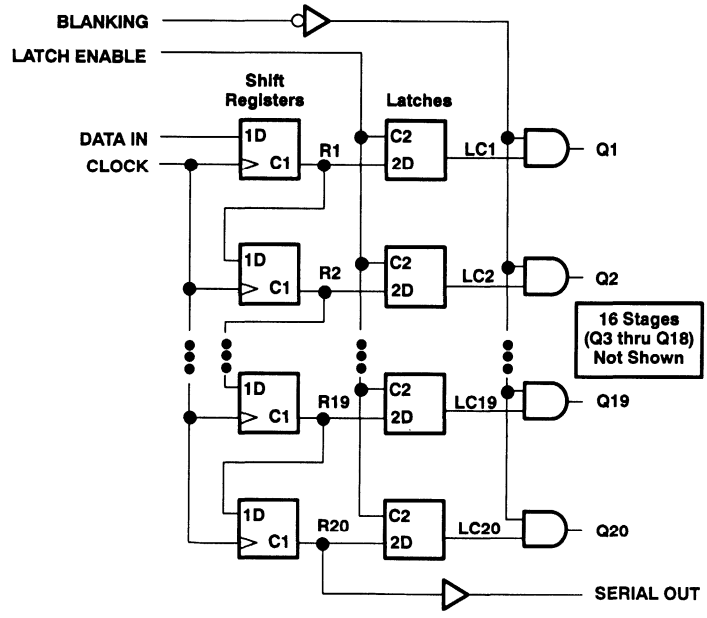
† BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

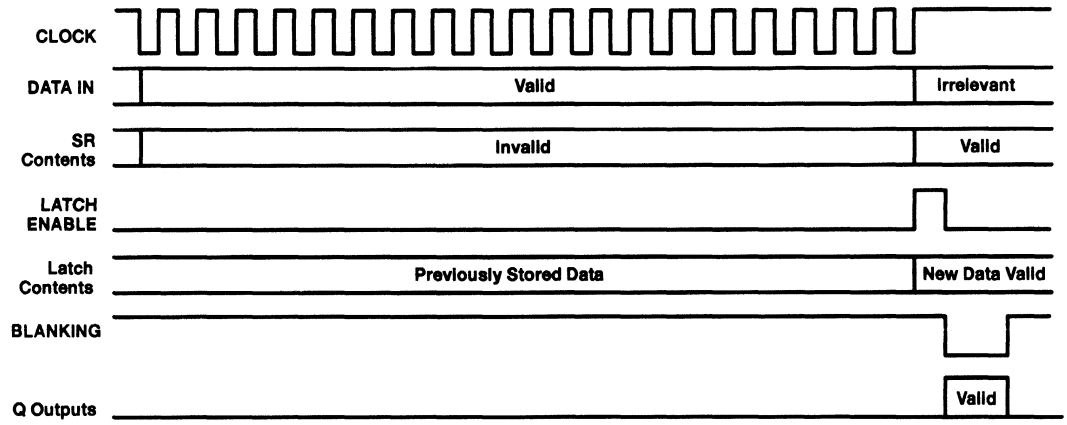


FUNCTION TABLE

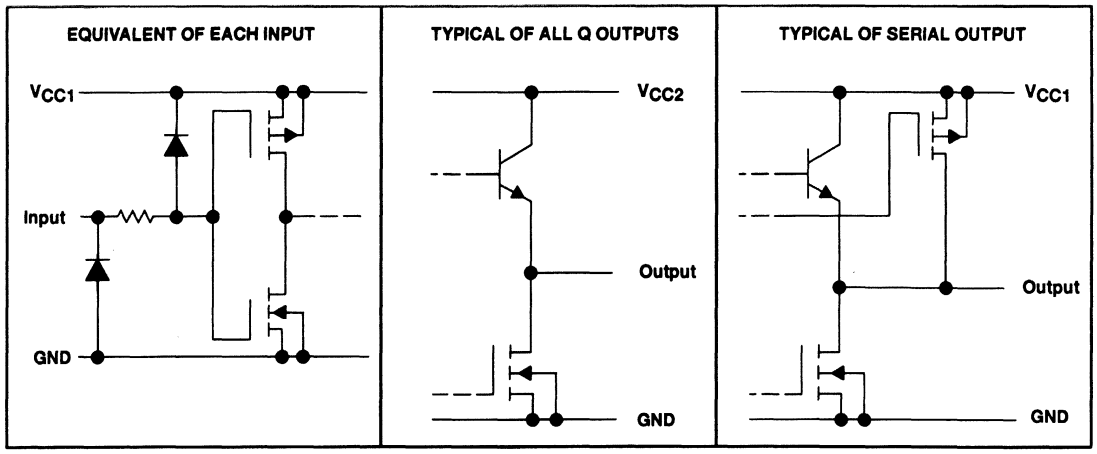
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R20	LATCHES LC1 THRU LC20	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANKING			SERIAL	Q1 THRU Q20
Load	↑	X	X	Load and shift†	Determined by LATCH ENABLE‡	R20	Determined by BLANKING
	No↑	X	X	No change		R20	
Latch	X	L	X	As determined above	Stored data	R20	Determined by BLANKING
	X	H	X		New data	R20	
Blank	X	X	H	As determined above	Determined by LATCH ENABLE‡	R20	All L
	X	X	L			R20	LC1 thru LC10, respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
† R20 takes on the state of R19, R19 takes on the state of R18, ... R2 takes on the state of R1, and R1 takes on the state of the data input.
‡ New data enter the latches while LATCH ENABLE is high. These data are stored while LATCH ENABLE is low.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) ..... 15 V
Supply voltage, V_{CC2} ..... 70 V
Output voltage, V_O ..... 70 V
Input voltage range, V_I ..... −0.3 V to V_{CC1} +0.3 V
Output current, I_O ..... −40 mA
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range: TL5812 ..... 0°C to 70°C
TL5812I ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
FN	1400 mW	11.2 mW/°C	896 mW	728 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		4.5		15	V
Supply voltage, V_{CC2}		0		60	V
High-level input voltage, V_{IH}		$V_{CC1}-1.5$		$V_{CC1}+0.3$	V
Low-level input voltage, V_{IL}		−0.3†		0.8	V
High-level output current, I_{OH}				−40	mV
Operating free-air temperature, T_A	TL5812	0		70	°C
	TL5812I	−40		85	

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over operating free-air temperature range, V_{DD} = 5 V to 15 V, V_{BB} = 60 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output	Q outputs	I_{OH} = −25 mA		57.5	58.2		V
		SERIAL DATA OUT	V_{CC1} = 5 V,	I_{OH} = −20 µA	4.5	4.9		
			V_{CC1} = 15 V,	I_{OH} = −20 µA	14.5	14.9		
V_{OL}	Low-level output voltage	Q outputs	I_{OL} = 1 mA,	BLANKING at V_{CC1}		0.7	1.5	V
		SERIAL DATA OUT	V_{CC1} = 5 V,	I_{OL} = 20 µA		0.06	0.3	
			V_{CC1} = 15 V,	I_{OL} = 20 µA		0.03	0.3	
I_{IH}	High-level input current		$V_I = V_{CC1}$			0.3	1	µA
I_{IL}	Low-level input current		V_I = 0			−0.3	−1	µA
I_{OL}	Low-level output current (pulldown current)		V_O = 60 V,	BLANKING at V_{CC1}	2.5	3.2		µA
$I_{O(off)}$	Off-state output current		V_O = 0,	BLANKING at V_{CC1}		< −1	−15	µA
I_{CC2}	Supply current from V_{CC2}		Outputs high			3.5	8	mA
			Outputs low			0.02	0.5	
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 5 V			1.5	3	mA
			V_{CC1} = 15 V			1.7	4	

‡ All typical characteristics are at T_A = 25°C.

timing requirements over operating free-air temperature range

			MIN	MAX	UNIT
$t_{w(CKH)}$	Pulse duration, CLOCK high	V_{CC1} = 5 V	500		ns
		V_{CC1} = 15 V	100		
$t_{w(LEH)}$	Pulse duration, LATCH ENABLE high	V_{CC1} = 5 V	500		ns
		V_{CC1} = 15 V	100		
$t_{su(D)}$	Setup time, DATA IN before CLOCK↑	V_{CC1} = 5 V	150		ns
		V_{CC1} = 15 V	75		
$t_{h(D)}$	Hold time, DATA IN after CLOCK↑	V_{CC1} = 5 V	150		ns
		V_{CC1} = 15 V	75		
$t_{d(CKH-LEH)}$	Delay time, CLOCK↑ to LATCH ENABLE high	V_{CC1} = 5 V	150		ns
		V_{CC1} = 15 V	75		

switching characteristics, V_{BB} = 60 V, T_A = 25°C

PARAMETER			MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, LATCH ENABLE to Q outputs	V_{CC1} = 5 V		2.2		μs
		V_{CC1} = 15 V		0.8		

PARAMETER MEASUREMENT INFORMATION

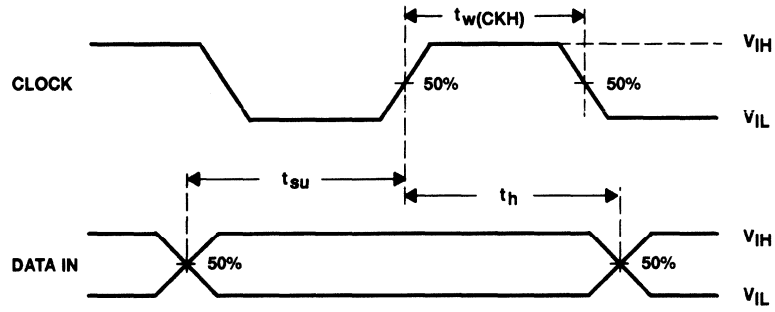


Figure 1. Input Timing

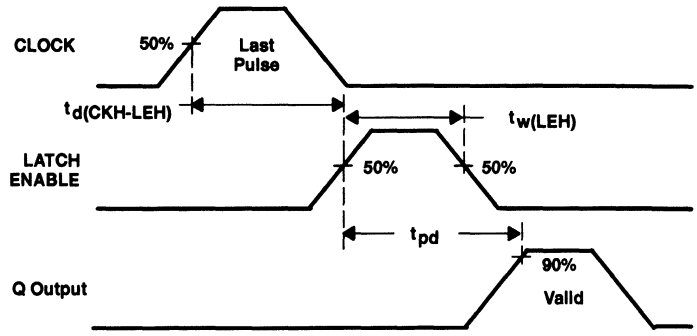


Figure 2. Output Switching Times

THERMAL INFORMATION

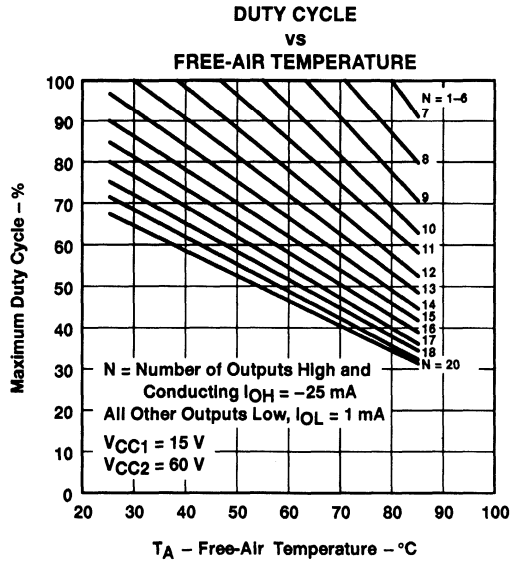


Figure 3

Contents

Power Systems

Table of Contents

5.1 Introduction

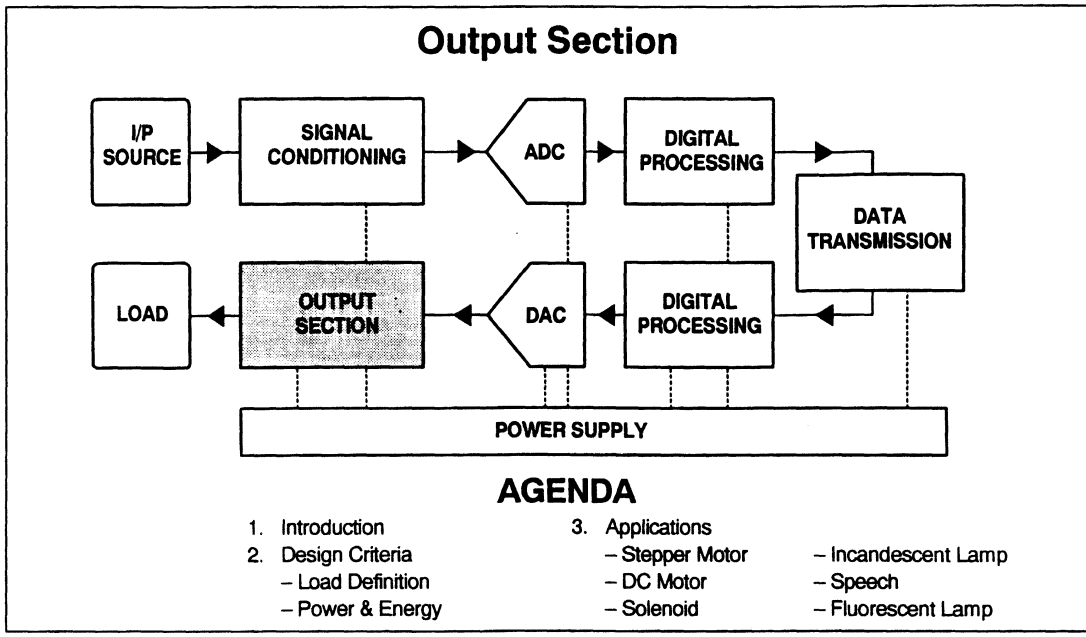


Figure 5.1.1 - Output Section

The output section of a control system serves as the interface between electrical control signals and the "real world". The end product of the output section is the control of a "real world" function such as motion, light, sound or any number of other physical actions. Control systems vary greatly in their complexity from controlling a simple single action to complex interactive systems with multiple feedback signals, fault isolation and adaptive software. Regardless of the system complexity, an output system is normally employed to complete the interface between control system and the "real world" .

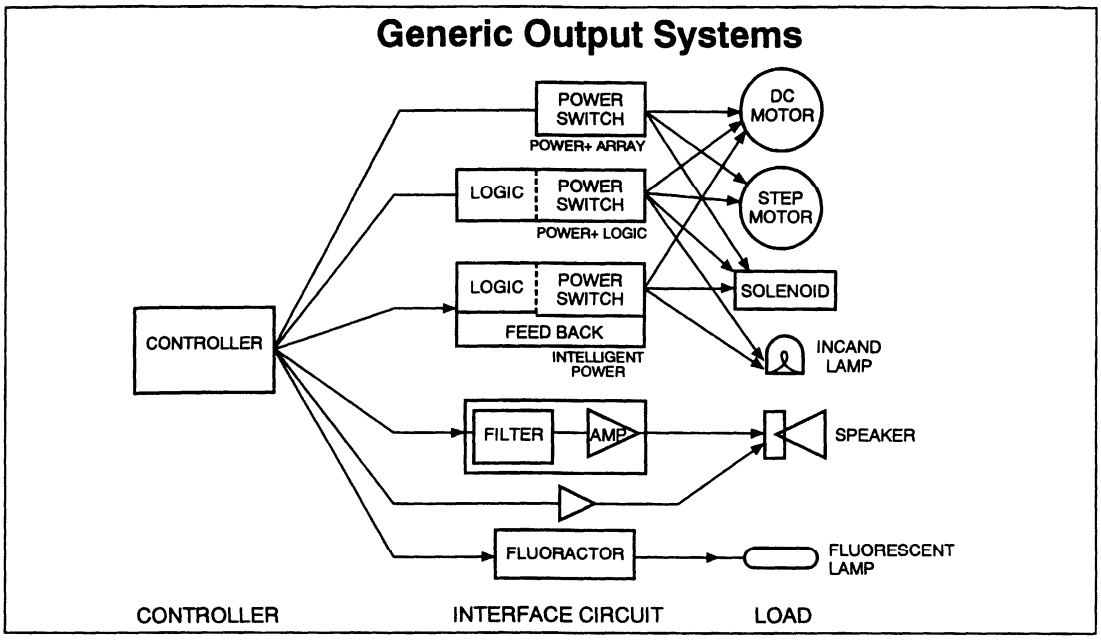


Figure 5.1.2 - Generic Output Systems

Figure 5.1.2 represents a generalized output system consisting of a controller, an interface circuit and a load. The design problem we are addressing is controlling the operation of a load with a small signal. Several typical loads such as motors, solenoids, speakers and lamps are shown. Notice that for most of the loads several signal paths exist from the controller through the interface circuits. Each path represents a solution to one specific design problem. Although multiple solutions exist they may not all be the best solution. The next section will discuss the methodology for designing an output system that is well suited for a particular application.

5.2 Output System Design

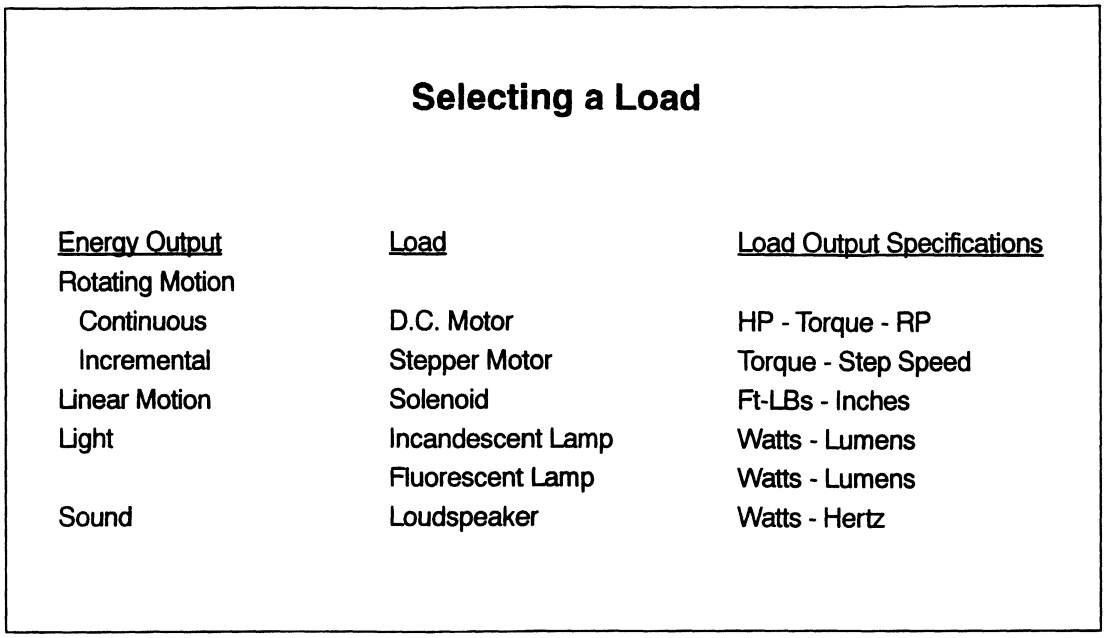


Figure 5.2.1 - Selecting a Load

Selecting a load device

The first step is selecting a load. Selecting the load involves defining the type of output energy needed, selecting the proper class of load, and selecting the correct size load. Figure 5.2.1 depicts some energy types with the corresponding load and output parameters. A DC motor, for example, will usually have an output specification that is in terms of torque at a given speed. Matching the mechanical requirements for a particular application is outside the scope of this discussion. We will assume that a suitable load can be selected.

The second step is evaluation of the input requirements for a particular load. Load input specifications address the voltage and current requirements during normal operation. Normal operation includes load switching (turn on, turn off and accompanying transients). Often the behavior of a load during switching is not adequately specified and must be characterized for the specific application. Understanding load input requirements will lead to the interface circuit requirements.

Interface Circuit Requirements

If we assume that the interface circuit is a switch then what do we need to know in order to select the right switch?

Motors, solenoids, lamps and other assorted loads are generally specified by operating voltage and current with a specified power output. The information provided is sufficient for operating at continuous duty cycle, however, in most applications the load is being switched on and off. When switching loads, the operating requirements as well as transient conditions must be considered. The power requirements are often further influenced by dynamic

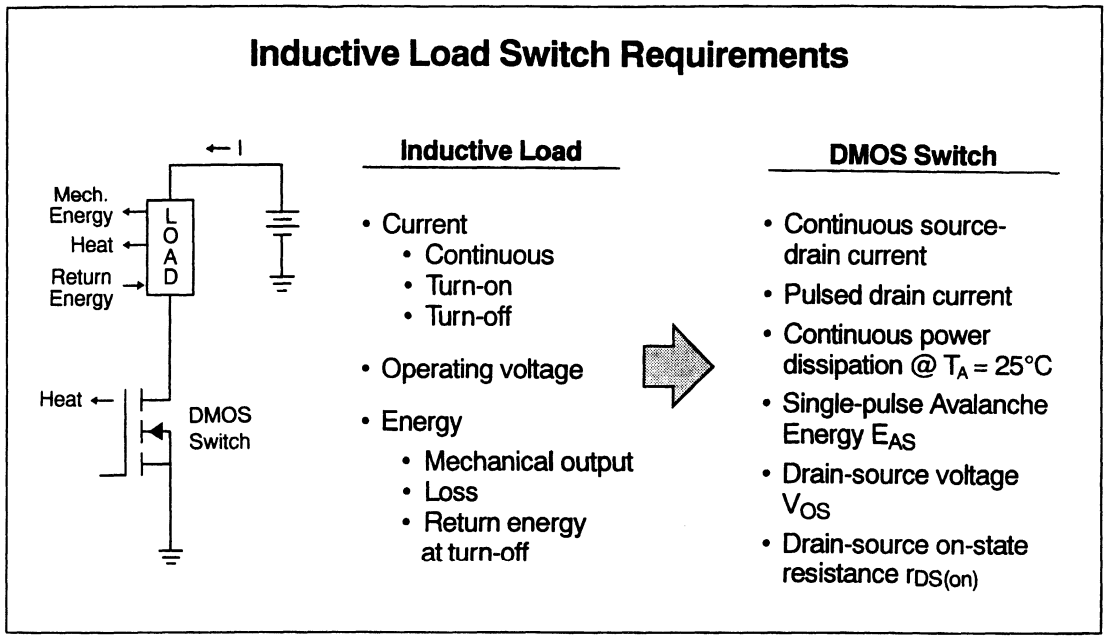


Figure 5.2.2 - Inductive Load Switch Requirements

The easiest way to look at load requirements is to consider the example in Figure 5.2.2, of a load operating from a battery and controlled by a low side switch. What is needed to design the switch and evaluate the system?

The system power supply and load choice will determine:

- Current drawn from the battery, including transients when the switch is turned on and off.
- Battery terminal voltage. (V)
- Energy output from the load (motion, sound, etc.)
- Energy dissipated from the load in the form of heat. (IR loss, magnetic loss, friction)
- Energy returned to system (inductive, regeneration, cross coupling)

These system load requirements must then be used to determine the switch requirements:

- Continuous source-drain current
- Pulsed drain current
- Continuous power dissipation @ T_A = 25 °C

- Drain-source voltage (V_{DS})
- Drain-source on-state resistance ($R_{DS(on)}$)

Selecting or designing a switch is a three step process; determine the total energy, current, and voltage required, select a switching device which will accommodate the energy, and evaluate the system power dissipation to determine any heat sinking requirements.

Determine Total Energy

Determining the total energy begins with evaluating load current during operation and switching.

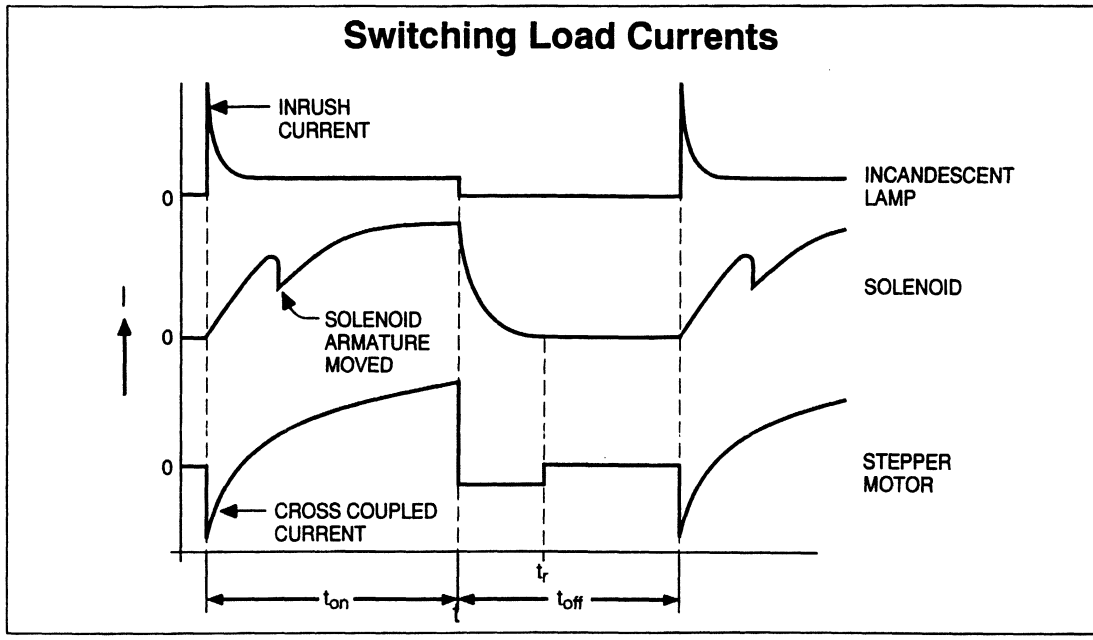


Figure 5.2.3 -Switching Load Currents

Figure 5.2.3 shows the current wave forms for an incandescent lamp, a solenoid and a stepper motor. This diagram depicts steady state and switching conditions which must be considered in controlling a load.

The incandescent lamp current shows a high inrush value at turn on (t_{on}), decreasing to a steady current value. Current remains at this value until turn off (t_{off}). Upon t_{off} the current drops to zero. The high inrush is due to the difference in filament resistance when cold and hot. A lamp control switch will need to withstand high peak currents or limit the current until the lamp filament warms up.

The solenoid current increases starting at t_{on}, and continues to increase until t_{off}. Upon t_{off}, the current steadily drops until t_R. The change in current slope between t_{on} and t_{off} is caused by the solenoid armature moving closer to the coil and increasing the coil inductance. The current flow between t_{off} and t_R is a result of the magnetic field in the solenoid collapsing

operating current and the system must provide a method for accommodating the energy returned to the system at turn off. Several methods are employed to deal with the returned energy. When this energy is dissipated in the switch, it is referred to as avalanche energy.

The stepper motor exhibits an exponential current increase characteristic of an inductive load. Return energy is a factor in stepper motor control. Additionally, stepper motor windings can produce currents as a result of cross coupling from adjacent motor windings. A control circuit for a stepper motor such as depicted in Figure 5.2.3 must accommodate the transient energy at turn on and the returned energy at turn off.

Once the load characteristics are determined energy calculations can proceed.

Energy and Power Calculations for an Inductive Load

- Power-on time MOSFET dissipation

$$P_{on} = \frac{1}{3} (I_p^2)\, r_{DS(on)}\, d \qquad \text{For } \frac{L}{R_L} > t_{on}$$

- Back e.m.f. energy

$$E_T = \frac{3\, L\, I_p^2 V_{CL}}{6\,(V_{CL} - V_{SS}) + 4 R_L I_P}$$

- Power off dissipation

$$P_{off} = E_T f$$

- Total average switch power dissipation

$$P_T = (P_{on} + P_{off})n + P_{(quies)}$$

L = Load Inductance
I_p = Peak Drain Current
V_{CL} = Max Output Clamp Voltage
V_{SS} = Load Supply Voltage
R_L = Inductor Resistance
f = Switching Frequency
d = Duty Cycle (Ratio)
$r_{DS(on)}$ = Drain to Source on Resistance
n = Total Number of Switches Operating
$P_{(quies)}$ = Quiescent Power Dissipation of Switch Circuit
t_{on} = Switch On Time

Figure 5.2.4 - Energy and Power Calculations for Inductive Loads

The energy calculations for an inductive load are presented in Figure 5.2.4. The intent is to calculate the total power dissipated in the transistor switch.

Power dissipated during switch "on" time is calculated as follows:

During the power-on time the inductor's current approximates to a linear ramp, assuming the inductors L/R_L time constant is greater than the turn on time (t_{on}). This results in a mean square drain current of 1/3 I_P^2 with I_P equal to the peak drain current. Therefore the average power dissipated in the output MOSFET, P_{on}, is equal to:

$$P_{on(av)} = 1/3\, (I_P^2)^* r_{DS(on)} * d$$

This assumption would be applicable to the stepper motor wave form in figure 5.2.3, but would not work for the solenoid. The solenoid time constant L/RL is less than t_{on}, therefore P_{on} will be greater than that calculated above.

Power dissipated during switch off time is calculated as follows:

When the output MOSFET is turned off, the back e.m.f. generated by the inductor raises the drain voltage, which must be clamped either externally or internally. External clamping is normally accomplished with a snubber diode. Internal clamping is also accomplished with a zener diode. The clamp voltage V_{CL} is also called avalanche voltage.

The equation to define avalanche energy is:

$$E_T = (3 * L_H * I_P^2 * V_{CL})/(6 * (V_{CL} - V_{SS}) + 4 * R_L * I_P) \quad \text{.... JEDEC Standard No. 10;}$$

This equation assumes a linear decay of the current in the inductor. A more accurate E_T calculation can be accomplished by integrating the inductor current and clamp voltage in the load. The integration is taken from turn off (t_1) until the inductor current decays to zero. The calculation is as follows:

$$E_T = \int_0^{t_1} V_{CL} * I_L * dt ;$$

$$I_L = (I_P + (V_{CL} - V_{SS})/R_L)\ e^{-(RL/L)t} - (V_{CL} - V_{SS})/R_L ;$$

$$I_P = V_{SS}/R_L\ (1 - e^{-(RL/LH * d/f)}) ;$$

$$t_1 = L/R_L * \ln [\, 1 + (\, I_P * R_L/(V_{CL} - V_{SS}))]$$

$$E_T = V_{CL} * L_H/R_L * (\, I_P - (\, V_{CL} - V_{SS}\,)/R_L * \ln (\, 1 + (\, I_P * R_L\,)/(V_{CL} - V_{SS}\,)\,)$$

The power dissipated during the turn-off period, P_{off}, can be equated to the product of E_T and the frequency of switching

$$P_{off} = E_T * f$$

Hence the total power, P_T, dissipated in an integrated switch with multiple output sections is:

$$P_{T(av)} = (P_{off} + P_{on}) * n + P_{(quies)}$$

This is the average power dissipation for multiple sections whose duty cycles have a fixed time relationship to each other. For multiple outputs with variable duty cycles the power calculation becomes more difficult.

Where:

E_T = Total turn-off transient energy absorbed

f = Switching frequency

L = Load Inductance

I_P = Peak output load current

n = Number of output switches operating

P_{off} = Turn-off power dissipation in each switch

P_{on} = On-state power dissipation each switch

$P_{(quies)}$ = Interface device bias power dissipation

$P_{T(av.)}$ = Average total power dissipation

R_L = Resistance of inductor

V_{CL} = Clamp voltage

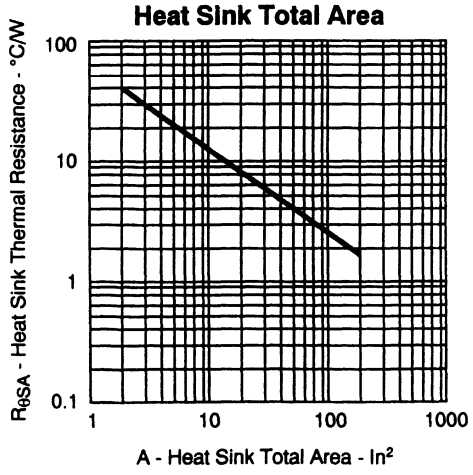
V_{SS} = Load supply voltage

Thermal Considerations

Now that the total power dissipation for the device has been calculated, a thermal evaluation can proceed. The objective is to determine if external heat sinking will be required.

Thermal Consideration for Power Switches

Typical Heat Sink Thermal Resistance vs. Heat Sink Total Area



Max Power Dissipation

$$P_{MAX} = (T_{J(MAX)} - T_A) / R_{\theta JA}$$

Thermal Resistance

$$R_{\theta SA} = \frac{T_J - T_A}{P_{T(AV)}} - \left| R_{\theta JC} + R_{\theta CS} \right|$$

Where:

$R_{\theta SA}$ = Heat sink-to-ambient thermal resistance, °C/W

$R_{\theta JC}$ = Device junction-to-case thermal resistance = 3.0°C/W

$R_{\theta CS}$ = Case-to-heat sink thermal resistance, °C/W = 0.5°C/W typical with thermal joint compound

$P_{T(AV)}$ = Total average power dissipation, W

T_J = Junction operating temperature, °C

T_A = Operating ambient temperature, °C-

Figure 5.2.5 -Thermal Considerations For Power Switches

The requirement for external heat sinking is calculated based on the device's total average power dissipation, maximum junction temperature, and ambient operating temperature. The maximum power which can be dissipated in a device (P_D) can be determined as follows:

$$P_D = (T_J - T_A) / (R_{\theta JA})$$

Where:

T_J = Maximum device junction operating temp.

T_A = Maximum ambient operating temp.

$R_{\theta JA}$ = Junction to ambient thermal resistance, °C/W

T_J and $R_{\theta JA}$ are taken from the device specification and T_A is determined by the application environment.

Is a heat sink required?

If the total power dissipated in the device (P_T) exceeds the maximum power dissipation P_D then a heat sink must be used or a different device must be selected.

A heat sink size can be determined by first calculating the required heat sink to ambient thermal resistance $R_{\theta SA}$ as follows:

$$R_{\theta SA} = [(T_J - T_A)/P_{T(AV)}] - [R_{\theta JC} + R_{\theta CS}]$$

Where:

$R_{\theta JC}$ = device junction to case thermal resistance

$R_{\theta CS}$ = case to heat sink thermal resistance, °C/W

= 0.5 /W typical with thermal joint compound

$P_{T(AV)}$ = total average power dissipation, W

T_J = junction operating temperature, °C (from data sheet)

T_A = operating ambient temperature, °C

The $R_{\theta SA}$ required can now be compared to heat sink design specifications to determine the design type and size required.

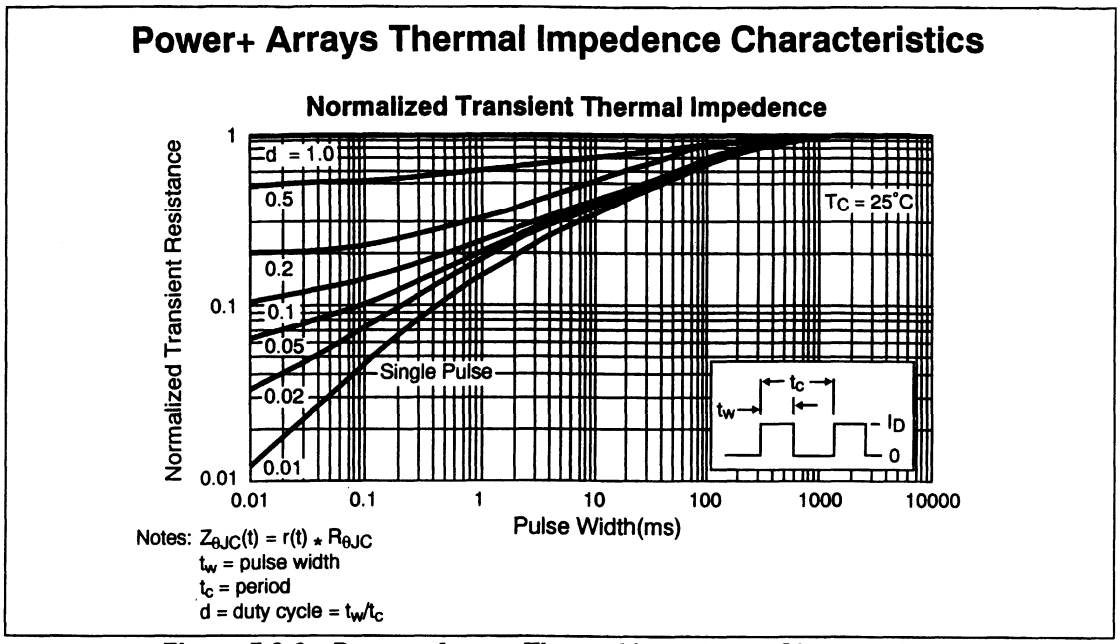


Figure 5.2.6 - Power+ Arrays Thermal Impedance Characteristics

The preceding thermal calculations were based on the assumption that the device average power was duty cycle dependent. This is true if the pulse widths are short in relation to the device thermal time constant. In the example of a switch that is "on" for one hour in every twenty four hours, the actual duty cycle is low but your system must be designed to accommodate 100% on time for the switch. The graph in Figure 5.2.6 gives the times associated with the Power+ Arrays.

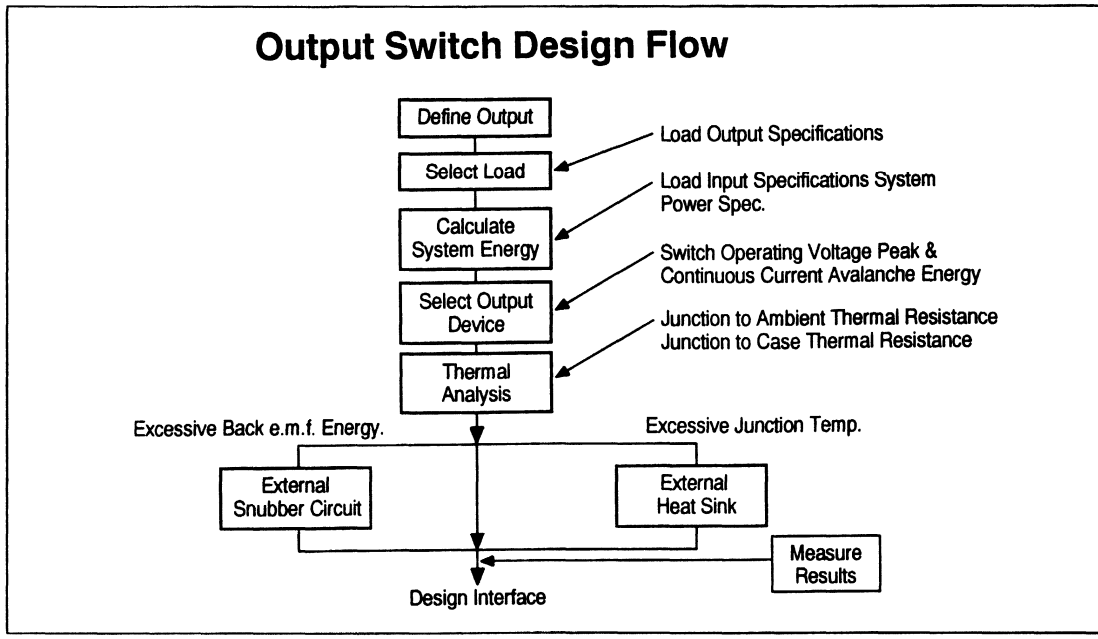


Figure 5.2.7 - Output Switch Design Flow

Conclusion

Summarizing the process, we begin with selection of a load based on the load output specifications. System energy can then be calculated based on the load characteristics, and load input specifications. A switching device can then be selected based on power and energy calculations. A thermal analysis based on the selected device thermal specifications will determine if additional heat sinking and external circuitry for back e.m.f. energy dissipation will be required.

The design of the switch section will be completed when actual measurements from the system are used to verify the design.

5.3 Stepper Motor Application

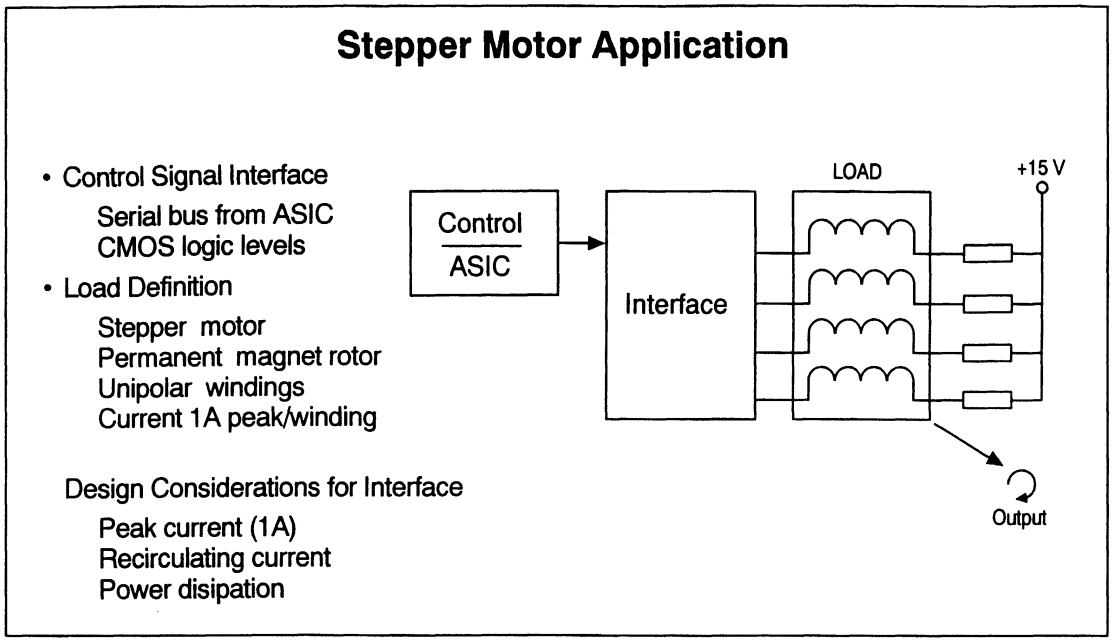


Figure 5.3.1 - Stepper Motor Application

Stepper motors are often chosen to provide incremental rotating motion. Some typical applications are printers, copiers, and industrial robots. Stepper motors present a multiple phase inductive load to the output circuit.

Figure 5.3.1 shows a block diagram of the application. The motor chosen has unipolar windings which require a peak current of 1A.

Load Description:

The first consideration in designing this application is to consider the load, which in this case is a Superior Electric stepper motor. The permanent magnet rotor stepping motor has two forms of stator winding. The bipolar stepping motor has a single winding on each stator pole and uses a full bridge to drive each phase winding. In the unipolar stepping motor, the flux reversal is accomplished by individually driving a bifilar winding on each pole. The windings are phased such that when current is passed through one winding, a given flux direction is generated. By passing current through the other winding, the opposite flux polarity is produced. Thus, the overall magnetic effect is the same as the bipolar motor, but the phase windings can be more economically driven by interface devices with open-drain outputs. The motor chosen for this application has unipolar windings. Due to the manner in which the windings are constructed when one winding is turned off a back e.m.f. voltage will be induced both in the winding that was turned off and in the other bifilar winding.

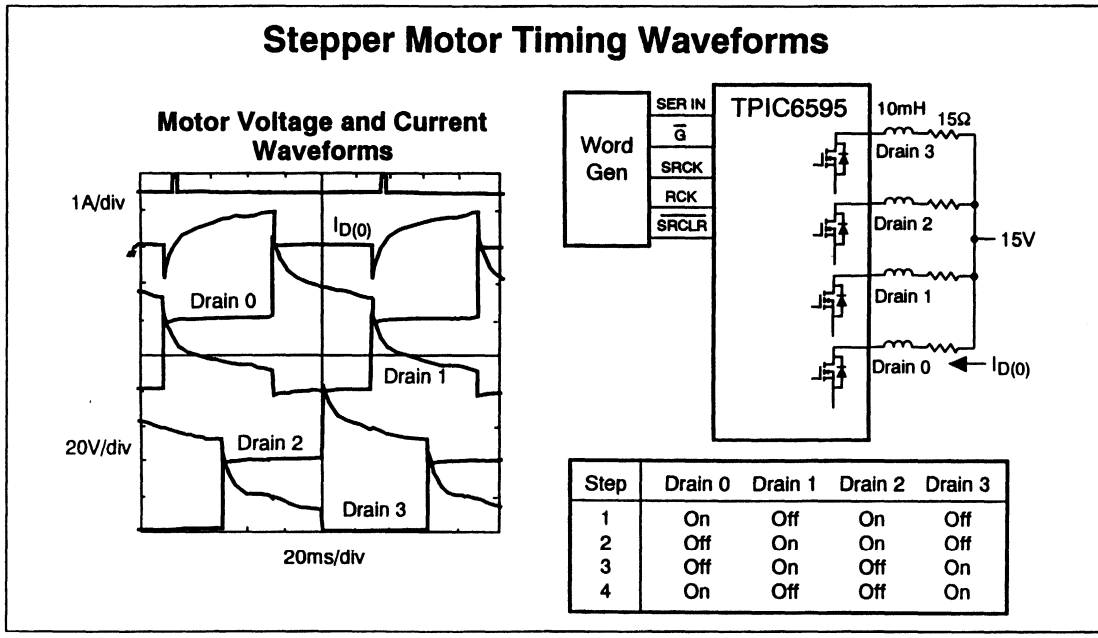


Figure 5.3.2 - Stepper Motor Timing Waveforms

Energy Calculations

Figure 5.3.2 shows a timing waveform of the stepping motor. The table in the lower right section shows the winding switching sequence. Additionally we can see that at any step two windings will be energized. With the knowledge that the windings are driven two at a time and by observation of the current waveform we can begin energy calculations. The value of back e.m.f. energy will remain the same as if it were all returned to one winding.

Observation of the timing diagram indicates t_{on} = 5 ms and that the winding current approximates a linear ramp (L/R > t_{on}). This indicates that the simplified formula will be a good approximation.

Therefore:

$$P_{on} = 1/3\ (I_P{}^2)^* r_{DS(on)}{}^* d$$

Where, d = 0.5 (each winding conducts twice in the four step cycle)

Note that in this example if the motor is stopped the current through each winding will be a steady 1 A. This brings up an important point. The power calculations are based on an assumed operating frequency. If the motor is stopped the individual drive currents may exceed the maximum continuous current rating of the switches. When calculating energy and power worst-case assumptions must be considered.

Choosing an Interface Circuit

For the application in Figure 5.3.2, the TPIC6595 has been chosen. This device was chosen because it can meet the power requirements, can drive all four windings from a single integrated circuit, and includes interface logic.

Figure 5.3.2 shows the TPIC6595 driving the stepper motor. The motor is driven at its rated 1 amp by operating two output DMOS transistors in parallel. In Figure 5.3.2, drain 0 is representative of output transistors 1 and 5 in parallel. Similarly, drain 1 is representative of output transistors 2 and 6, etc. Anti-parallel source-drain diodes are included for clarity. In this example, the input logic which would normally be provided by the system's microprocessor is provided by a Hewlett Packard HP8180A data generator.

The anti-parallel diodes are used to recirculate the current that is induced in the winding when the current through the previously activated winding on the pole is terminated. Hence, during each motor revolution both positive and negative current flows through the power switches which control the winding.

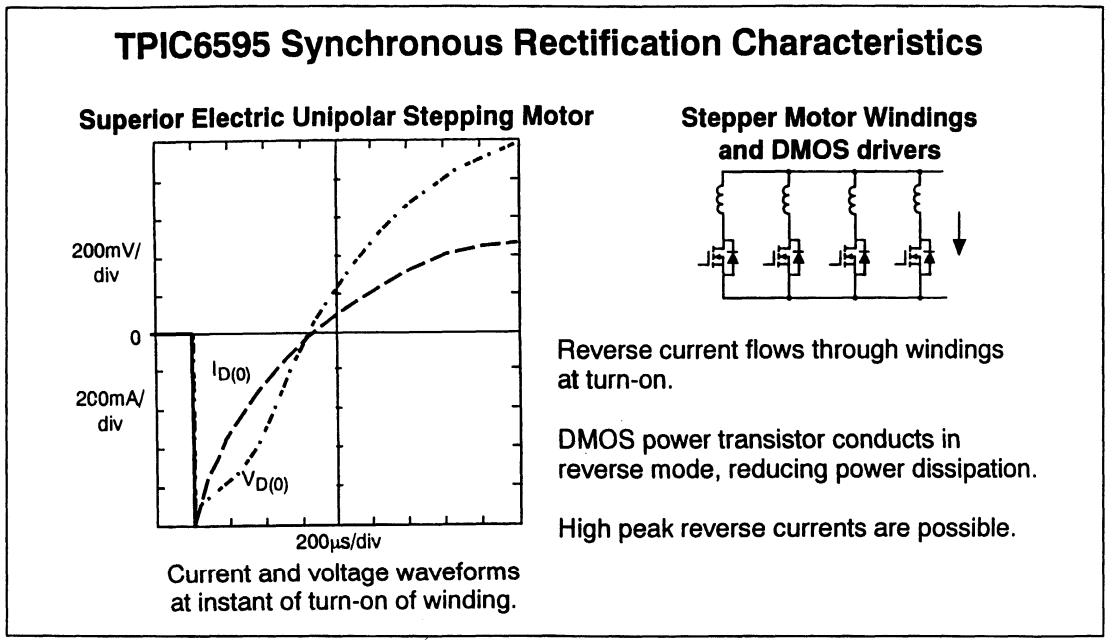


Figure 5.3.3 -TPIC6595 Synchronous Rectification Characteristics

Figure 5.3.3 shows an expansion of the wave forms of the negative current region of the winding pulse from the stepper motor application.

As previously mentioned, the anti-parallel diodes of the DMOS output allow the recirculation of current at winding turn-on. It is the anti-parallel diode which allows the DMOS output to withstand high peak reverse currents. In contrast, a power bipolar structure does not benefit from an inherent anti-parallel diode; one must be physically added, either to the integrated circuit design, or externally at the board level. If negative currents are required of a bipolar power switch which does not include such a diode, parasitic isolation diodes in the bipolar structure will conduct which may cause system malfunction. It is for this reason that a DMOS solution is often the most practical and economical for motor drive applications.

Returning to the stepper motor example, as the winding turns on the voltage drop across the output decreases. Once the voltage drop across the output ceases to be at least 0.7V , the

body drain diode no longer conducts. At this point, the DMOS power transistor turns on in the reverse direction, allowing continued negative current flow to the inductor.

Once reverse conduction through the DMOS becomes the vehicle for negative current flow to the inductor, the power dissipation is given by the product of $r_{DS(on)}$ and the square of the drain current. Reverse conduction continues through the DMOS transistor until the current reaches zero.

Why choose a Power+ Logic device for an application?

The DMOS output structure is power efficient.

The output structure can withstand high avalanche energy.

System design is simpler than with discrete DMOS or bipolar transistors.

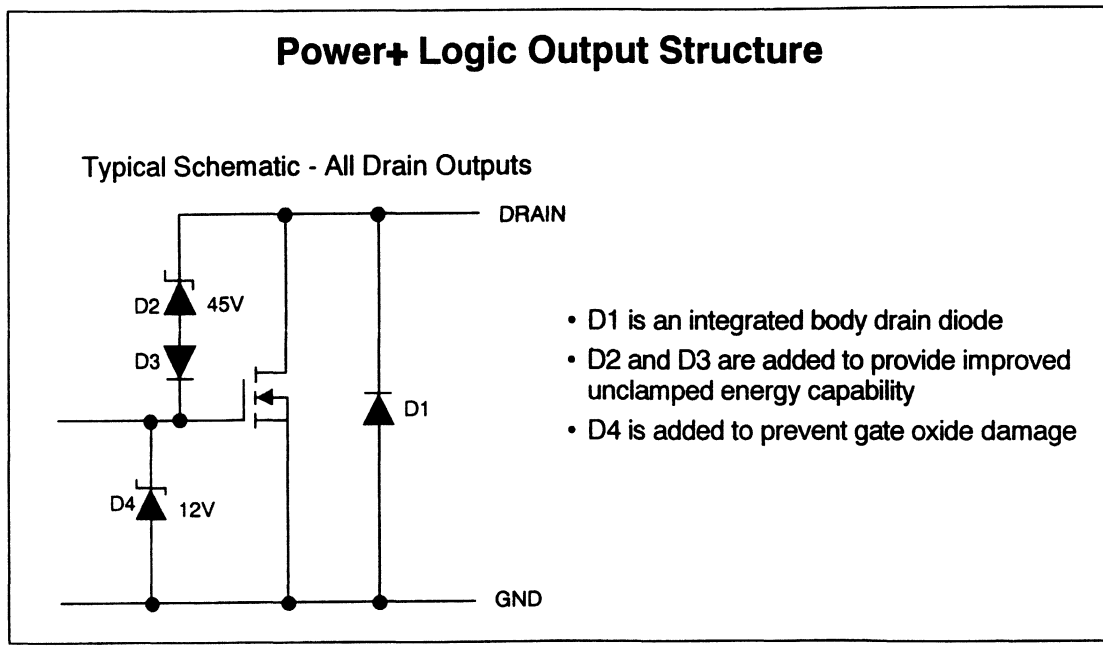


Figure 5.3.4 - Power+ Logic Output Structure

The TPIC6595 device has 8 power DMOS outputs with built-in 45V voltage clamps for enhanced inductive energy switching capability. When switching inductive loads, high voltage transients are seen at the device output when the output is placed in a high impedance state. The voltage generated by the inductive transient is limited by the breakdown mechanism of the output structure.

For the Power+ Logic devices, the internal dynamic 45V clamp circuit will eventually conduct during switching of an unclamped inductive load, allowing current to charge up the gate of the transistor. Once the DMOS gate voltage exceeds the threshold voltage of the device, the DMOS turns back on, completely dissipating the energy from the inductor.

Thus, the entire active area of the DMOS transistor is used in the forward bias mode to absorb energy from the inductive load. Without the internal clamp circuitry, the device output would be driven into avalanche breakdown, and would operate in the much lower energy capability reverse bias mode. The built-in voltage clamps of the Power+ Logic devices allow the user to switch up to 75 mJ of avalanche energy without the use of external snubber circuitry.

Each DMOS output of the TPIC6595 can provide 250 mA of continuous current with all outputs turned on. Individually, the outputs can be pulsed to provide up to 1.5 A of current. Or, multiple outputs can be paralleled for increased current drive of up to 6A of pulsed total load current. This rating is sufficient to drive the stepper motor when operating at the described duty cycle.

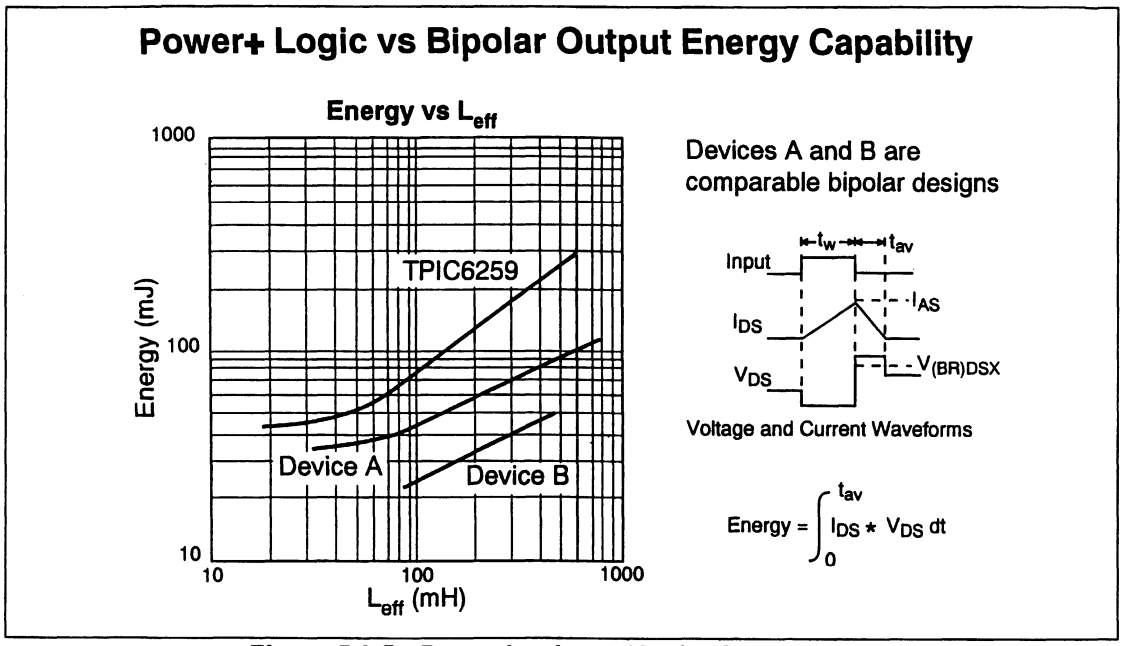


Figure 5.3.5 - Power Logic vs Bipolar Output Energy

In describing the ruggedness of any power output, a key parameter is the avalanche energy capability. While the maximum energy capability is determined by thermal limitations of the silicon, the energy that can be dissipated during avalanche is not a constant, but varies with peak switching current and load inductance. Some power structures, however, may be prematurely limited by secondary breakdown and will have a constant energy rating. For an inductive switching pulse within the energy capability of the device, the energy dissipated in the output is proportional to the product of the current and voltage wave forms.

Figure 5.3.5 benchmarks the ruggedness of the Power+ Logic devices against two low side bipolar devices having comparable voltage capability. Device A has a breakdown voltage of 37V, while device B has a breakdown voltage of 50V. Each bipolar device has approximately twice the output active area as the Power+ Logic devices. The data in the figure reflects the last point of output survival just prior to its destruction.

It is evident that the Power+ Logic DMOS device is much more rugged that either of the bipolar structures. While switching a 350 mH inductor, the TPIC6259 dissipates 200 mJ prior to destruction, more than twice the energy of the bipolar devices. Note that while the energy capability of the Power+ Logic devices decrease to 45 mJ while switching a 30 mH load, this is still significantly more than comparable bipolar devices.

Unclamped Inductive Switching Test Data

Maximum Energy Capability Prior to Device Destruction
T_j = Starting Junction Temperature = 25 °C

Device Type	I_{AS} (A)	t_{av} (ms)	V_{DSX} (V)	V_{DD} (V)	L_{eff} (mH)	L (mH)	E (mJ)	P_o (W)	K	T_m (°C)	T_{jpk} (°C)
DMOS	2.1	0.8	50	15.1	19	13.2	42.2	105.5	269.0	378	403
TPIC6259	1.7	1.4	50	15.1	42	29.4	58.1	83.0	269.0	394	419
Bipolar	1.3	1.5	37	9.0	41	30.7	35.4	48.8	139.5	122	147
Device A	0.9	2.6	37	12.8	101	66.3	43.9	34.4	139.5	114	139
	0.8	5.0	37	19.0	247	120.0	69.4	27.8	139.5	129	154
Bipolar	0.8	1.3	50	11.6	80	61.4	25.6	40.0	139.5	94	119
Device B	0.7	1.8	50	9.5	125	101.0	30.6	35.0	139.5	96	121
	0.5	3.4	50	15.0	335	335.0	41.9	25.0	139.5	95	120

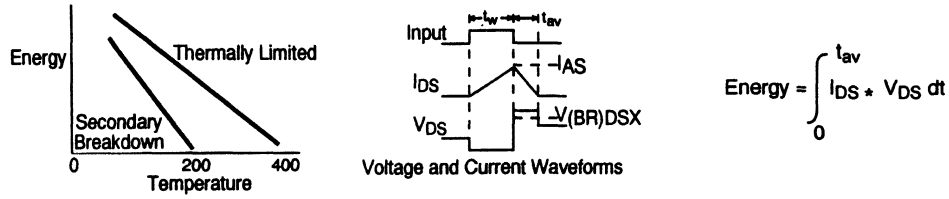


Figure 5.3.6 - Unclamped Inductive Switching Test Data

In addition to peak switching current and load inductance, the energy capability of a power device varies with temperature. As the junction temperature of the device increases, energy capability decreases. This temperature-energy relationship was exploited to further understand the avalanche energy capabilities of the Power+ Logic devices.

Unclamped inductive switching tests were performed on the Power+ Logic devices in which the junction temperature of the DMOS output was gradually raised by forcing the device to dissipate increasingly large amounts of energy. The virtual junction temperature of the device immediately prior to destruction was calculated. Note that for the purposes of these tests, the 150 °C maximum junction temperature specification of the Power+ Logic devices was violated; these tests do not reflect recommended operation of the Power+ Logic devices.

Assuming mechanical limitations of the package are disregarded, the maximum avalanche energy capability of a power device operating in the forward bias mode is limited by the thermal capabilities of the silicon. However, the actual avalanche energy dissipated by a given power structure may be prematurely limited by a secondary breakdown mechanism. In the case of the Power+ Logic outputs, the absence of forward secondary breakdown can be shown. The calculated virtual junction temperature of the Power+ Logic output structure at the point of device destruction was greater than 400°C. Since silicon is thermally limited at

approximately 400°C, silicon thermal limitations were the probable cause of device destruction.

For comparison, similar tests were performed on the bipolar devices A and B. Bipolar device B (50V clamp) had a calculated maximum virtual temperature of approximately 120°C immediately prior to destruction, clearly illustrating a secondary breakdown limitation. Bipolar device A (37V clamp) had improved characteristics, but still clearly experienced secondary breakdown limitations with destruction temperatures ranging from approximately 140°C to 150°C.

The following terms and definitions apply to figure 5.3.6:

I_{as} = Peak current reached during device avalanche

t_{av} = Time duration of device in avalanche

L = Load inductance

L_{eff} = Effective load inductance; accounts for supply voltage

E = Energy absorbed by device under test ($L_{eff} \times I_{as}^2/2$

V_{dd} = Output supply voltage

V_{dsx} = Effective device avalanche voltage

T_C = Case temperature

T_M = Maximum junction rise which occurs in inductive switching

P_o = Power = $I_{as} \times V_{dsx}$

K = 139.5 = A thermal constant where the area of active silicon = 1k mils square.

$= 2/(A(p\ kc)^{1/2})$

where A = Area of power generation silicon

p = density of silicon

k = thermal conductivity of silicon

c = thermal capacity of silicon

$T_M = (2^{0.5})/3\ Po\ k(tav)^{0.5}$

T_{JPK} = Peak junction temperature at point of destruction = $T_M + T_C$

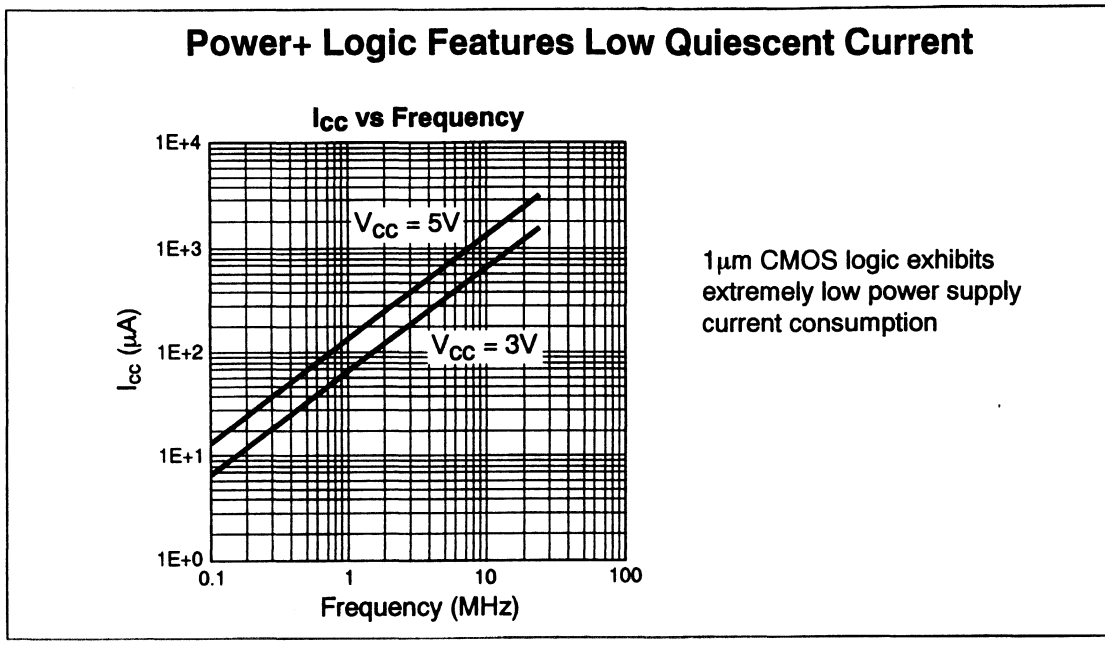


Figure 5.3.7 - Power+ Logic Features Low Quiescent Current

The Power+ Logic devices integrate performance power output structures with high-density sub micron CMOS logic. Figure 5.3.7 shows I_{CC} versus SRCK frequency for the TPIC6595 with the outputs static and an alternating bit pattern on the SER IN pin. This example demonstrates the high logic frequency capability of the Power+ Logic devices, as well as the low V_{CC} power consumption. Having high logic speed capability allows the information to be transferred from the µ-P interface very quickly even though the switch and load operation occurs at a much slower repetition rate. This would especially be important when cascading several devices for a large number of outputs all controlled by a single serial interface.

The power described in this graph is the term P_{quies} and is used in calculating the total average power dissipated in a device.

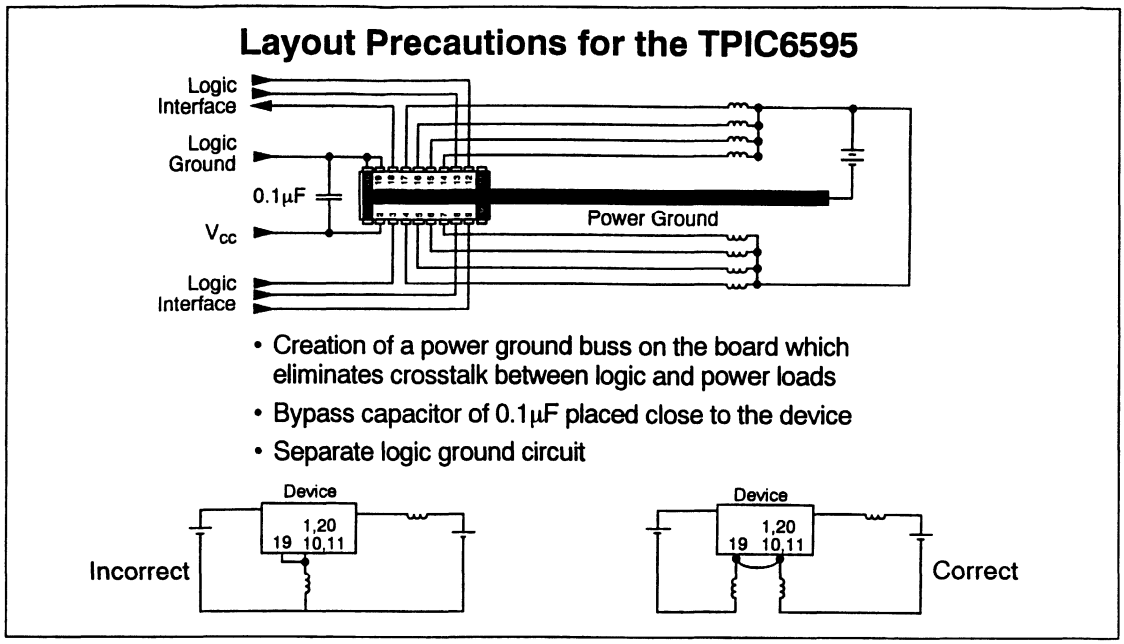


Figure 5.3.8 - Layout Precautions for the TPIC6595

When using the TPIC6595, or any of the Power+ Logic devices, there are several PCB layout considerations which should be kept in mind. High frequency layout rules should be used when designing power switching systems. This is because mutual inductance (i.e. capacitance between the drive circuit and load circuit) can cause coupling of erroneous signals resulting in false operation. The following precautions are offered:

Use of a power ground buss on the PCB to eliminate crosstalk between the power loads and input logic.

Addition of a 0.1 mF bypass capacitor between V_{CC} and the logic ground line, placed close to the device to dampen any stray signals experienced by the drive circuit.

Separate power and logic ground circuits.

Figure 5.3.8 shows the implementation of these board layout considerations using the TPIC6595.

5.4 Bi-directional Motor Drive Application

DC motors play an important role in a wide variety of electronic systems. Efficient control of motor speed and torque is an important issue for many system designers.

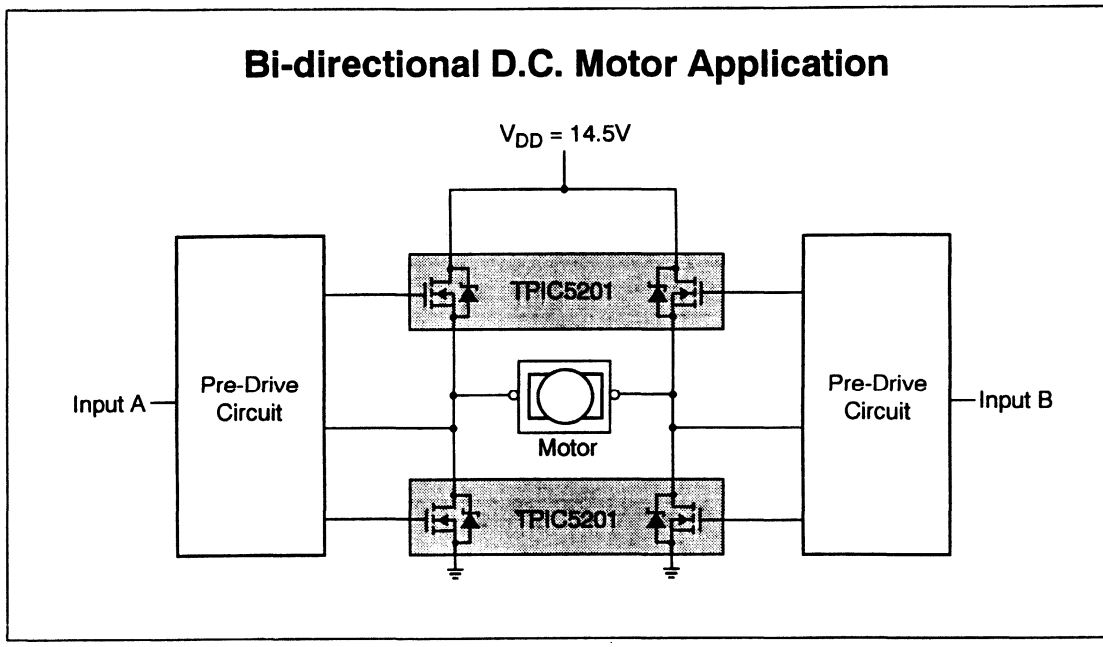


Figure 5.4.1 - Bi-directional DC Motor Drive

Figure 5.4.1 shows a bi-directional DC motor being driven from a 14.5 V supply by two dual DMOS switch devices arranged in a full H-bridge configuration. This circuit uses 20 kHz PWM input signals that are 180 degrees out of phase. In most systems, these signals would be supplied by a micro controller. A 50% duty cycle on both input signals produces a net zero voltage across the motor, creating a stall condition. Control of the motor's speed and direction of rotation is achieved by varying the duty cycle of one of the input signals while keeping the other fixed at 50% duty cycle. This variation between the input signals results in a net DC voltage across the motor, providing the drive current needed to meet the torque requirements of the motor.

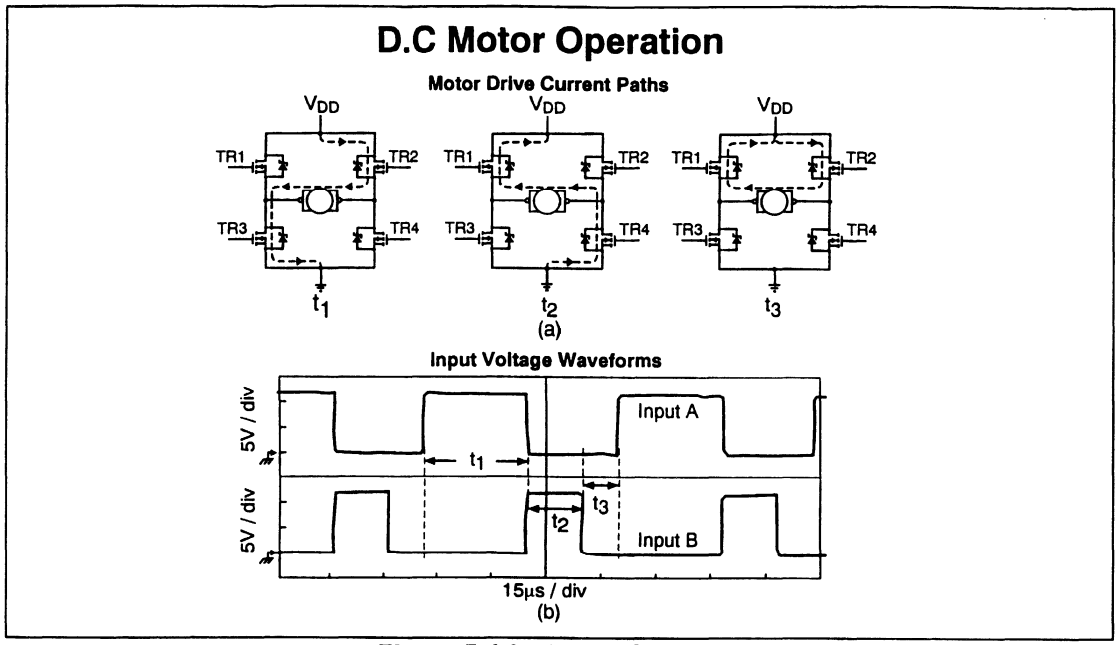


Figure 5.4.2 - Motor Operation

Motor Operation

Motor operation is shown in Figure 5.4.2. In this example, the motor is driven in the forward direction. The motor speed is controlled by varying the duty cycle of input signal B. While input signal A is high and input signal B is low, there is a net negative voltage across the terminals of the motor and current through the motor ramps up. Once input A goes low, a net positive voltage appears across the motor terminals and the motor current ramps down. When both input signals are low, there is no net voltage across the motor terminals, and the H-bridge recirculates a relatively constant current through its upper stages. To drive the motor in the reverse direction, input signal B is held to a 50% duty cycle, while the duty cycle of input A is varied.

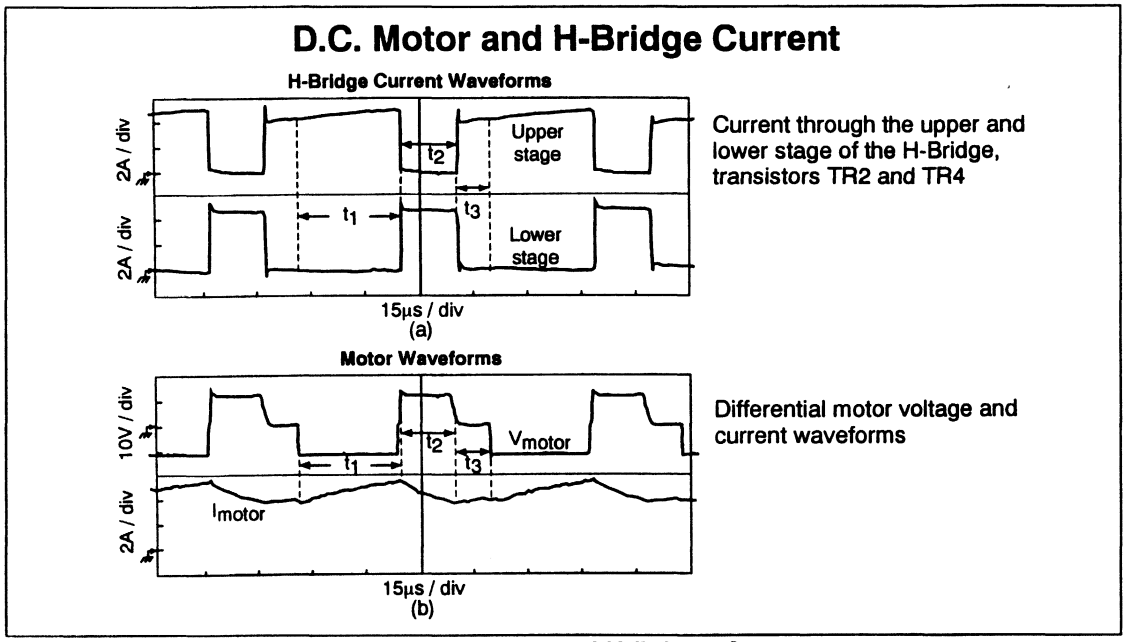


Figure 5.4.3 - Motor and H-Bridge Currents

Figure 5.4.3(a) shows the current through the transistors on one side of the H-bridge during time periods t_1, t_2, and t_3. Operation of the other side of the H-Bridge is similar.

Figure 5.4.3(b) shows the motor voltage and currents during the same time periods.

In this example, the pulse width of the input signal is approximately 25 µs at a 50% duty cycle. It is important to note that when switching both the upper and lower transistors on the same side of the H-bridge, a brief delay must occur to allow the conducting transistor to turn off before the non-conducting transistor is allowed to turn on. Without this delay, excessive cross conduction current may result. Cross conduction is a condition in which the upper and lower FET's on one side of the H-bridge are on simultaneously, providing a low impedance path between the source voltage and ground. While small cross conductance currents can actually be used to enhance system performance, uncontrolled cross conduction can result in excessive heat dissipation and degradation of the device.

System power considerations

The motor drive current shown in Figure 5.4.3(b) has a peak value of slightly less than 6 A with a minimum value of 4 A. Energy calculations must be based on the condition when one of the input signals is at the minimum duty cycle. The motor current during time t_3 is due to back e.m.f. and must be included in power dissipation calculations.

Choosing an Output Switch

The device required for this application must be capable of conducting at least 5 A continuous and as shown in the previous diagrams must be configured in an H-bridge.

TPIC5201 Power+ Array

- Two independent N-channel enhancement-mode DMOS transistors
- 7.5A continuous current per channel
- Low $r_{DS(on)}$ . . . 90mΩ typical
- 60V maximum output voltage
- 15A pulsed current per channel
- High avalanche energy rating - 120mJ

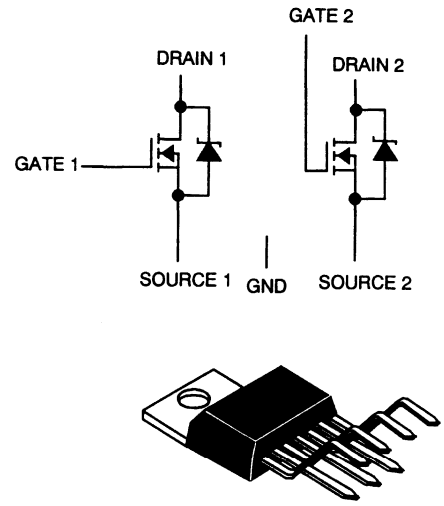


Figure 5.4.4 - TPIC5201 Power+ Array

The device chosen for this application is a TPIC5201 Power+ Array. This device contains two totally independent high performance DMOS transistors in a single power package. The independent transistors allow for an H-bridge configuration. The low $r_{DS(on)}$ minimizes the power dissipation.

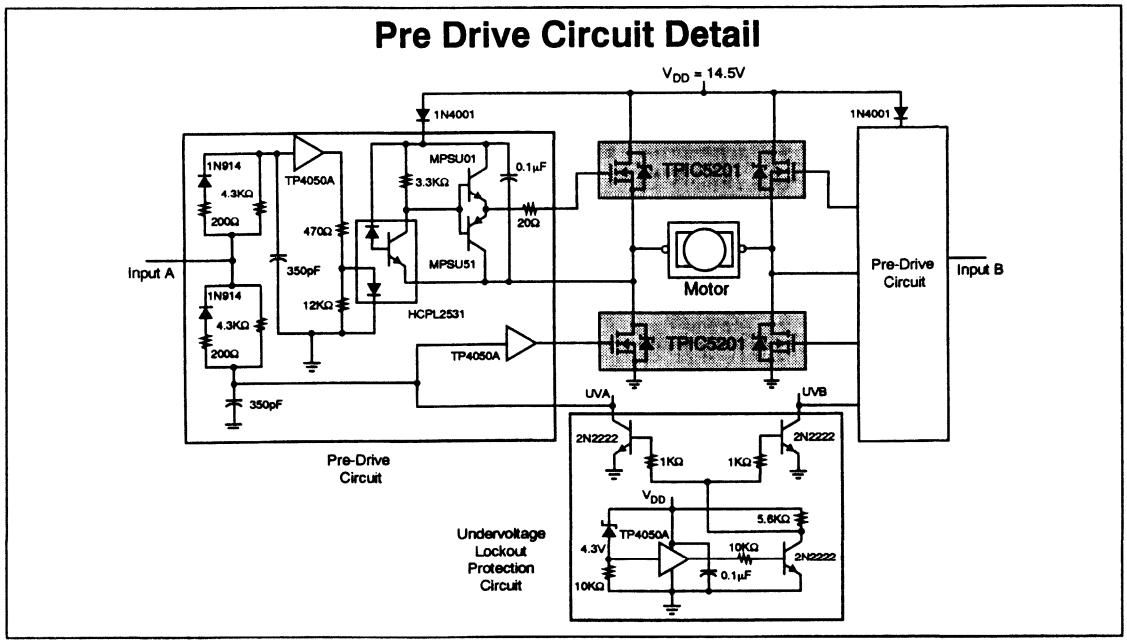


Figure 5.4.5 - Pre-drive Circuit Detail

Pre-Drive Circuit

In this application, two symmetrical pre-drive circuits are used to drive the gates of the upper and lower FET's. The pre-drive circuit schematic is shown in Figure 5.4.5. Drive to the upper transistors is achieved through the use of an HCPL2531 optocoupler followed by an emitter-follower stage. the high speed optocoupler isolates and level shifts the upper stage FET's from the input, while providing a reference to ground. The emitter-follower provides low impedance drive for fast charging of the intrinsic gate-source capacitor to enhance switching times.

A 0.1 μF bootstrap capacitor is used to allow the gates of the upper FET's to rise above the supply voltage rail. The bootstrap must be at least 10 times larger than the parasitic gate capacitance of the TPIC5201, typically 18 nF. Inclusion of the emitter-follower and the bootstrap capacitor allow the upper transistors to be turned on hard when the input signal transitions high.

The low gate capacitance of the TPIC5201 allows for improved efficiency in the motor control circuit. In a power switching application, as the switching frequency increases, switching losses due to the continuous charge and discharge of the gate capacitor become the dominating component of the power loss. By minimizing typical gate capacitance, the TPIC5201 reduces switching losses, which results in reduced system power consumption, and improved system efficiency.

The pre-drive circuit includes a delay RC network to insure that cross conduction does not occur. The time constant of this RC network must be greater than the 0.8 μs propagation delay associated with the switching times of the HCPL2531 optocoupler. By delaying the turn-on drive to the gates of the power MOSFET's, cross conduction currents are eliminated.

External under-voltage lockout protection is added to the circuit to keep the lower stage FET's turned off until a pre-defined threshold voltage is obtained. This threshold voltage is determined by the threshold of the zener diode coupled with the threshold of the TP4050 buffer. In this circuit, the lower FET's remain off between 2 V and 6.2 V.

Advantages Over Discrete Transistors

Since the two power MOSFET's of each TPIC5201 are fabricated monolithically, the FET's within each device are inherently well-matched. As a result, there is little variation in the switching times and transconductance of the upper stage transistors. This device-matching aids in system design by significantly reducing the need for feedback circuitry to compensate for potential switching time mismatches. As a result, the necessary pre-drive circuitry is greatly simplified.

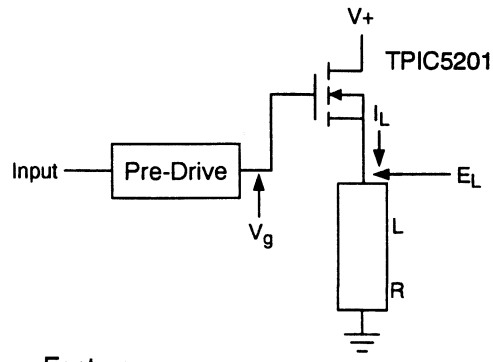
Each power transistor in the TPIC5201 features a low on-resistance of 90 mΩ. By minimizing on-resistance, the power consumption of the H-bridge is reduced, increasing the power available to the motor. Motor control systems built with low on-resistance power switches allow more efficient motor performance.

The energy capabilities of the TPIC5201 have been characterized over its entire range of operation. The specifications for the TPIC5201 include peak avalanche current versus avalanche time rating curves. Unlike the single point energy specifications typical of discrete MOSFET's, designers using the TPIC5201 can accurately monitor compliance with active safe operating area design constraints.

5.5 Solenoid Application

Solenoids are used to provide linear motion. Solenoid applications include electric locks on automobiles, mechanism actuators in tape recorders, and air control valves.

Solenoid High Side Drive Application



Features

- High side drive
- Back emf conduction through DMOS switch
- Solenoid
  L = 300mH
  R = 20Ω

Figure 5.5.1 - Solenoid Application

Figure 5.5.1 shows a solenoid with a high side driver. The high side drive places the control switch between V_{CC} and the load. Selection of a switch device for this application must include an energy evaluation and a device which can operate as a high side switch. The solenoid load is inductive like the stepper motor, however instead of having cross coupled signals the solenoid has a dynamically changing impedance.

When the current reaches a level sufficient to cause the solenoid to operate the armature begins to move. When the armature moves relative to the coil the coil inductance changes. The amount of change is a function of the solenoid design. Conventional relays also exhibit this change in inductance since they are solenoids which operate switches.

Energy and power considerations are similar to the stepper motor. The interface circuit must drive an inductive load with a peak current. The solenoid winding inductance and resistance must be considered when evaluating the avalanche energy. Just as with any inductive load the total avalanche energy must be considered as well as the peak avalanche current.

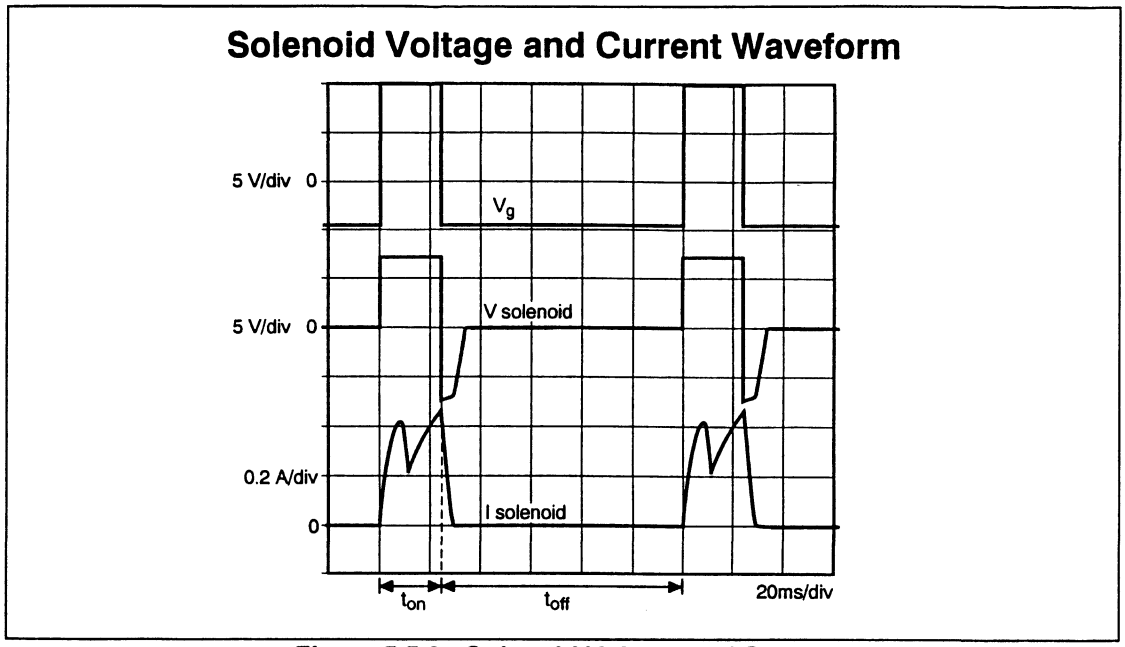


Figure 5.5.2 - Solenoid Voltage and Current

The voltage and current waveforms for the solenoid are shown in Figure 5.5.2. This particular solenoid was chosen because of the drastic inductance change during operation. The inductance change causes the discontinuity seen in the inductor current during t_{on}.

Notice that V_g, the output from the pre-drive circuit, is at -5 V during t_{off}. The circuit as shown relies on the DMOS transistor to provide the conduction path for the back e.m.f. current from the inductor when the drive is turned off (t_{off}). This was described in the stepper motor application Section 5.3. When the switch is turned off the solenoid voltage goes negative. When the solenoid voltage reaches approximately -7.5 V (V_g - 2.5 V) the DMOS transistor is turned on, effectively clamping the inductor voltage. If V_g = 0 V at t_{off} then the solenoid voltage would be clamped at -2.5 V and the time required for the solenoid current to reach zero would be longer.

Power & Energy Calculation

Switching

$E_T = 113$ mJ

$P_{off} = 940$ mW

$P_{on} = 2$ mW

$P_T = 942$ mW

Continuous

$P_{on} = 32.4$ mW

$$E_T = \frac{3L\ I_P^2\ V_{CL}}{6\ (V_{CL} - V_{SS}) + 4\ R_L\ I_P}$$

$$P_{off} = E_T * f$$

$$P_{on} = \frac{1}{3}\ (I_P^2)\ r_{DS(on)}\ d$$

$$P_T = P_{off} + P_{on} + P_{quies}$$

$$P_{on} = I_P^2 * r_{DS(on)}$$

$t_{on} = 25$ms
$t_{off} = 95$ms
$V_{SS} = 12$ V
$V_{CL} = 8$ V
$L_H = 300$ mH
$I_{Pk} = 0.5$ A
$r_{DS(on)} = 90$ mΩ
$P_{quies} = 0$

Figure 5.5.3 - Solenoid Energy Calculation

Using the current waveforms from Figure 5.5.2 the energy dissipated in the switch can be calculated. A TPIC5201 Power+ Array has been chosen as the switch for this application.

Using the calculations presented in Section 5.2:

$E_T = 3(L_H * I_P^2 * V_{CL})/[6(V_{CL}-V_{SS}) + R * I_P]$
$= 113$ mJ

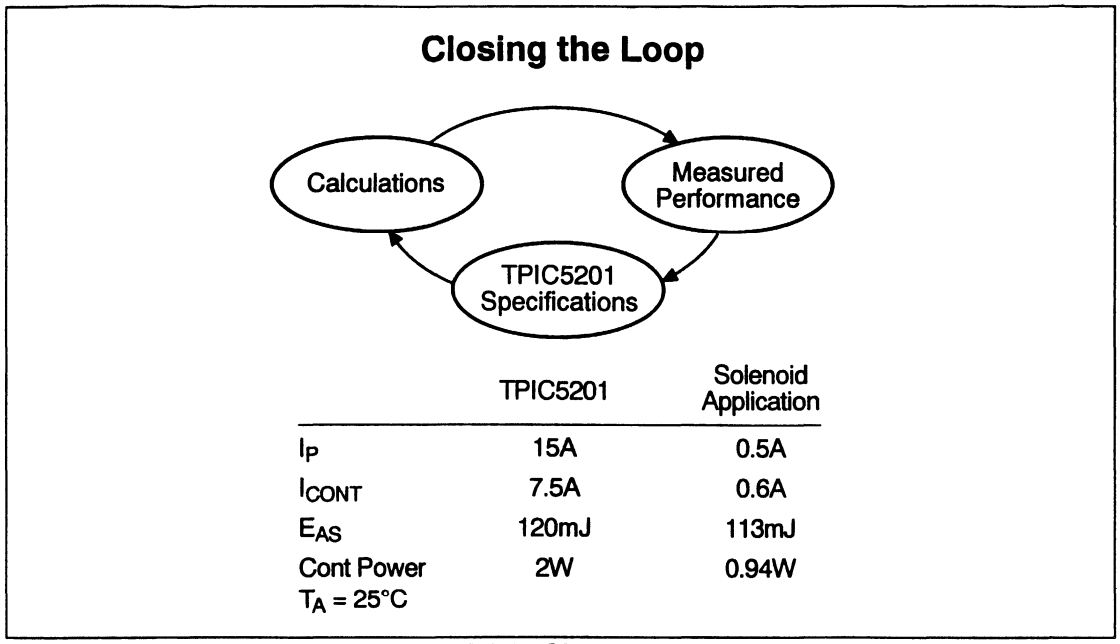
$P_{off} = E_T * f$
$= 0.94$ W

$P_{on} = 1/3\ I_{PK}^2 * r_{DS(on)} * d$
$= 7.5$ mW

$P_{T(av)} = P_{off} + P_{on} + P_{quies}$
$= 0.94$ W

Assuming that the solenoid could be turned on for an extended period of time the power dissipated in the switch would be :

$P_T = I^2 * r_{DS(on)}$
$I = V_{CC} / R$
$= 0.6$ A
$P_T = 0.6^2 * 0.09$ W
$= 32.4$ mW



	TPIC5201	Solenoid Application
I_P	15A	0.5A
I_{CONT}	7.5A	0.6A
E_{AS}	120mJ	113mJ
Cont Power T_A = 25°C	2W	0.94W

Figure 5.5.4 - Closing the Loop

Closing the design loop and comparing calculations, results and specifications will verify the design and indicate changes when necessary.

The results of this comparison are not what would be expected. The avalanche energy is high (113 mJ) while the power dissipation is quite low (0.9 W). This indicates that no heat sinking is required and that a device with a lower power and current rating could be used in this application. It also illustrates the importance of doing thorough energy calculations. In this case a quick look at current handling alone might suggest the device chosen is overkill, but when avalanche energy is considered we can see the TPIC5201 is a good match for the application. A similar device rated at a lower peak current value would probably be unable to handle the avalanche energy, possibly resulting in repeated "mysterious" device failures.

5.6 Incandescent Lamp Application

Incandescent lamps are found in many industrial applications as well as automotive, marine and aeronautical applications. Incandescent lamps provide high output energy with rugged construction.

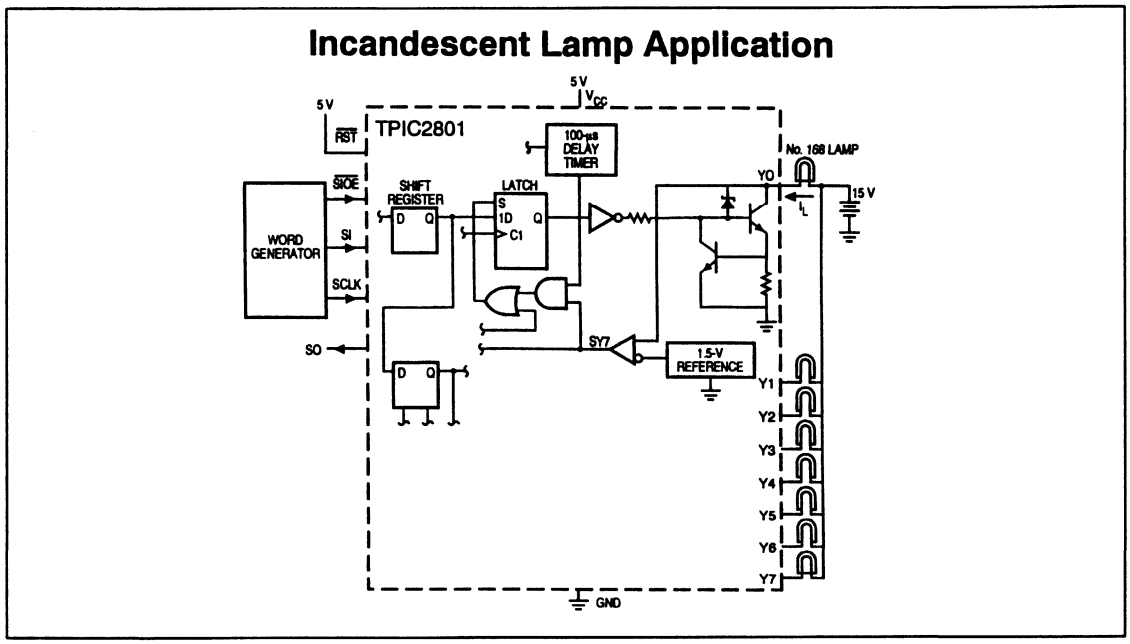


Figure 5.6.1 - Incandescent Lamp Application

The circuit in Figure 5.6.1 shows an application driving eight automotive lamps from a 15V source. Incandescent lamps present a unique resistive load. The filament resistance increases dramatically as the lamp warms up to operating temperature.

Incandescent lamps are often operated with extended on time which results in a very low duty cycle for the inrush current. If inrush current duty cycle is very low, the power dissipation could be ignored. If the high peak current is ignored premature failure of the switch transistor is likely. If the switch transistor is selected to accommodate the lamp peak current then circuit size and cost are sacrificed.

One solution is to current limit the inrush current. A conventional linear current limiting circuit would require dissipation of a large amount of heat during the warm up time. The choice of an Intelligent Power device such as the TPIC2801 allows the output circuit to be implemented with a single integrated circuit. The TPIC2801 contains eight 1A/30 V low-side switches packaged in a 15 pin Single-In-Line package (SIP). The eight switches are controlled with a single input, SI (Serial Input), by an 8-bit serial word. Diagnostics are also provided through the output, SO (Serial Output). Independent over-voltage and over-current protection are provided to all eight switches.

Circuit Operation

Shift register data is latched into the parallel latch and output switches are activated by the new data on the rising edge of the SIOE-pulse following the data word. However, to allow the part to overcome high in-rush current, such as the lamp cold filament current, an internal 100 µs delay timer is started at the SIOE-pulse rising edge during which time the switch over-voltage fault shutdown circuit is inhibited. During this 100 µs interval the switch is protected by an internal current limiter, which is set to regulate the current to approximately 1.5 A. Once the

output switch with output voltage greater than 1.5 V is latched off. It is important to note that these current-limited, 100 μs, soft start bursts of power not only protect the TPIC2801, but also protect the lamp filament from an otherwise filament degrading high in-rush current.

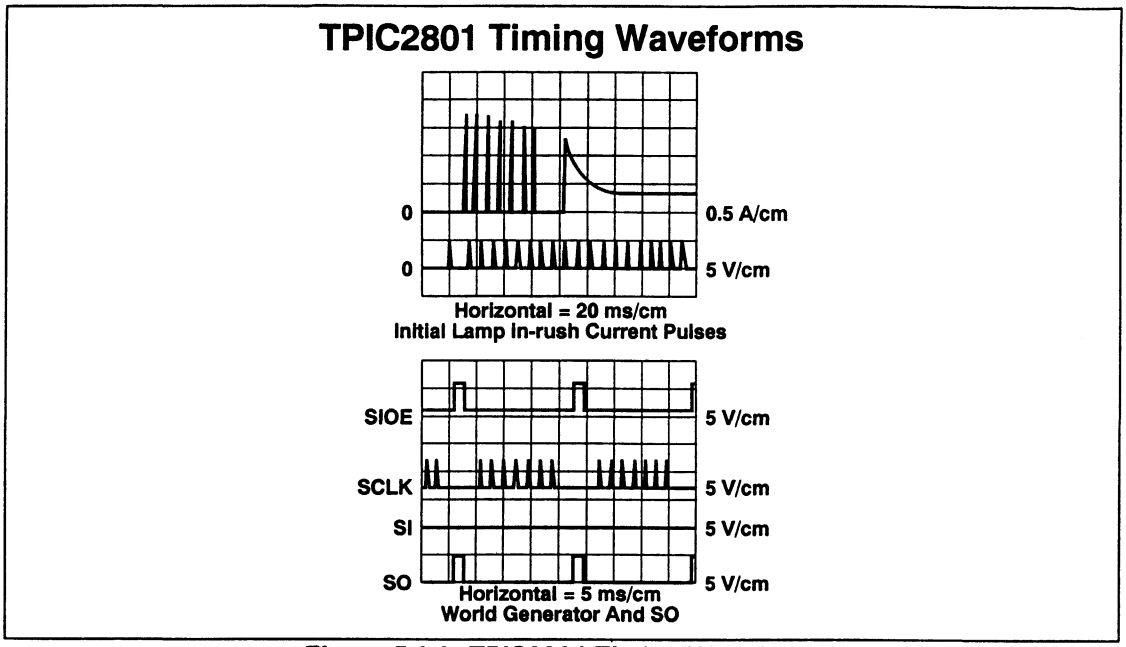
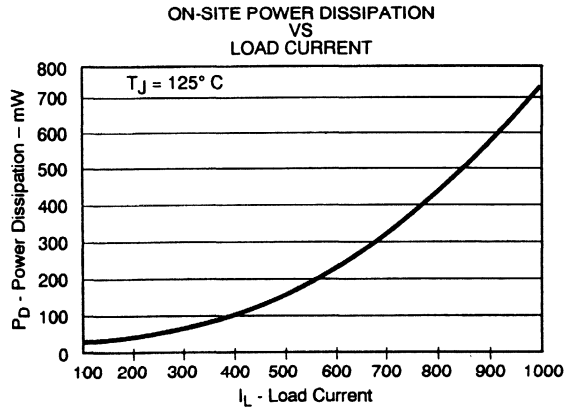


Figure 5.6.2 -TPIC2801 Timing Waveforms

The lamp current waveform shows the initial lamp in-rush current decrease from a value slightly greater that 1.5 A to a value of less than 0.5 A during a period of approximately 120 ms. The current initially presented to the lamps is a series of pulses. The first pulse is a 1.5A / 100 μs pulse that is coincident with the rising edge of the first SIOE-pulse that follows the data word.

TPIC2801 Power and Thermal Considerations



TPIC2801
Power Dissipation
(Continuous Lamp Operation)

I = 0.5 A
P = 150 mW (from chart)
P_T = P(Y0...Y7) + P_{quires}
= 8 * 0.15 + 1.25
= 2.45 W

TPIC2801 Ratings
I_{CONT} = 1A/Ch
$P_{CONT}(T_A = 25°C)$ = 3.575 W

Figure 5.6.3 -TPIC2801 Power and Thermal Considerations

Figure 5.6.3; the on-state power dissipation vs load current chart can be used to determine the dissipation of each output. This chart takes into consideration the bipolar transistor saturation voltage and the internal resistor I^2R power dissipation.

Calculation of the switch power dissipation for continuous duty cycle:

Output Switches Y0...Y7: I = 0.5 A , duty cycle = 1.0

From figure 5.6.3

$P(Y0...Y7)$ = 0.15W x 1.0 x 8 = 1.2 W

$P_{(QUIES)}$ = 0.25 A x 5 V = 1.25 W (per TPIC2801 data sheet)

$P_{T(AV)}$ = P(Y0...Y7) + $P_{(QUIES}$
= 2.45 W

The maximum power dissipation for the TPIC2801 at T_A = 25 °C is 3.45W.

The self-protection capability of the TPIC2801 along with its power handling capability makes this a good selection for this design .

Additional features include the ability to switch high currents and inductive loads. This device is well suited for switching high energy unclamped inductive loads since each of the eight power switches is equipped with an internal 35-V collector-to-base voltage clamp. The current

capability of a single switch can be extended by parallel switch operation. This application utilized one of a series of intelligent power devices.

Other Intelligent Power devices are available with different configurations and feedback features providing effective system solutions for output systems.

5.7 Power+ Product Summary

Power+ Product Configuration

Power+ Arrays — Multiple MOSFET in a Single Package

TPIC2202	2 Channel	Common-Source	Power	DMOS	Array
TPIC2301	3 Channel	Common-Source	Power	DMOS	Array
TPIC5201	2 Channel	Uncommitted	Power	DMOS	Array
TPIC2701	7 Channel	Common-Source	Power	DMOS	Array

Power+ Logic Multiple MOSFET and Interface Logic in a Single Package

TPIC6259	Power+ Logic	8-Bit Addressable Latch
TPIC6273	Power+ Logic	Octal D-Type Latch
TPIC6595	Power+ Logic	8-Bit Shift Register

Intelligent Power — Power Outputs, Interface Logic and Diagnostics in a Single Package

TPIC2801	Octal Intelligent Power Switch with Serial Input
TPIC2404	Intelligent Power Quad Low-Side Switch
TPIC2406	Intelligent Power Quad MOSFET Latch

Figure 5.7.1 - Power+ Product Configuration

Power+ products are available in many configurations. The table in Figure 5.7.1 shows the Phase 1 products for Power+ Arrays and Power+ Logic and some of the Intelligent Power products. This chart can serve as a starting point in choosing the product which functionally fits an application.

Power+ Product Performance

Power+ Arrays

	Pkg	I_{CONT}	I_{MAX}	$r_{DS(on)}$	EAS	VDS
TPIC2202	KC	7.5A	15A	90mΩ	120mJ	60V
TPIC2301	KV					
TPIC5201						
TPIC2701	N	0.5A	3A	0.5Ω	22mJ	

Power+ Logic

	Pkg	I_{CONT}	I_{MAX}	$r_{DS(on)}$	EAS	VDS
TPIC6259	N	250mA	1.5A	1.3Ω	75mJ	45V
TPIC6273						
TPIC6595						

Intelligent Power

	Pkg	I_{CONT}	I_{MAX}	$r_{DS(on)}$	EAS	VDS
TPIC2801	KV	1A	1A	Bipolar xstr	40mJ	35V
TPIC2404	KN		1.5A			45V
TPIC2406	NE	0.7A	3A	0.5Ω	50mJ	60V

* I_{CONT} & I_{MAX} are per channel

Figure 5.7.2 - Power+ Product Performance

Selecting a Power+ product includes choosing a product that meets the application performance requirements. The chart in Figure 5.7.2 compares some of the key specifications off all three product families. These are the parameters most often used for an initial product selection.

The applications and design information presented in the previous sections have relied on some assumptions about device parameters in order to simplify the analysis while still arriving at a meaningful evaluation.

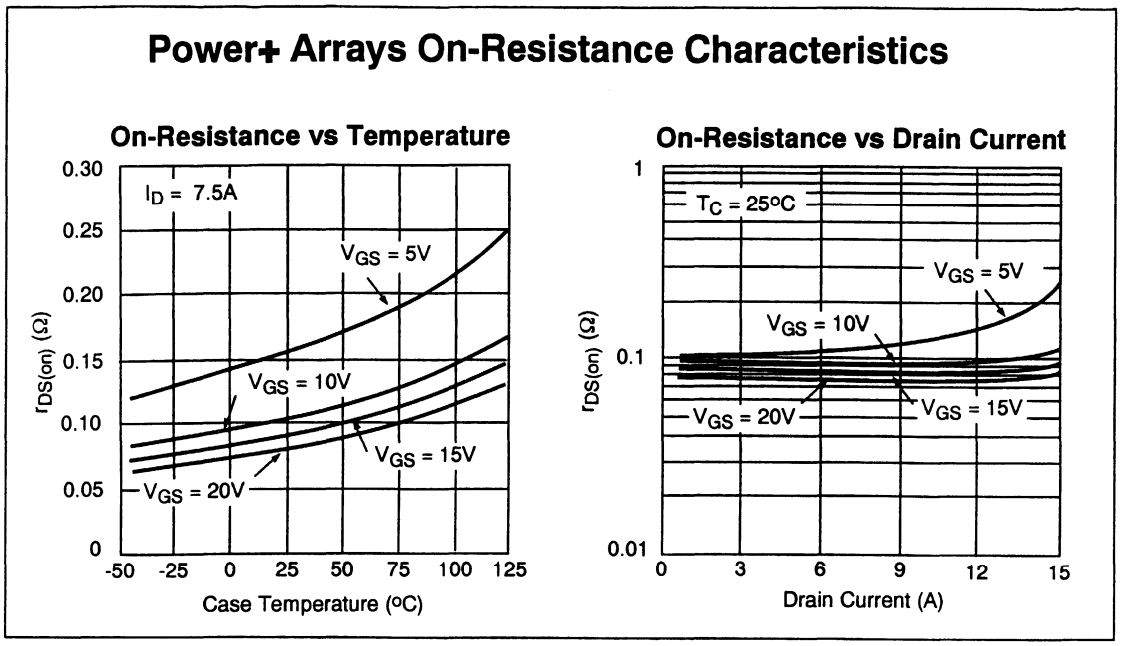


Figure 5.7.3 - Power + Arrays On-Resistance Characteristics

The two graphs in figure 5.7.3 show the excellent on resistance stability for the Power+ Array DMOS transistors. This also shows the type of device information available in the data sheet. Complete device characterization is provided in the data sheets for Texas Instruments Power+ products.

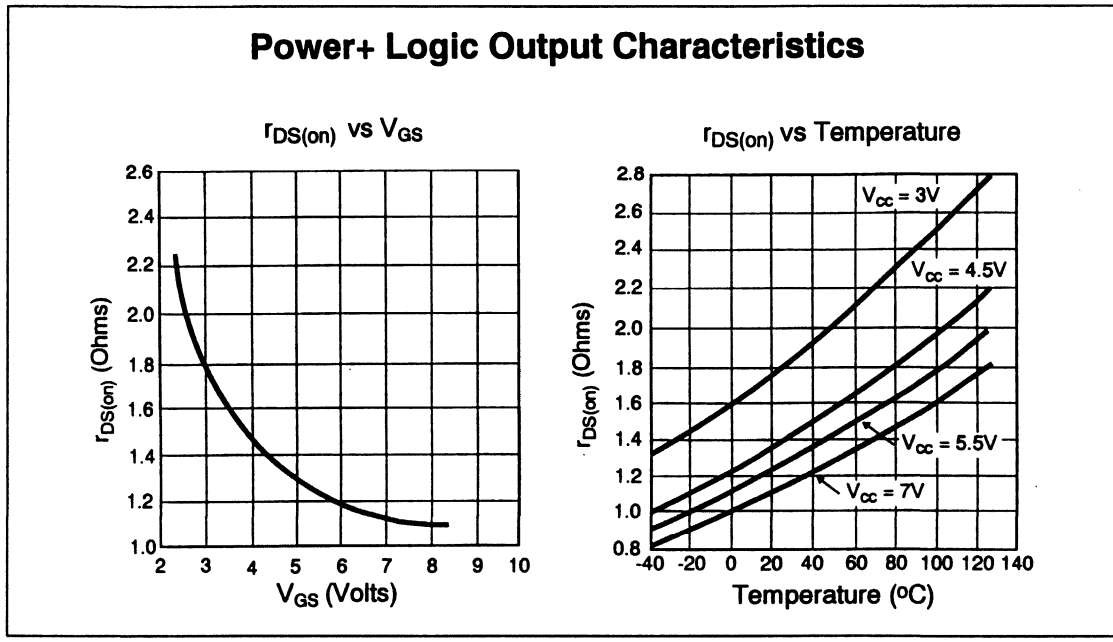


Figure 5.7.4 - Power+ Logic Output Characteristics

Figure 5.7.4 shows device on-resistance performance for the Power+ Logic family of devices. Note that while the $r_{DS(on)}$ is higher than that for the Power+ Arrays, the power handling for these outputs is still substantial as shown in the chart of Figure 5.7.2.

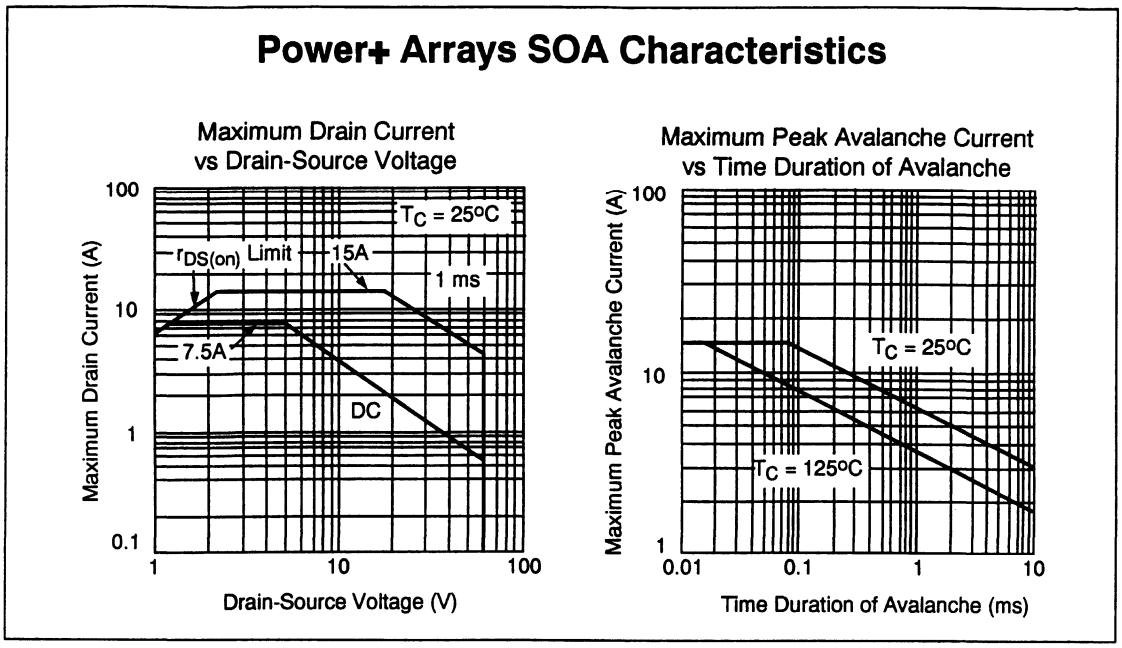


Figure 5.7.5 - Power+ Arrays Safe Operating Characteristics

The Safe Operating Area (SOA) characteristics are presented in graphical form to include peak currents and absolute times. Avalanche energy capability depends on many factors and cannot be adequately described by a single number. The graphs in Figure 5.7.5 indicate the relationship between safe avalanche operating conditions and time, temperature, and current for Power+ Arrays. Similar information is included in the data sheets for other Power+ products.

TPIC2404
50-W Intelligent-Power Quadruple Low-Side Switch

TEXAS INSTRUMENTS

Contents

List of Illustrations

Introduction

The TPIC2404 is a monolithic, quadruple, low-side intelligent power switch packaged in a 15-pin Single-In-Line Package (SIP). It is capable of switching in harsh electrical and thermal environments; a capability inherent by design of its four 1-A power output switches to have overvoltage, overtemperature, and current-limiting protection.

The TPIC2404 has a high current gain, 16,667 minimum, and is recommended for interfacing from low-power 5-V logic controls (60-μA maximum input current) to peripheral loads such as incandescent lamps, relays, solenoids, dc motors, stepping motors, and other loads requiring up to 45-V supply voltage. Also, the TPIC2404 has a fault-sensing circuit that monitors for open and shorted loads, overvoltage shutdown, and thermal shutdown. When a fault is sensed, the $\overline{\text{FAULT}}$ output goes low (see Figure 1 and Table 1).

In addition to the direct drive of peripheral loads, the TPIC2404 is also recommended for driving power bipolar and power MOSFET transistors. A power bipolar transistor switching amperes of load current requires several hundred milliamperes of base current for saturated switching. A power MOSFET transistor, when switching at high speed, also requires several hundred milliamperes of peak gate drive current, although its average gate drive current is usually minimal.

Table 1. TPIC2404 Function Table

	ENABLE	A	Y	$\overline{\text{FAULT}}$
Normal operation	H	H	L	H
	H	L	H	H
	L	X	H	H
Open load	H	L	L	L
Short to GND				
Overvoltage shutdown	H	X	H	L
Thermal shutdown				
Short to V_{CC}	H	H	H	L

Functional Description

Error Sensing

The error sensing circuit monitors the outputs for open and short conditions by sensing and comparing the input state to the output state. An error condition is generated when the input voltage (V_I) and output voltage (V_O) are logically the same. This condition can exist for overvoltage shutdown, thermal shutdown, open loads, and output shorts to V_{CC} and to GND. When one of these conditions is sensed, the $\overline{\text{FAULT}}$ output will go to a low state and the current sink is activated. An external filter is required to eliminate false pulses due to switching. Unused outputs should be left open and unused inputs should be tied high to avoid false errors.

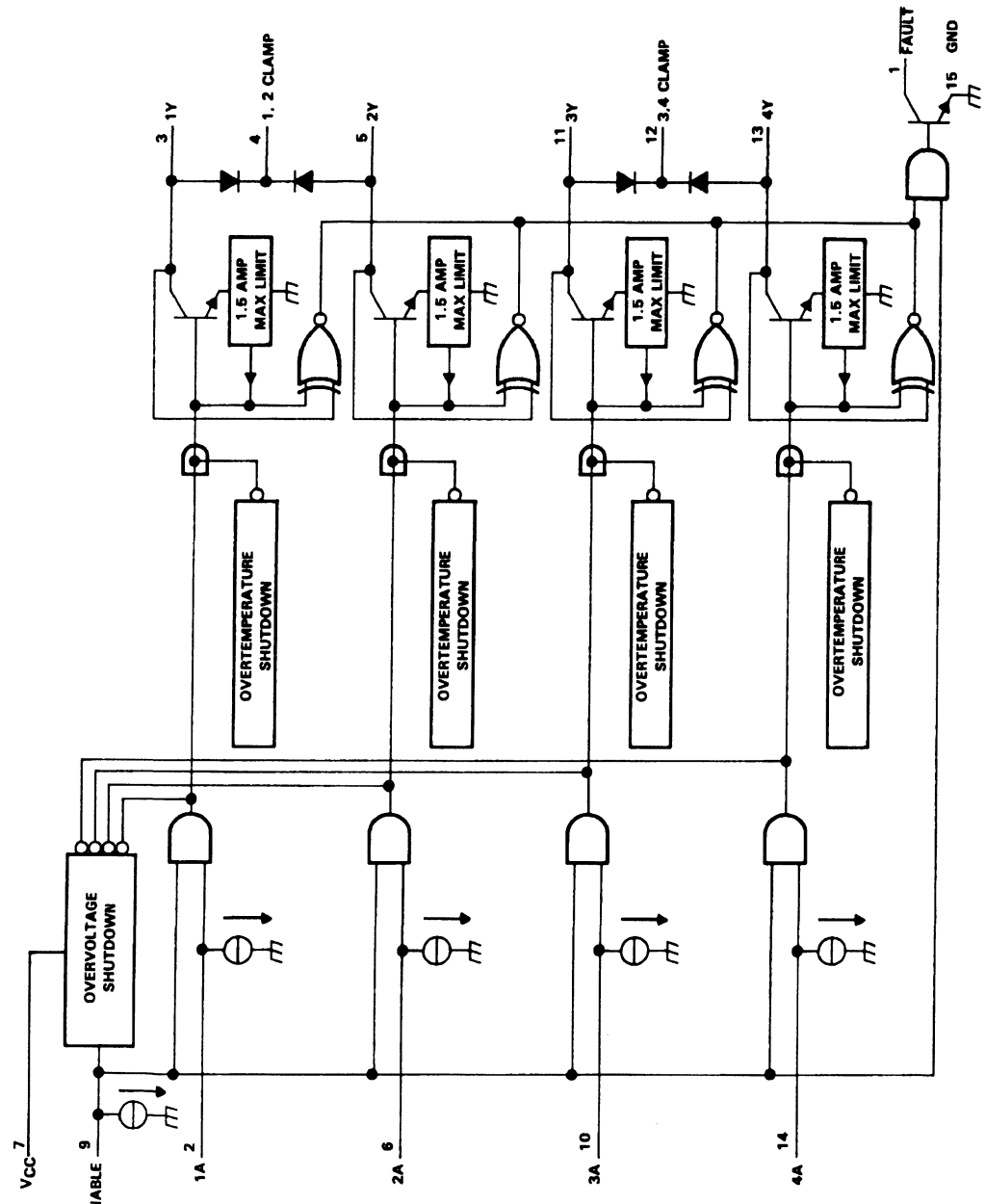


Figure 1. TPIC2404 Logic Diagram

Thermal Shutdown

Independent thermal shutdown circuits monitor and disable each output when the maximum temperature is reached, typically 155 °C. A fault condition is then sensed and reported by the error sensing circuit. This condition remains until the temperature falls below 140 °C and the thermal shutdown circuit allows the output to return to normal operation.

Overvoltage Shutdown

When the supply voltage exceeds the overvoltage condition of 25.5 V to 31 V, all outputs are disabled and a fault condition is sensed. When the supply voltage falls below 25.5 V, the fault condition is removed and the outputs return to normal operation.

Overcurrent Limit

The overcurrent limit is the maximum current each output is independently allowed to sink. The current limiting circuitry monitors the output transistor's emitter current and limits its base drive when the maximum output current limit is reached. The output functionality is not affected nor is a fault condition reported.

Inputs

All inputs have a current sink controlled by ENABLE, which ensures that an open input is pulled down to GND causing the output to be off.

Application Design Considerations

Power and Thermal Considerations

Power dissipation of the TPIC2404's individual switches is a function of output load current and is determined from the graph in Figure 2. The requirement for external heat sinking is calculated based on the device's total average power dissipation, maximum junction temperature, and ambient operating temperature as seen in equation (1).

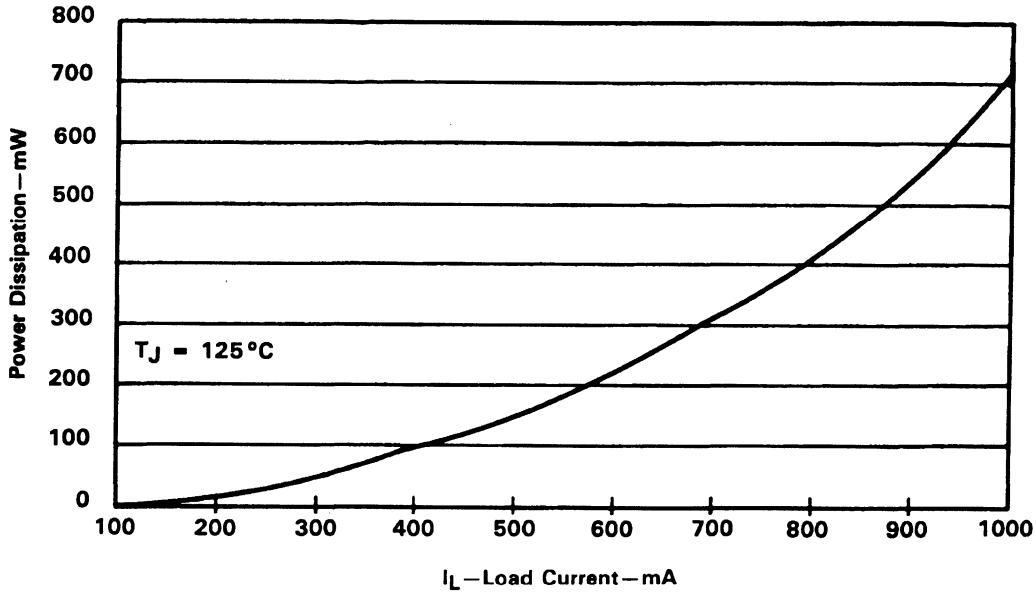


Figure 2. Typical Power Dissipation vs Load Current

$$R_{\theta SA} = \frac{T_J - T_A}{P_{T(AV)}} - |R_{\theta JC} + R_{\theta CS}| \quad (1)$$

Where:

$R_{\theta SA}$ = heat sink thermal resistance, °C/W

$R_{\theta JC}$ = device junction-to-case thermal resistance
= 2.5 °C/W

$R_{\theta CS}$ = case-to-heat sink thermal resistance, °C/W
= 0.5 °C/W typical with thermal joint compound

$P_{T(AV)}$ = total average power dissipation, W

T_J = maximum junction temperature, or operating junction temperature

T_A = operating ambient air temperature, °C

If the $R_{\theta SA}$ calculated is less than 47.5 °C/W, an external heat sink is required. The size heat sink necessary to achieve the required $R_{\theta SA}$ can be determined from Figure 3 or from a heat sink catalog.

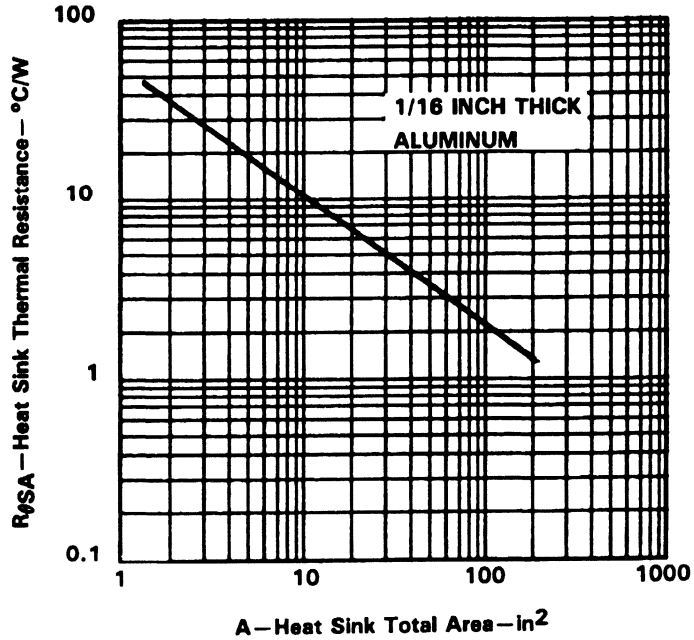


Figure 3. Typical Heat Sink Thermal Resistance vs Heat Sink Total Surface Area

Example 1: Determining Heat Sink Thermal Resistance and Size

Operating Conditions

T_A = 85 °C
T_J = 125 °C
Output Switch 1: I_L = 0.8 A, duty cycle = 0.8
Output Switch 2: I_L = 0.9 A, duty cycle = 1
Output Switch 3: I_L = 1 A, duty cycle = 1
Output Switch 4: I_L = 0.8 A, duty cycle = 0.7

The equations from Figure 2 are as follows:

P (switch 1) = 0.4 W × 0.8 = 0.32 W
P (switch 2) = 0.53 W × 1 = 0.53 W
P (switch 3) = 0.72 W × 1 = 0.72 W
P (switch 4) = 0.4 W × 0.7 = 0.28 W

Next, the total average power dissipation is calculated in equation (2).

$$P_{T(AV)} = P\ (\text{switch 1} + \text{switch 2} + \text{switch 3} + \text{switch 4}) \quad (2)$$

This number is then used to calculate the heat sink thermal resistance in equation (1).

$$R_{\theta SA} = \frac{T_J - T_A}{P_{T(AV)}} - |R_{\theta JC} + R_{\theta CS}| \quad (1)$$

$$= 18.6\,°C/W$$

From Figure 3, the heat sink total area (both sides) is $A = 5\ in^2$. Using this number for the area, the heat sink size can be determined using equation (3).

$$\sqrt{\frac{A}{2}} = 1.6\text{ in.} \times 1.6\text{ in} \quad (3)$$

Short-Circuit Safe Operating Area, SCSOA

When the TPIC2404 is operating from a load supply voltage less than 20 V, its self-protection features make it virtually indestructible. However, when the TPIC2404 is operating from a load supply voltage between 20 V and 45 V (its maximum output voltage), the TPIC2404's $\overline{\text{FAULT}}$ output must be monitored to detect faults. This is especially true for shorted loads since the $\overline{\text{FAULT}}$ output must be used to detect the fault and signal the microprocessor controller to immediately turnoff all the output switches. The controller turnoff is necessary at voltages of 20 V or greater because the TPIC2404's thermal shutdown time is longer than its short-circuit withstand time and uninterrupted shorted load current will cause output switch secondary breakdown and device destruction.

Parallel Operation of Quad Outputs for Extended Output Current Capability

If all four output switches are not needed for an application and an output load current greater than 1 A is required, the switches can be connected in parallel for an extended current capability. To demonstrate current sharing between the TPIC2404 switches, it is operated in the configuration of Figure 4 at $T_A = 25\,°C$ on various heat sinks. The load currents, I_L, of all four switches are measured at an approximate total load of 4 A. The current difference, ΔI, measured between any combination of switches is typically no greater than 40 mA (see Table 2).

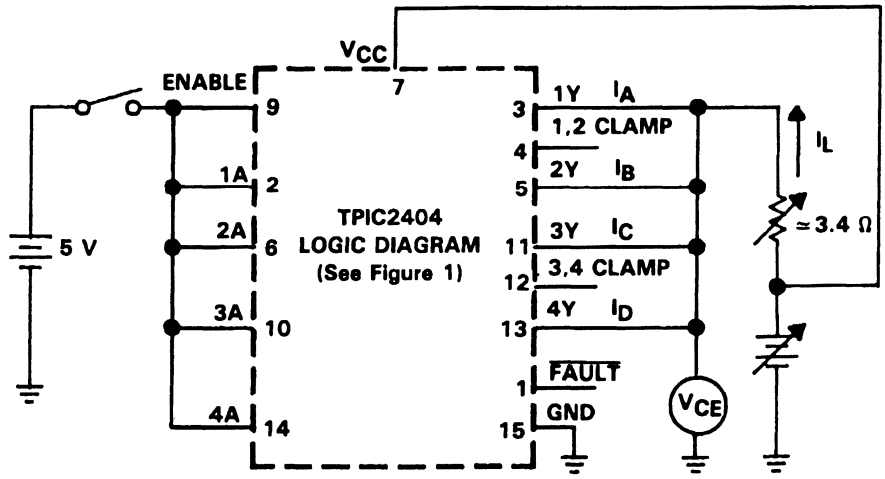


Figure 4. TPIC2404 Mounted on 1/16 Thick Aluminum Heat Sink

Table 2. Typical TPIC2404 Load Current Data, Parallel Switch Operation

HEAT SINK SIZE 1/16 ALUMINUM (In)	TAB TEMPERATURE (°C)	I_L (A)	I_A (A)	I_B (A)	I_C (A)	I_D (A)	V_{CE} (V)	ΔI (A)
8 × 8	29	2.01	0.5	0.5	0.5	0.5	0.25	0.002
8 × 8	31	4.18	1.05	1.07	1.03	1.03	0.59	0.04
5 × 5	34	4.2	1.06	1.04	1.05	1.05	0.59	0.02
3.5 × 3.5	41	4.19	1.07	1.05	1.03	1.04	0.61	0.04
2.5 × 2.5	44	4.25	1.05	1.08	1.06	1.06	0.62	0.03
1.5 × 1.5	58	4.26	1.08	1.06	1.06	1.06	0.67	0.02

Switching Inductive Loads and Voltage Clamps

For switching inductive loads, the TPIC2404 device includes two pairs of integral transient suppression clamp diodes. One diode pair is connected to the open collectors of output switches 1 and 2 and the other diode pair is connected to the open collectors of output switches 3 and 4 as seen in Figure 1.

The absolute maximum voltage rating of the TPIC2404's output switches is 45 V; therefore, the clamp diodes should never be connected to a zener diode or power supply voltage that exceeds 45 V. See Figure 5 for details.

With the transient suppressor clamp diodes disconnected, the TPIC2404's typical unclamped inductive energy is measured as 2.8 mJ using equation (4).

$$L = \frac{L \times I^2}{2} = 2.8 \text{ mJ} \quad (4)$$

This high unclamped inductive energy capability of the TPIC2404 should protect it from reverse secondary breakdown during the transient turn-on interval of even the slowest voltage clamp circuits.

Power Drive Options for Switching High-Power Bipolar and MOSFET Devices

In addition to the direct drive of topside loads, the TPIC2404 is recommended for driving power bipolar and MOSFET transistors switching large ground-side loads. Bipolar devices switching a large current require a large base drive current for saturated switching. Also, power MOSFET devices require a high peak gate drive current to charge/discharge gate capacitance even though their quiescent gate current during the on state is minimal.

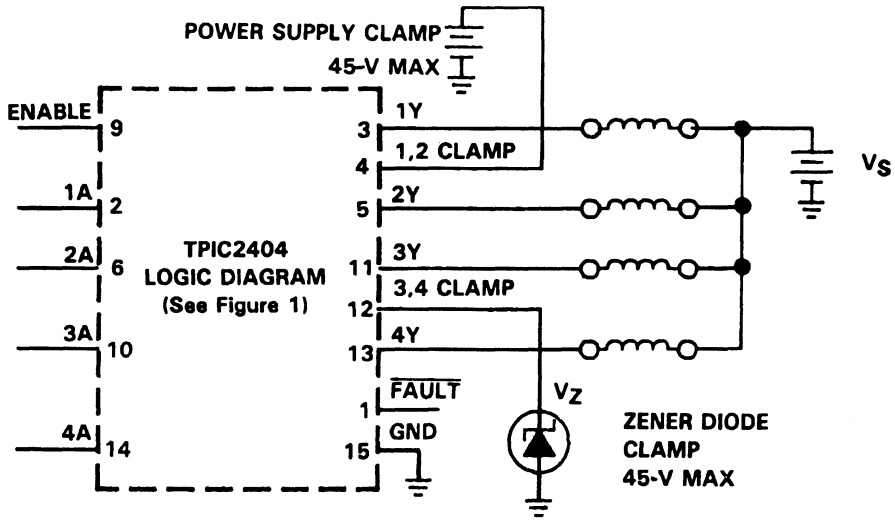


Figure 5. TPIC2404 Circuit for Switching Inductive Loads

Example 2. Determining Bias Conditions for Power Bipolar Q1

The circuit used to determine bias conditions for power bipolar Q1 can be seen in Figure 6.

Operating Conditions/Design Parameters

V_S = 15.3 V
R_L = 1.5 Ω
I_O = 10 A
Duty cycle = d = 0.8
$h_{FE(Q1)}$ = 10 min (TIP36)
$V_{BE(on)(Q1)}$ = 2 V Max (TIP36)
$V_{BE(off)(Q1)}$ = 0.1 V
V_{OL} = 1.3 V (TPIC2404's on voltage at 1 A)
$I_{O(off)}$ = 2 mA Max (TPIC2404)

Next, the bias conditions for the power bipolar Q1 are determined using equations (5) through (9).

$$I_B = \frac{I_O}{h_{FE(Q1)}} = \frac{10\text{ A}}{10} = 1\text{ A} \tag{5}$$

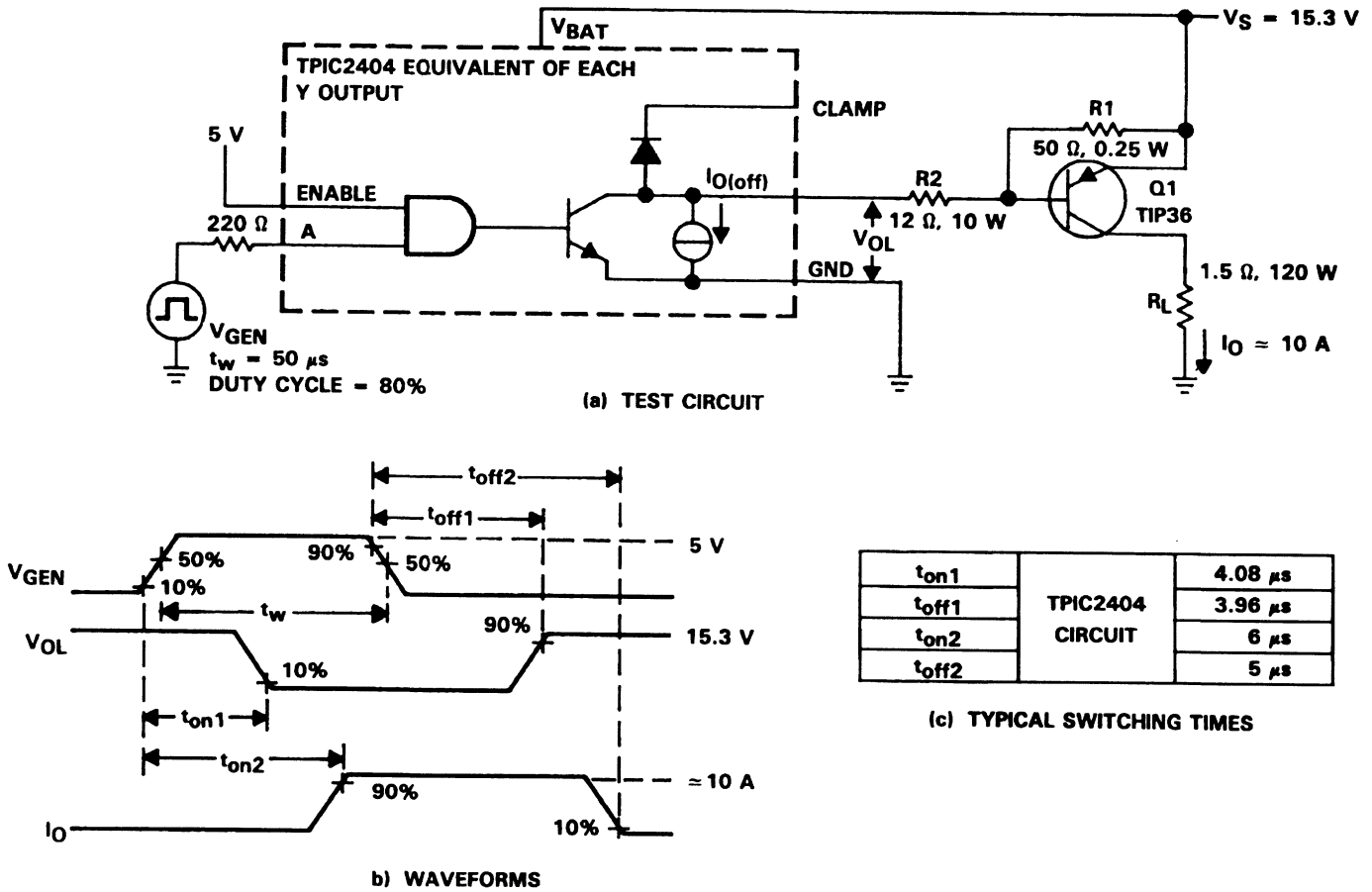
$$R2 = \frac{V_S - |V_{BE(on)(Q1)} + V_{OL}|}{I_B} \tag{6}$$

$$= \frac{15.3\text{ V} - |2\text{ V} + 1.3\text{ V}|}{1\text{ A}} = 12\ \Omega$$

$$R1 = \frac{V_{BE(off)(Q1)}}{I_{O(off)}} = \frac{0.1\text{ V}}{0.002\text{ A}} = 50\ \Omega \tag{7}$$

$$P_{(R1)} = \frac{V_{BE}^2}{R1} \times d = \frac{2\text{ V}^2}{50\ \Omega} \times 0.8 = 0.064\text{ W} \tag{8}$$

$$P_{(R2)} = I_B^2 \times R2 \times d = 1\text{ A}^2 \times 12\ \Omega \times 0.8 = 9.6\text{ W} \tag{9}$$



t_{on1}	TPIC2404 CIRCUIT	4.08 µs
t_{off1}		3.96 µs
t_{on2}		6 µs
t_{off2}		5 µs

(c) TYPICAL SWITCHING TIMES

Figure 6. TPIC2404 Circuit for Determining Bias Conditions for Power Bipolar Q1

Example 3. Determining Bias Conditions for Power MOSFET Q2

The circuit used to determine bias conditions for power MOSFET Q2 can be seen in Figure 7.

Operating Conditions/Design Parameters

V_S = 14.3 V
RO = 3.8 Ω
I_O = 3 A
Duty Cycle = d = 0.8
$I_{GM(Q2)}$ = 1 A (peak gate current Q2)
$I_{O(off)}$ = 2 mA Max (TPIC2404)
$V_{GS(off)(Q2)}$ = 0.6 V Min
V_{OL} = 1.3 V (TPIC2404 on voltage at 1 A)

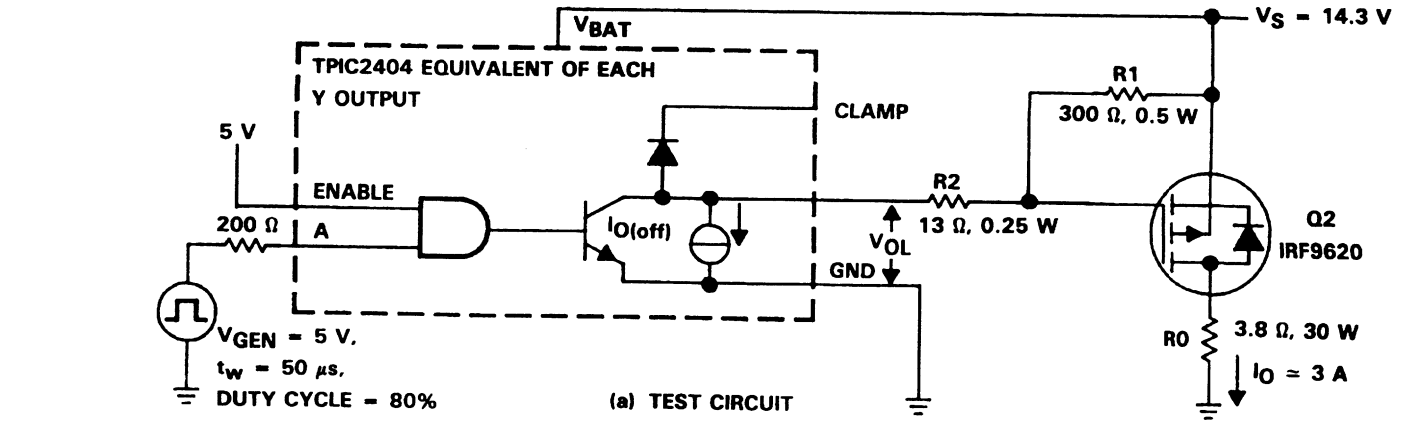
Next, the bias conditions for the power MOSFET Q2 are determined using equations (10) through (13).

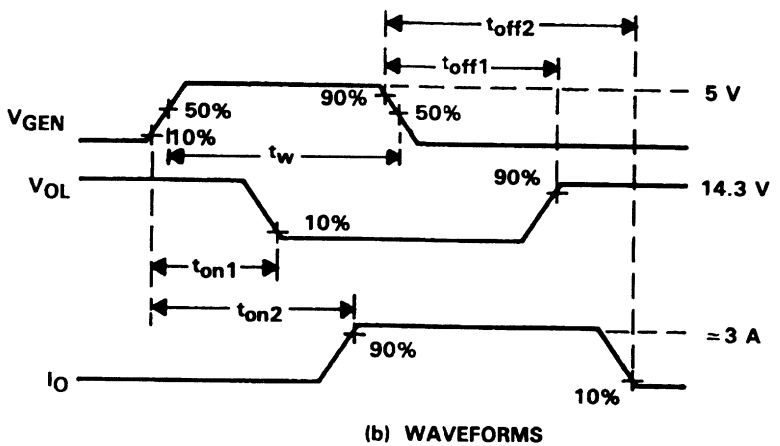
$$R2 = \frac{V_S - V_{OL}}{I_{GM(Q2)}} = \frac{14.3\ V - 1.3\ V}{1A} = 13\ \Omega \tag{10}$$

$$R1 = \frac{V_{GS(off)(Q2)}}{I_{O(off)}} = \frac{0.6\ V}{0.002\ A} = 300\ \Omega\ \text{Max} \tag{11}$$

$$P_{(R1)} = \frac{V_S - V_{OL}}{R1 + R2}^2 \times R1 \times d = 0.414\ W \tag{12}$$

$$P_{(R2)} = \frac{V_S - V_{OL}}{R1 + R2}^2 \times R2 \times d = 0.0179\ W \tag{13}$$





t_{on1}	TPIC2404 CIRCUIT	4.08 μs
t_{off1}		3.96 μs
t_{on2}		4.5 μs
t_{off2}		4 μs

(c) TYPICAL SWITCHING TIMES

Figure 7. TPIC2404 Circuit for Determining Bias Conditions for Power MOSFET Q2

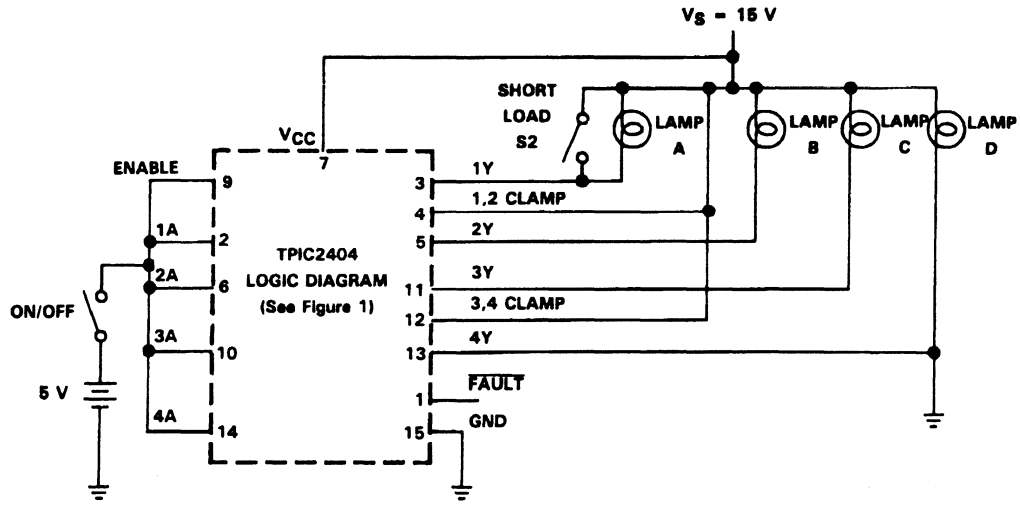
Application Design Examples

Directly Driven Automobile Dome Lamps Simultaneous Operation of Four Lamps

Figure 8 shows the test circuit and oscilloscope waveforms of the TPIC2404 switching four 15-W automobile dome lamps from a 15-V source.

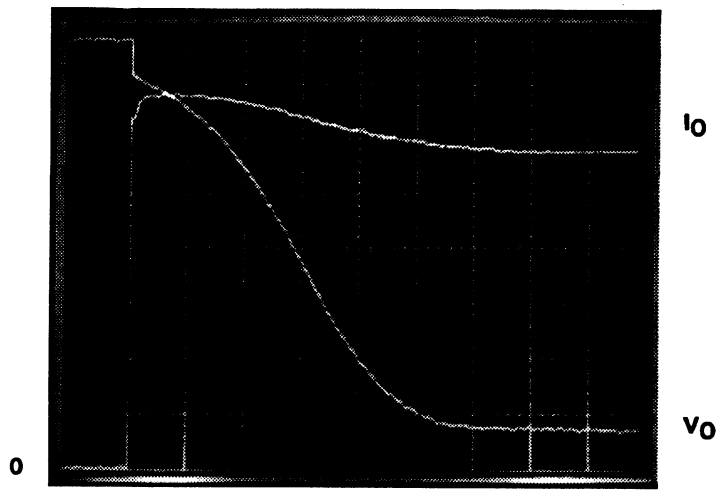
The turn-on waveform shows the bulb's initial cold filament resistance allows the current to be in excess of 1.3 A for approximately 100 ms, during which time the TPIC2404 operates in an overcurrent mode.

If any of the bulbs shown in the circuit are shorted and no external shutdown is employed, the switch with the shorted load will change to a current-limit mode. In this mode, the current is limited below 1.5 A maximum and will sustain the 15-V supply voltage (22.5 W) for a period of approximately 25 seconds (25 s was measured for a tab temperature of 109 °C) until its independent thermal shutdown turns it off. If the load remains shorted, a thermal equilibrium condition will be reached with the shorted switch cycling on and off (a 0.7-ms on time and 1-ms off time was measured for a tab temperature of 109 °C). The other 3 switches with the nonshorted loads will continue normal operation without any load interruption, completely independent of the shorted switch.



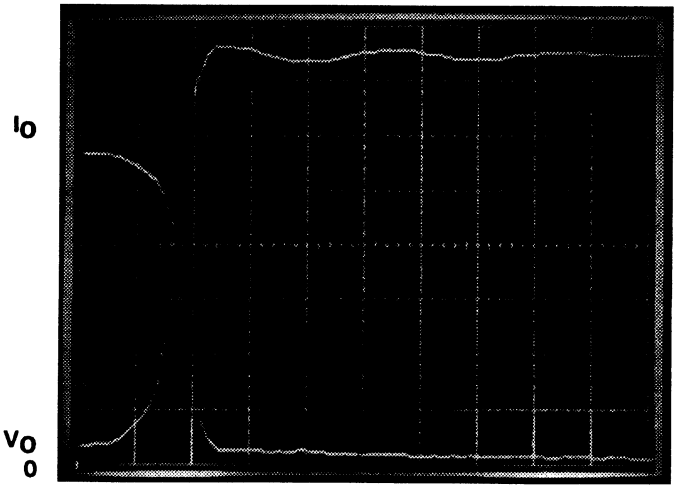
(a) TEST CIRCUIT

Figure 8. Directly Driven Automobile Dome Lamp



HORIZONTAL: 50 ms/cm

(b) TURN-ON WAVEFORM



HORIZONTAL: 0.5 μs/cm

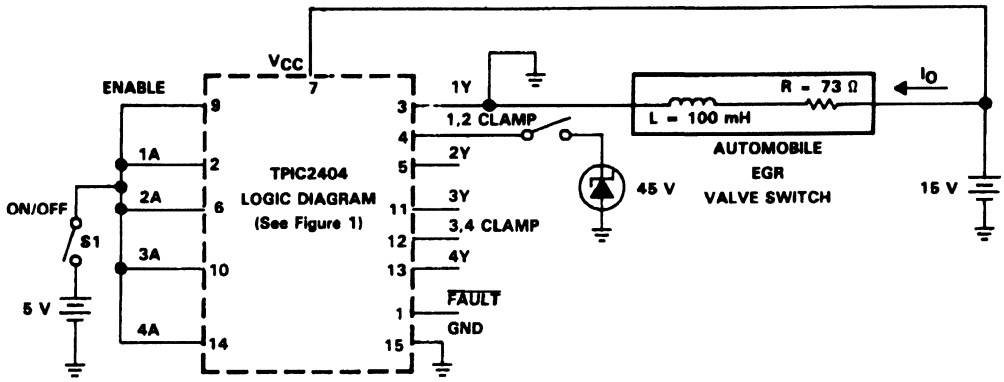
(c) TURN-OFF WAVEFORM

I_O = 200 mA/cm
V_O = 2 V/cm

Figure 8. Directly Driven Automobile Dome Lamp (Continued)

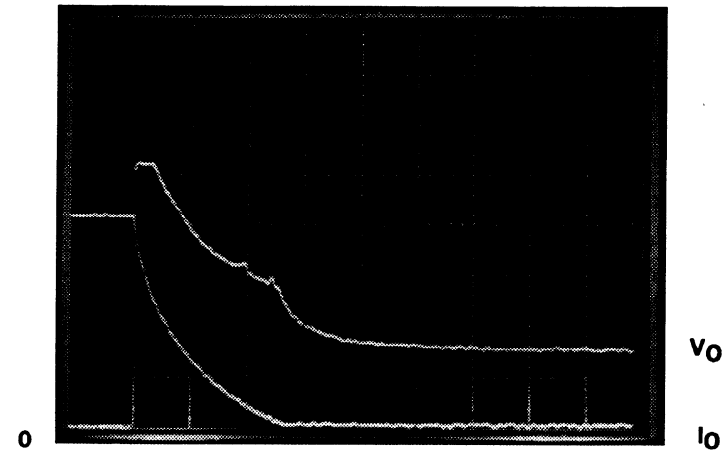
Directly Driven Automobile EGR Solenoid

Figure 9 shows the test circuit and oscilloscope waveforms of the TPIC2404 switching an automobile EGR (Emission Gas Return) solenoid (R = 73 Ω, L = 100 mH, nonenergized) from a 15-V source. To illustrate the avalanche energy capability of the TPIC2404, the 45-V zener clamp is disconnected and the TPIC2404 is forced to dissipate all of the solenoid's inductive energy, approximately 2.1 mJ [See Figure 9(c)]. However, a clamp circuit should always be used when switching inductive loads since this unclamped switching is performed only for a demonstration of the TPIC2404's reliability.



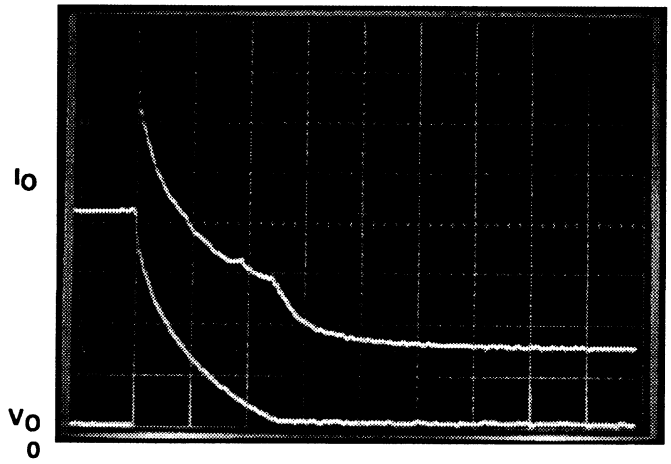
(a) TEST CIRCUIT

Figure 9. Directly Driven Automobile EGR Solenoid



HORIZONTAL: 500 μs/cm

(b) CLAMPED SWITCHING WAVEFORM



HORIZONTAL: 500 μs/cm

(c) UNCLAMPED SWITCHING WAVEFORM

I_O = 50 mA/cm
V_O = 10 V/cm

Figure 9. Directly Driven Automobile EGR Solenoid (Continued)

Full H-Bridge Drive Using All N-Channel Power MOSFETs Controlling Automobile Window Lift Motor

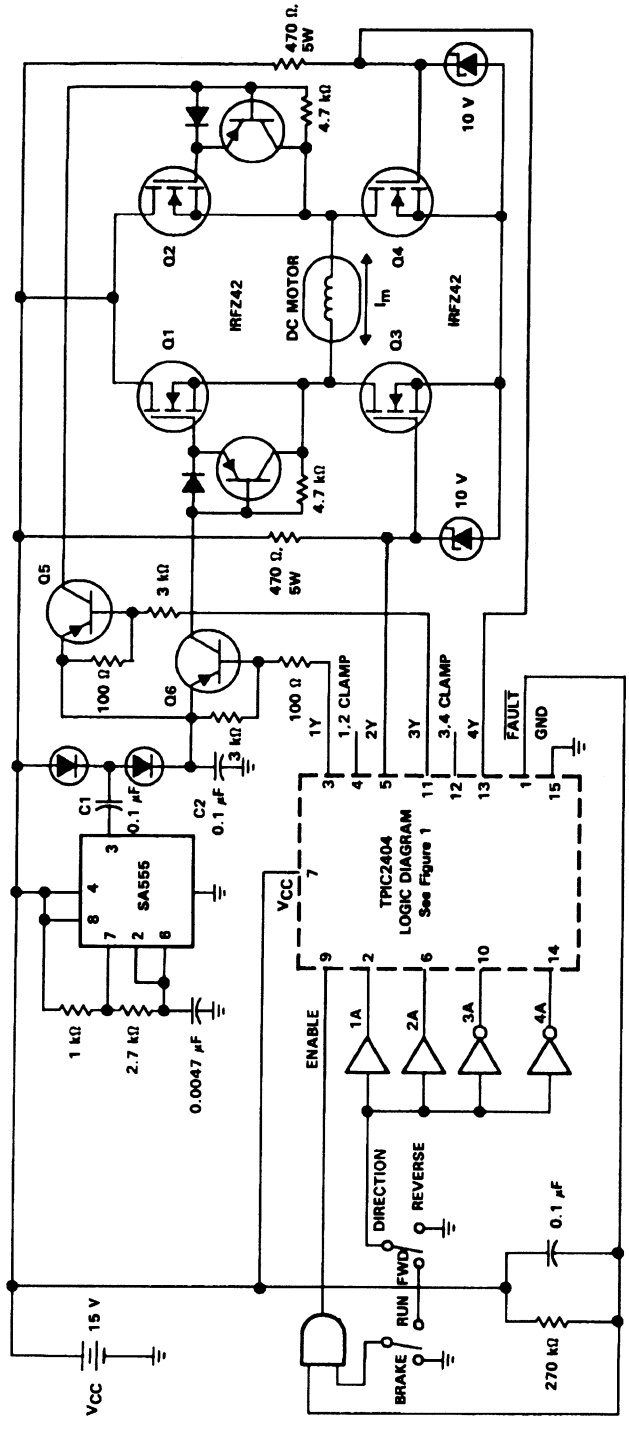
Figure 10 is a reversible dc motor control circuit featuring the TPIC2404 driving four N-channel power MOSFET transistors that control an automobile window lift motor (United Technologies 2.5-in PM High-Torque Motor 1875422M025WM12V). Figure 10(b) is an oscilloscope waveform of a 25-A peak motor current. The peak current occurs for a duration of approximately 20 ms after motor direction is reversed while the motor is running.

Since an N-channel power MOSFET has approximately 1/3 the rds(on) of an equivalent area P-channel power MOSFET, an all N-channel design is used. However, to turn on the top MOSFET devices of the bridge circuit, a gate drive voltage approximately 10 V higher than the 15-V supply voltage is required.

To generate the necessary 25-V gate drive, a charge pump containing a SA555 circuit programmed for 50 kHz/50% duty cycle is used. When the output of the SA555 is low, capacitor C1 charges to within a diode drop of the 15-V supply. When the output of the SA555 is high, capacitor C2 charges to the sum of capacitor C1 voltage plus the SA555 output voltage, less the diode drop of D2.

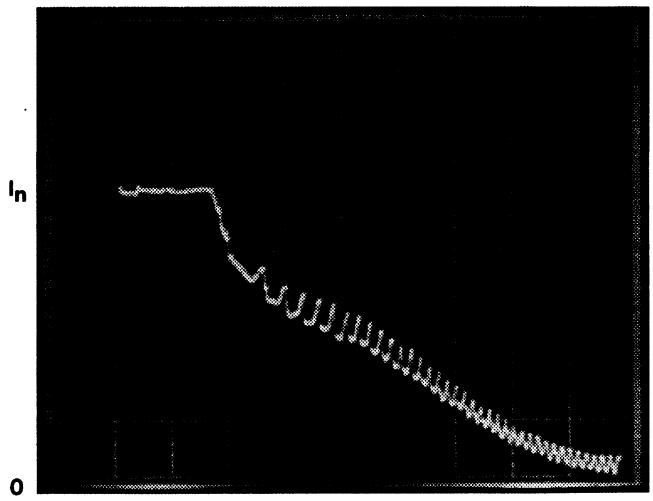
PNP transistors Q5 and Q6 provide a low resistance discharge path for the gate charge of power MOSFETs Q1 and Q2, thereby ensuring fast turn off.

The motor is braked by turning off the two top MOSFETs, Q1 and Q2, and turning on the two bottom MOSFETs, Q3 and Q4. Brake logic is implemented by simply turning off all four of the TPIC2404 outputs by setting the TPIC2404's ENABLE low.



(a) TEST CIRCUIT

Figure 10. Full H-Bridge dc Motor Controller



VERTICAL = 5 A/DIV
HORIZONTAL = 10 ns/DIV
V_S = 15 V

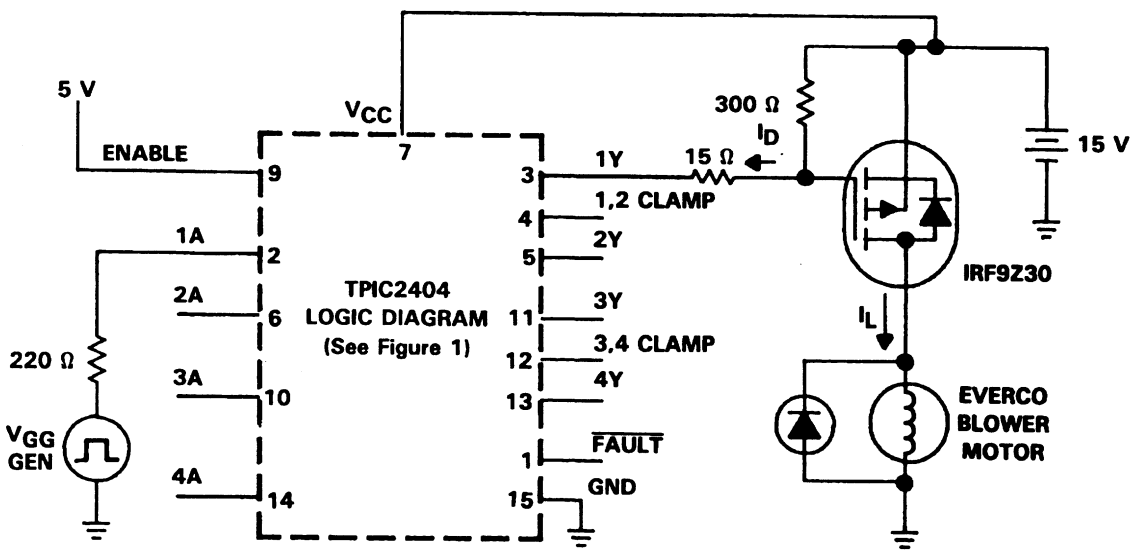
(b) PEAK MOTOR CURRENT WAVEFORM

Figure 10. Full H-Bridge dc Motor Controller (Continued)

PWM Speed Control Automobile Heater/AC Motor with TPIC2404 Driving P-Channel Power MOSFET

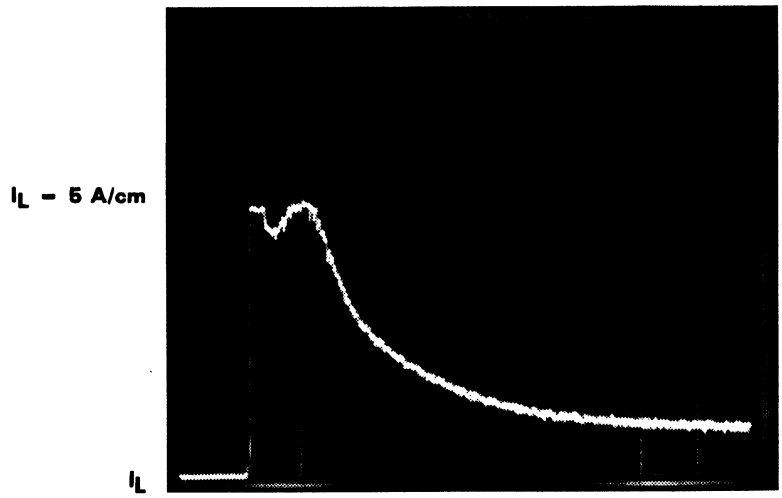
Figure 11 is a circuit featuring the TPIC2404 driving a P-channel power MOSFET transistor that is controlling an automobile airconditioning/heater blower motor e.g., (Everco Heavy Duty 900339 BLOWERMOTOR). The pulse generator, V_{GG}, operating at 5 V and a frequency of 20 kHz, provides input control to the TPIC2404 and simulates a microprocessor controller. The blower fan creates motor loading.

Figure 11(b) shows the motor start current as approximately 25-A peak and the average run current as approximately 4 A. Figure 11(c) shows the IRF9Z30 P-channel power MOSFET peak gate drive current as approximately 500 mA.



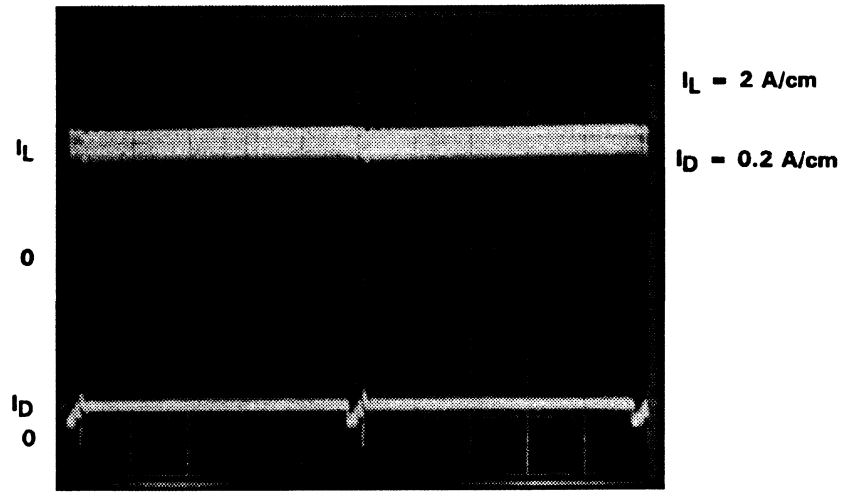
(a) TEST CIRCUIT

Figure 11. PWM Motor Speed Controller



HORIZONTAL: 50 ms/cm

(b) START-CURRENT WAVEFORM



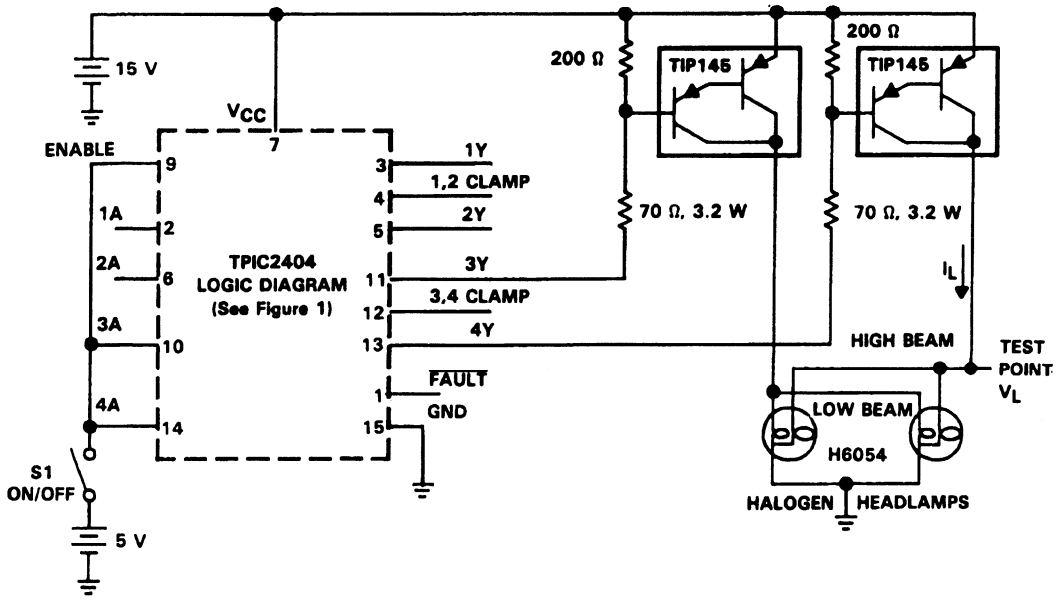
HORIZONTAL: 10 μs/cm

(c) RUN-CURRENT WAVEFORM

Figure 11. PWM Motor Speed Controller (Continued)

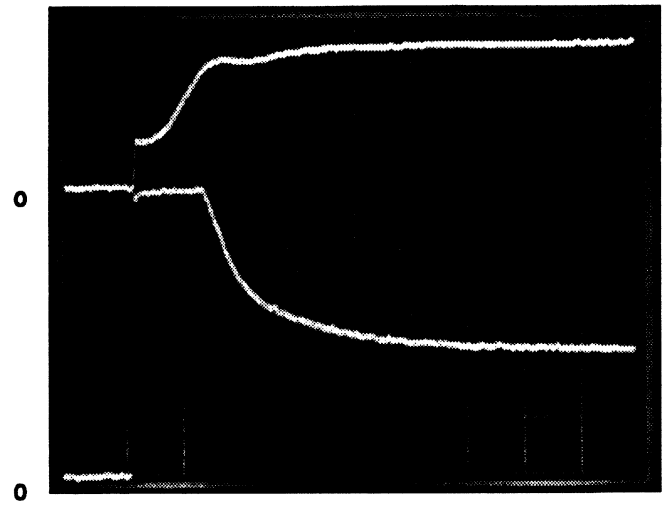
Drive for PNP Darlington Power Transistors Switching Automobile Headlamps

Figure 12 shows the test circuit and oscilloscope waveforms of the TPIC2404 driving a pair of TIP145 PNP power Darlington transistors that are topside switching a set of automobile high/low beam halogen headlamps (H6054 HALOGEN HEADLAMPS).



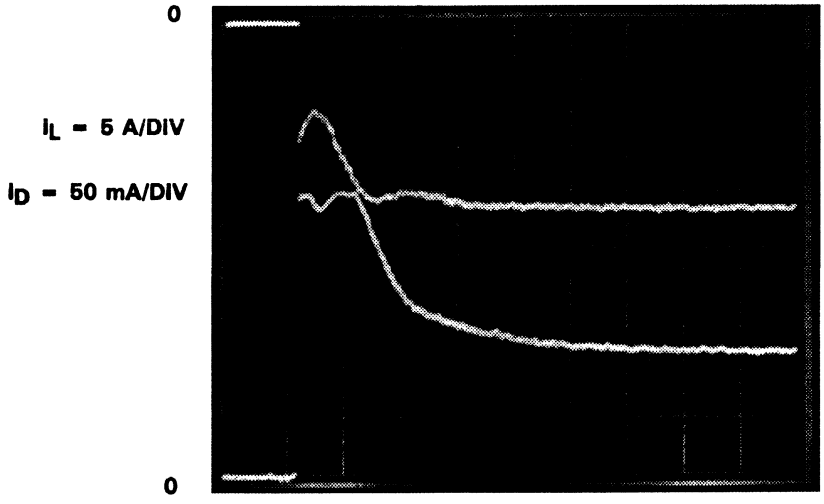
(a) TEST CIRCUIT

Figure 12. Automobile Headlamp Switching



HORIZONTAL: 50 ms/DIV

(b) LOAD CURRENT AND VOLTAGE WAVEFORM



HORIZONTAL: 50 μs/DIV

(c) DRIVE CURRENT AND LOAD CURRENT WAVEFORMS

Figure 12. Automobile Headlamp Switching (Continued)

Stepper Motor Drive

Figure 13 is a unipolar stepper motor circuit featuring the TPIC2404 providing up to 1-A direct drive to each of the motor's four windings. Input logic for the TPIC2404 is provided by a microprocessor controller.

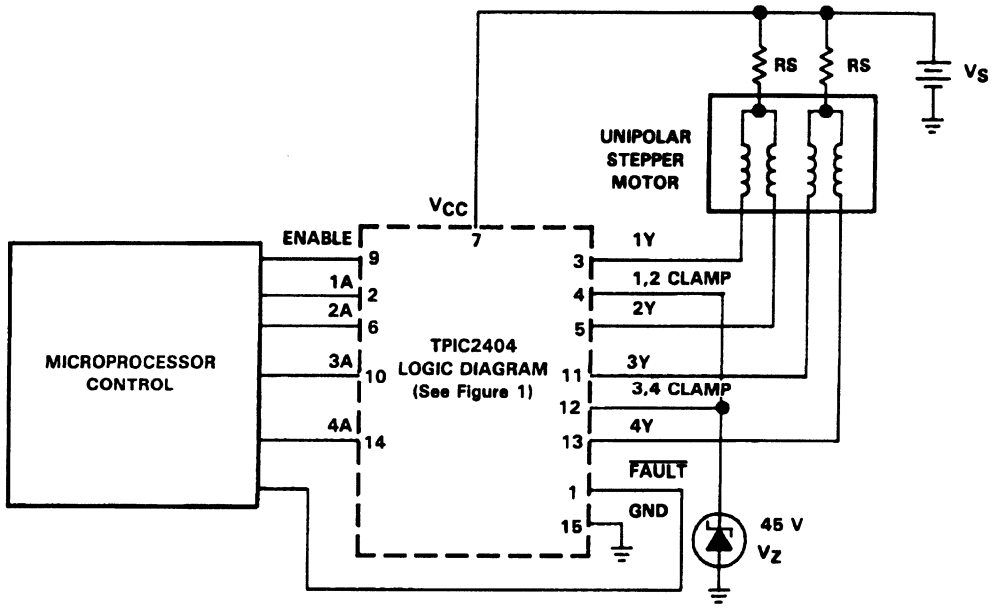


Figure 13. Stepper Motor Drive

Summary

The self-protection capability of the TPIC2404 is illustrated by the design example shown in Figure 8, "Directly Driven Automobile Dome Lamps Simultaneous Operation of Four Lamps", where one of the four lamp loads is shorted while the other lamp loads operate without interruption, completely independent of the one output switch connected to the shorted load.

Also, the capability to extend the TPIC2404 output switch 1-A load current by parallel switch operation is illustrated by the measurement data shown in Table 2, "Typical TPIC2404 Load Current Data, Parallel Switch Operation", where data showing up to a 4-A load is switched by four parallel connected output switches.

To demonstrate usage of the TPIC2404 as an effective driver for MOSFET and Bipolar High Power Switches (both technologies require high drive current for efficient, high-speed switching) application circuits are included as follows: Figure 10, "Full H-Bridge dc Motor Control", Figure 11, "PWM Motor Speed Controller", and Figure 12, "Automobile Headlamp Switching".

The excellent Safe Operating Area (SOA) of the TPIC2404's switches combined with its functions of thermal shutdown, overvoltage protection, overcurrent limit, and fault diagnostic makes the TPIC2404 an extremely reliable device well suited to driving loads requiring up to a few amperes of current in extremely harsh environments such as an automobile.

TPIC2406 Intelligent-Power Quadruple MOSFET Latch

TEXAS INSTRUMENTS

Contents

List of Illustrations

Introduction

The TPIC2406 is a monolithic, high-voltage, high-current, quadruple power driver. It is packaged in a 20-pin NE package designed for heat sinking and recommended for use in systems that require high load power. The device contains built-in, high-speed, output-clamp diodes for inductive transient protection. Applications include driving relays, solenoids, lamps, and dc stepping motors.

Functional Description

The TPIC2406 features four inverting open-drain outputs, each controlled by an input storage latch with common clear and enable controls, which is shown in Figure 1. All inputs accept standard TTL- and CMOS-logic levels.

The function table for each channe is seen in Table 1. The $\overline{CLR}$ function is asynchronous and turns all four outputs off regardless of data inputs. Taking $\overline{ENBL}$ low puts the input latch into a transparent mode, allowing the data inputs to affect the output. In this state, all four outputs are held off while $\overline{CLR}$ is low but will return to the stages on the data inputs when $\overline{CLR}$ goes high. When $\overline{ENBL}$ is taken high, the latch is put into a storage mode, and the last state of the data inputs is held in the latches. If the $\overline{CLR}$ input is taken low, the data in the latches is cleared, turning all outputs off. If $\overline{CLR}$ is taken high again, $\overline{ENBL}$ must be cycled low to read new data into the latch.

Table 1. Function Table (Each Channel)

FUNCTION	INPUTS			OUTPUT	FAULT
	$\overline{ENBL}$	$\overline{CLR}$	IN	Y	$\overline{F}$
Normal Operation	X	L	X	H	H
	L	H	L	H	H
	L	H	H	L	H
	H	H	X	Q_0	H
Thermal Shutdown	X	X	X	H	L

H = high-level, L = low-level, X = irrelevant

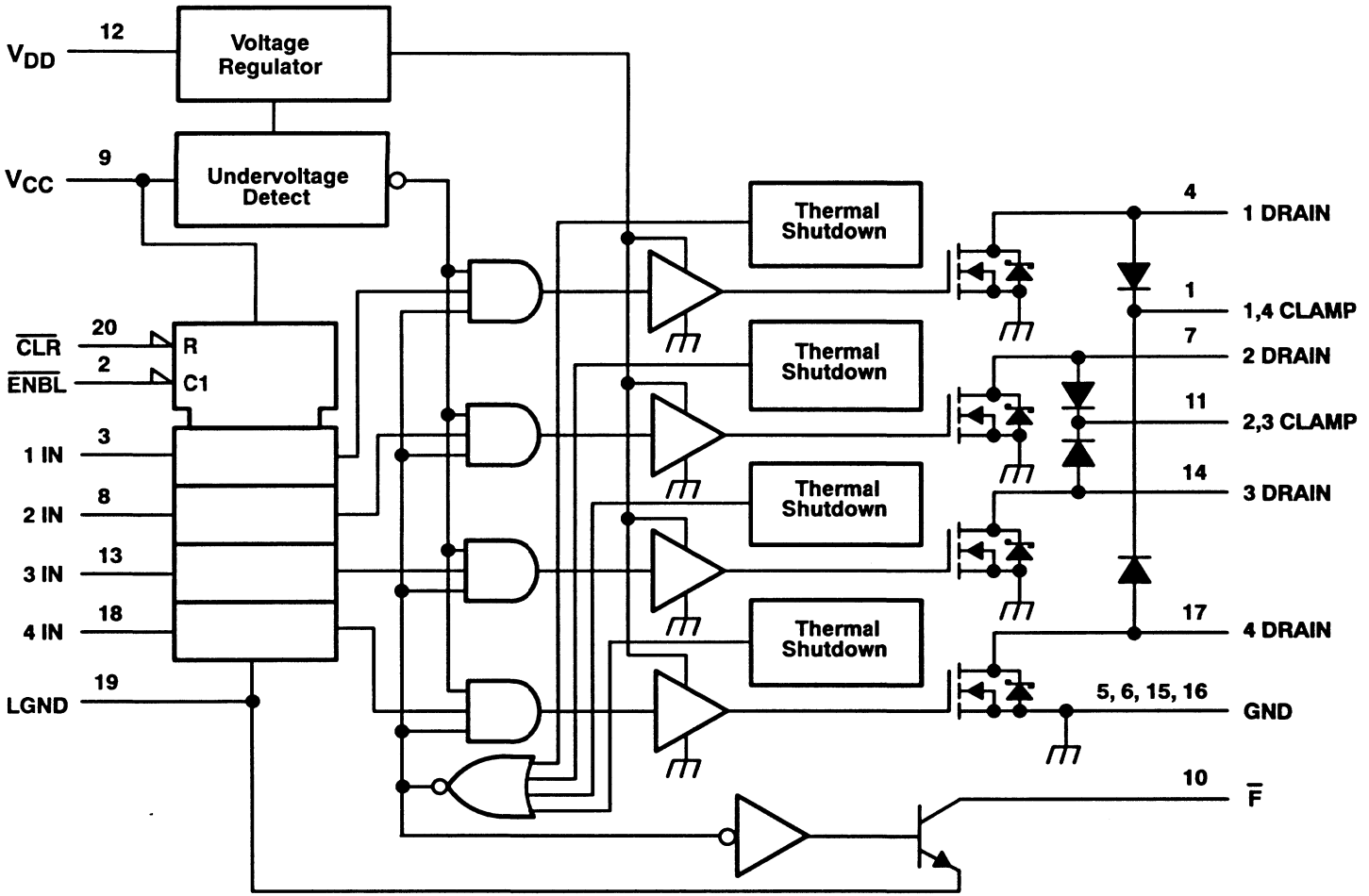


Figure 1. Logic Diagram

Application Design Considerations

Three important application considerations for a power device are the power, thermal, and inductive energy ratings with respect to the operational load demands. This includes the associated possible requirements for a heat sink and a voltage clamp. The following application design examples illustrate analytical approaches that ensure the device is operating with these maximum ratings.

Power and Thermal Considerations

Example 1 illustrates how the current capability of a single device output can be determined with n outputs simultaneously conducting. Example 2 illustrates how device current capability can be increased by reducing $R_{\theta JA}$, thereby creating a cost-effective thermal design.

Example 1. Using transient thermal impedance to determine the maximum current of a single output with n outputs simultaneously conducting

To calculate the current drain current (I_D) for a single output with n outputs conducting equal current, use equation 1.

$$I_D = \sqrt{\frac{T_J - T_A}{Z_{\theta JA} \times r_{DS(on)} \times 4}} \times K_n \qquad (1)$$

Where:

K_n	=	Current coefficient for the current of a single output with n outputs simultaneously conducting equal current	See Table 2
$Z_{\theta JA}$	=	Transient thermal impedance	See Figure 3
$r_{DS(on)}$	=	Static drain-source on-state resistance at 150°C (worst case)	1.05 Ω
T_J	=	Junction temperature (worst case)	150°C
T_A	=	Ambient temperature	
4	=	Maximum number of outputs conducting equal current	

Table 2. Values for the Current Coefficient K_n

Total Outputs On n	Current Coefficient K_n
4	1
3	1.123
2	1.309
1	1.630

The current coefficient values, K_n, shown in Table 2 are derived from the thermal model shown in Figure 2 and the data sheet thermal resistance values.

To calculate the current coefficient values in Table 2, use the model in Figure 2.

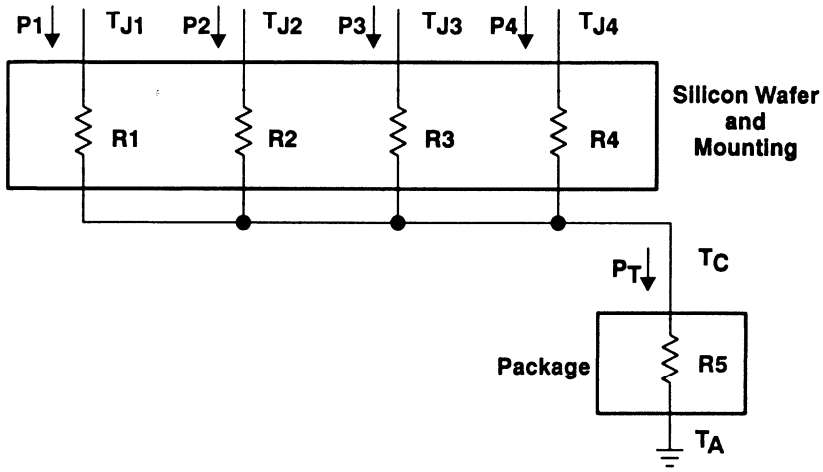


Figure 2. Thermal Model – Thermal Equilibrium, No Heat Sink

Where the following equations apply for the thermal model in Figure 2:

R1 || R2 || R3 || R4 + R5 = 50°C/W
R1 || R2 || R3 || R4 = 8.33°C/W
R1 = R2 = R3 = R4 = 33.32°C/W
R5 = 41.67°C/W
$T_{J1(n)}$ = Junction temperature of an individual output with n outputs conducting equal current
P1 = P2 = P3 = P4

Therefore:

$$T_{J1(n)} = P1R1 + nP1R5 + T_A$$

From the thermal model in Figure 2, P1 can be calculated using equation 3.

$$P_1 = \frac{T_{J1(n)} - T_A}{R1 + nR5} = I_D{}^2 r_{DS(on)} = I_D{}^2 1.05\ \Omega$$

Therefore, the current $I_{D(n)}$ is:

$$I_{D(n)} = \sqrt{\frac{T_{J1(n)} - T_A}{r_{DS(on)}(R1 + nR5)}} = \sqrt{\frac{K_n}{(R1 + nR5)}}$$

Using equation 4, the drain current for one to four outputs can be calculated as seen in equations 5 – 8.

For one output conducting:

$$I_{D(1)} = \sqrt{\frac{K_1}{33.32 + 1 \times 41.67}} = 0.115\sqrt{K_1}$$

Two outputs conducting:

$$I_{D(2)} = \sqrt{\frac{K_2}{33.32 + 2 \times 41.67}} = 0.092\sqrt{K_2}$$

Three outputs conducting:

$$I_{D(3)} = \sqrt{\frac{K_3}{33.32 + 3 \times 41.67}} = 0.0793\sqrt{K_3}$$

Four outputs conducting: (existing conditions in Figure 2)

$$I_{D(4)} = \sqrt{\frac{K_4}{33.32 + 4 \times 41.67}} = 0.0706\sqrt{K_4}$$

Once the drain current is calculated in terms of K_n, then K_n is obtained by normalizing 0.115, 0.092, 0.0793, and 0.0706 in reference to 0.0706. The number 0.0706 is the value for four outputs conducting the conditions in Figure 2.

The current coefficient values for one to four outputs conducting are as follows:

$$K_4 = \frac{0.0706}{0.0706} = 1.000$$

$$K_3 = \frac{0.0793}{0.0706} = 1.123$$

$$K_2 = \frac{0.0920}{0.0706} = 1.309$$

$$K_1 = \frac{0.1150}{0.0706} = 1.630$$

The switching requirement of many applications is characterized by either single current pulses of short on time or by pulses of repetitive duration. For many of these applications, the large thermal capacitance of the 20-pin NE package limits the junction temperature to

within the maximum ratings, even in the presence of large current pulses. For these applications, Figure 3 may be used to determine the peak junction temperature.

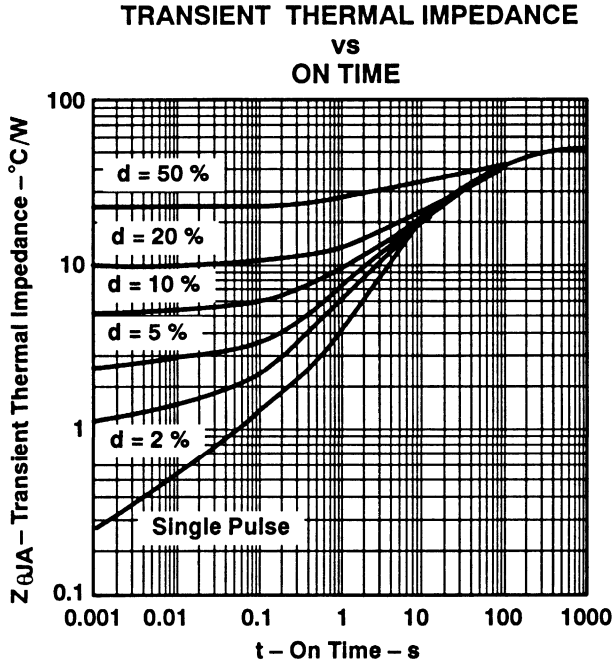


Figure 3. Transient Thermal Impedance vs On Time

The single-pulse curve in Figure 3 represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_{\theta(t_w + t_c)} + Z_{\theta(t_w)} - Z_{\theta(t_c)} \quad (13)$$

Where:

$R_{\theta JA}$ = Junction-to-ambient thermal resistance = 50°C/W
$Z_{\theta(tw)}$ = Single-pulse thermal impedance for $t = t_w$ seconds
$Z_{\theta(tc)}$ = Single-pulse thermal impedance for $t = t_c$ seconds
$Z_{\theta(tw + tc)}$ = Single-pulse thermal impedance for
$t = t_w + t_c$ seconds
$d = t_w/t_c$

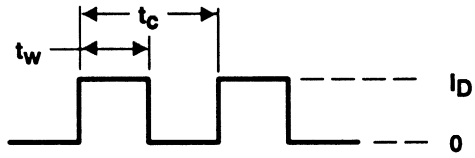


Figure 4 is shown to define the complete thermal impedance by combining the two elements, thermal resistance and thermal capacitance. The first cell in Figure 4 represents the silicon wafer, which has a time constant of approximately 30 ms. The second cell represents the lead frame, which has a time constant of approximately 2 s. The last two cells connected in parallel account for the external heat sink on the circuit board in parallel with the cell corresponding to the package molding compound. The time constant of the molding compound alone is approximately 200 s.

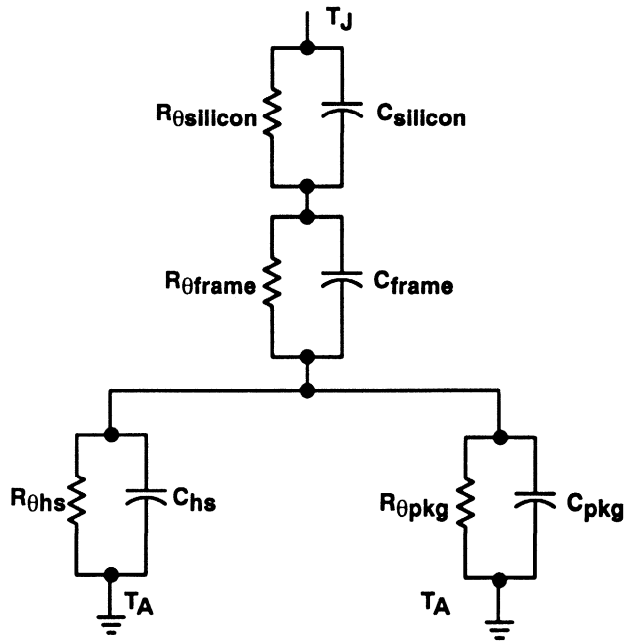


Figure 4. Thermal Circuit Model of a Power NE Package

Example 2. Determining reduced junction-to-free-air thermal resistance for increased device power dissipation using an external heat sink

The $R_{\theta JA}$ can be reduced by soldering ground pins 5, 6, 15, and 16 to a copper area on the printed-circuit-board or to an external heat sink as seen in Figure 5. Figure 6 is a graph of $R_{\theta JA}$ as a function of the size l of two equal copper areas, which can be used to calculate the junction-to-free-air thermal resistance.

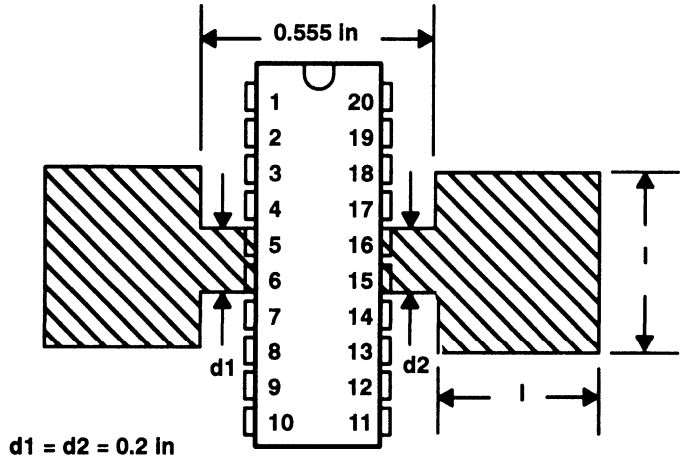


Figure 5. Copper PC Board Used as Heat Sink

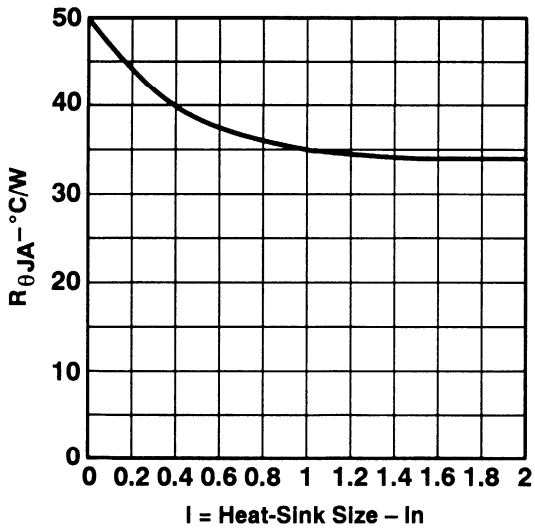


Figure 6. Junction-to-Ambient Thermal Resistance vs Heat-Sink Size

Switching Inductive Loads and Voltage Clamps

Example 3. Determining the maximum energy of an inductive load for choosing an external clamp

The avalanche energy rating of 50 mJ per output switch greatly enhances its value as an inductive load driver. Therefore, for inductive loads equal to or less than 50 mJ, an external voltage clamp may not be required, depending on the device's power dissipation, heat sinking, and operating temperature. If an external clamp is required, two pairs of integral transient suppression clamp diodes are included. One diode pair is connected to the open drains of output MOSFETs 1 and 4, and the other diode pair is connected to the open drains of output MOSFETs 2 and 3 as seen in Figure 1. The absolute maximum voltage rating of the output MOSFETs and clamp diodes is 60 V, which should not be exceeded.

Figure 7 shows the test circuit, output waveforms, and oscilloscope waveforms of the TPIC2406 simultaneously driving four 289-mH inductors at a 48 Hz and a 52% duty-cycle switching condition. The device provides a 0.4-A maximum current to each output switch, which is limited by the 11-ms on time and the 289-mH/15-Ω load.

Each output switch absorbs an inductive energy of 25.7 mJ if no external clamp is used, which makes the device's total power dissipation, P_T, 5.25 W. Therefore, external heat sinking is required, or an external clamp must be used if external heat sinking is not available.

The energy and power calculations are as follows:

$$E_T = E_L + E_S - E_R = \frac{3LI_{DM}^2 V_{CL}}{6(V_{CL} - V_{OP}) + 4R_L I_{DM}} = 25.7\text{mJ} \quad (15)$$

$$P_{off} = E_T \times f = 0.0257\ \text{J} \times 48\ \text{Hz} = 1.23\ \text{W} \quad (16)$$

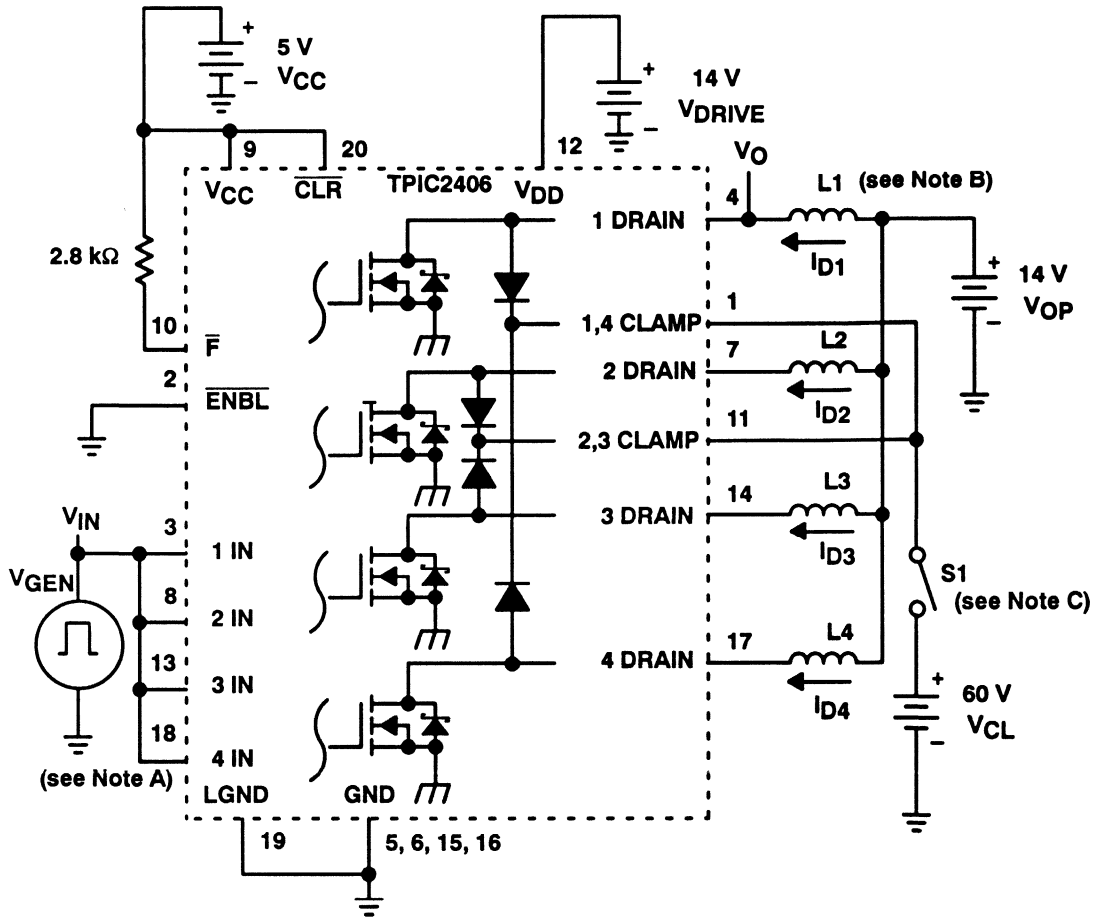
$$P_{on} = I_{DM}^2 \times r_{DS(on)} \times d = 0.4\ \text{A}^2 \times 1\ \Omega \times 0.52 = 0.083\ \text{W} \quad (17)$$

$$P_T = (P_{off} + P_{on}) \times n = (1.23\ \text{W} + 0.083\ \text{W}) \times 4 = 5.25\ \text{W} \quad (18)$$

Where:

L	Load inductance	289 mH
I_{DM}	Peak drain current	0.4 A
V_{CL}	External clamp voltage or $V_{(BR)DSX}$ voltage (typ) if no clamp is used	100 V
V_{OP}	Load supply voltage	14 V
R_L	Resistance of inductor	15 Ω
f	Switching frequency	48 Hz
d	Duty cycle (as ratio)	0.52
$r_{DS(on)}$	Static on-state drain-source resistance (T_J = 125°C)	1 Ω
E_L	Inductive energy stored in inductor	23 mJ

E_S	Energy from power supply during turn-off transient	3.6 mJ
E_R	Energy absorbed by resistance during turn-off transient	1.03 mJ
E_T	Total energy absorbed by each switch during turn-off transient	25.7 mJ
P_{OFF}	Turn-off power dissipation each switch	1.23 W
P_{ON}	On-state power dissipation each switch	0.083 W
n	Total number of switches operating	4
P_T	Total power dissipation	5.25 W



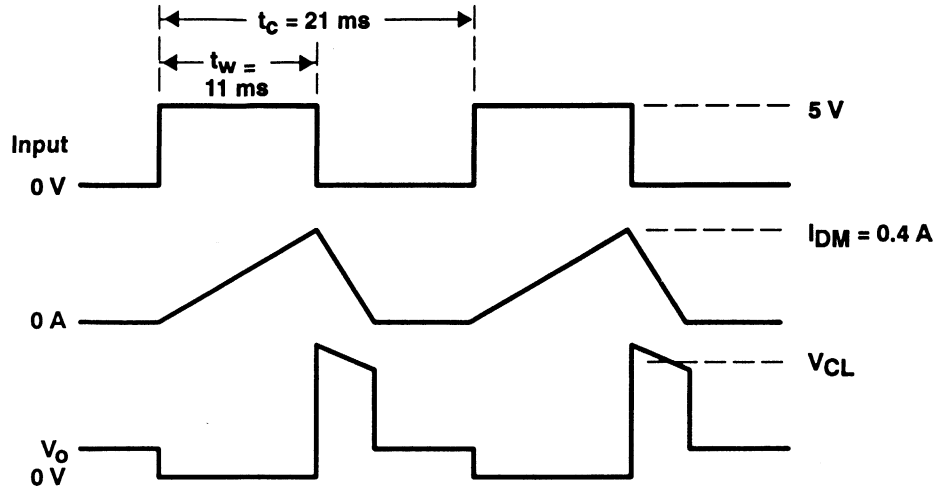
(a) TEST CIRCUIT

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 11$ ms, PRR = 48 Hz, $V_O = 5$ V, $Z_O = 50\ \Omega$. The input pulse duration, t_w, is increased until the peak load current, $I_{DM} = 0.4$ A.

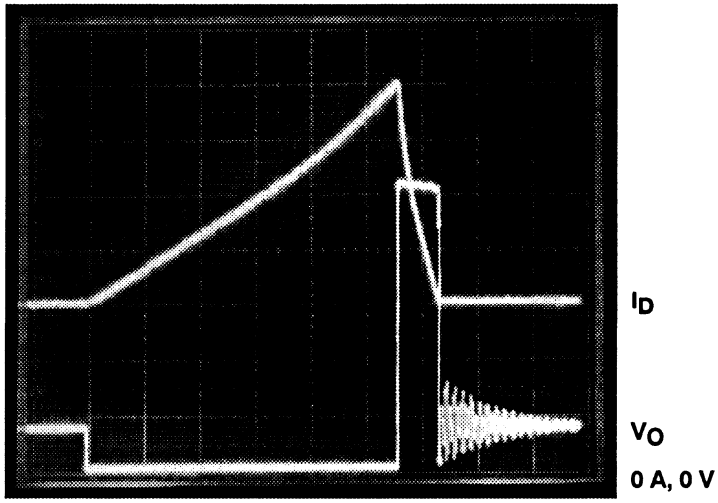
B. Inductors L1 = L2 = L3 = L4 = 289 mH/15 Ω.

C. If the device is operated on a heat sink capable of maintaining case temperature ≤ 107°C, no external voltage clamp is required and S1 remains open. If case temperature can not be maintained ≤ 107°C, an external voltage clamp is required, and S1 must be closed.

Figure 7. Directly Driven 289-mH Inductors



(b) OUTPUT WAVEFORMS FOR SWITCHING INDUCTIVE LOADS



Vertical: I_D = 100 mA/cm
V_O = 20 V/cm
Horizontal: 2 ms/cm

(c) OSCILLOSCOPE WAVEFORMS DRIVING FOUR INDUCTOR LOADS

Figure 7. Directly Driven 289-mH Inductors (continued)

Parallel Operation of Quad Outputs for Extended Output Current Capability

Example 4. Determining maximum load current with multiple device outputs connected in parallel

If all four output switches are not needed for an application and an output load current greater than 0.77 A is required, the switches can be connected in parallel for an extended current capability. To demonstrate current sharing between the switches, it is operated in the configuration shown in Figure 8 at T_A = 25°C using no heat sink. The load currents (I_D) of all four switches are measured at an approximate total load of I_T = 3.2 A. The current difference, ΔI, measured between any combination of switches is typically no greater than 100 mA (see Table 3).

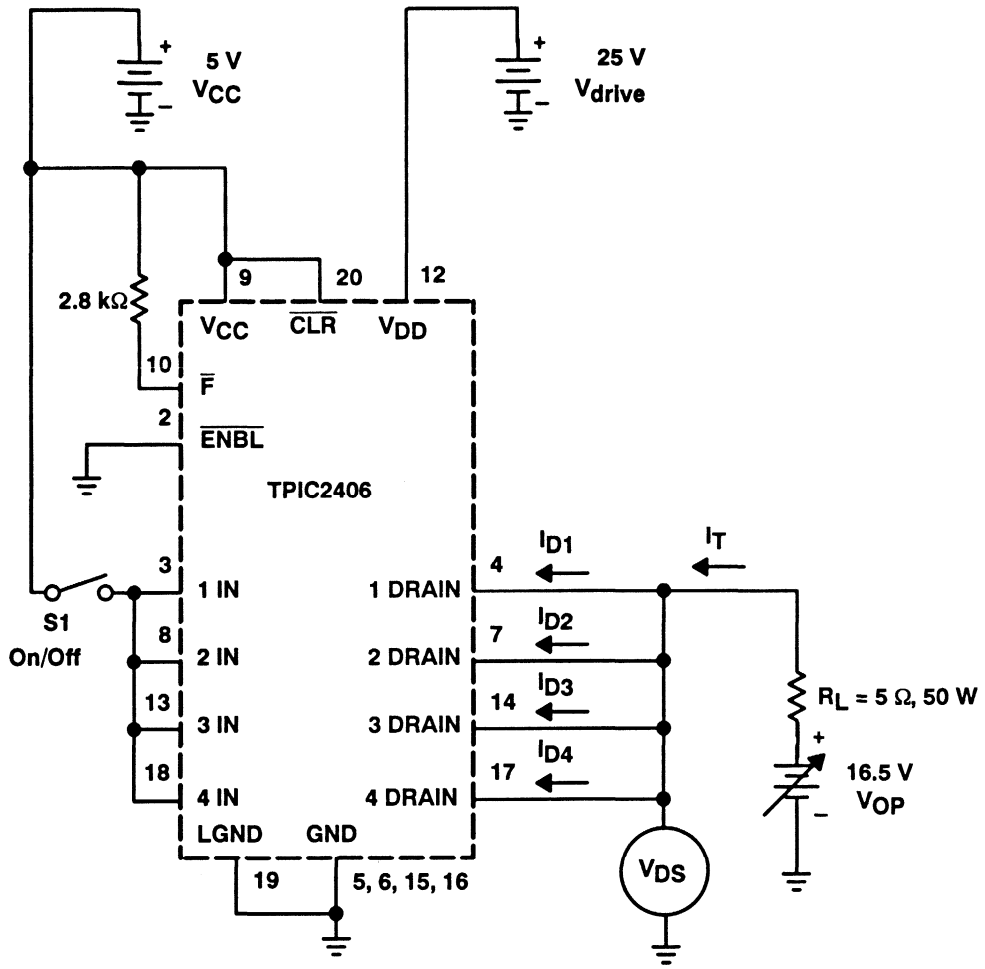


Figure 8. Test Circuit for Parallel Operation of Quad Outputs

Table 3. Typical Load Current Data, Parallel Switch Operation

UNIT NO.	V_{DS} (V)	I_T (A)	I_{D1} (A)	I_{D2} (A)	I_{D3} (A)	I_{D4} (A)	ΔI (A)
1	0.51	3.2	0.75	0.8	0.85	0.8	0.1
2	0.496	3.2	0.75	0.75	0.85	0.85	0.1
3	0.514	3.2	0.75	0.75	0.85	0.85	0.1
4	0.53	3.2	0.75	0.75	0.85	0.85	0.1

Application Design Examples

The TPIC2406 is recommended for driving both resistive and inductive loads, such as lamps and motors. To demonstrate usage of the device driving these loads, two specific application examples are given: (1) directly driving lamps, and (2) directly driving a stepping motor.

Directly Driven Automobile Lamps

To demonstrate the TPIC2406's capability to drive incandescent lamps, the lamp types listed in Table 4 are tested as shown in the Figure 9(a) circuit. In this circuit, the peak cold filament current (I_{DM}) and the continuous current (I_D) are measured.

Table 4. Evaluation of Switching Incandescent Automotive Lamps

Lamp Type	Single Output Lamp Current (A)		t_d (ms)	Case Temperature (°C) Number of Outputs Simultaneously Turned On			
	I_{DM}	I_D		1	2	3	4
194	2.6	0.284	50	25	26	27.5	30
168	3.5	0.345	50	26	28	31	34
631	5.5	0.677	50	35	47	58	70
1003	8.4	1.018	50	50	86	122	†
1004	8.8	0.992	50	49	82	124	†
211-2	8.8	1.032	50	50	82	129	†

† Thermal shutdown

The device is operated and measured with a maximum of all four outputs on, or up to the maximum outputs on not causing thermal shutdown. The case temperature (T_C) is measured for each combination of outputs operating. Also, the peak current decay time, t_d, is measured for the time duration that it takes the peak current, I_{DM}, to decrease to $I_{DM} = 1.2\,I_D$, see Figure 9(b). Figures 9(c) thru 9(h) illustrate the oscilloscope lamp-current turn-on waveforms.

The independent thermal shutdown circuits monitor each output and disable all outputs when the maximum junction temperature is reached, typically 155°C. At this point, fault condition is sensed and reported by the error-sensing circuit. This condition remains

until the junction temperature falls below 140°C (typically), and the thermal shutdown allows all outputs to return to normal operation, see Figure 9(i).

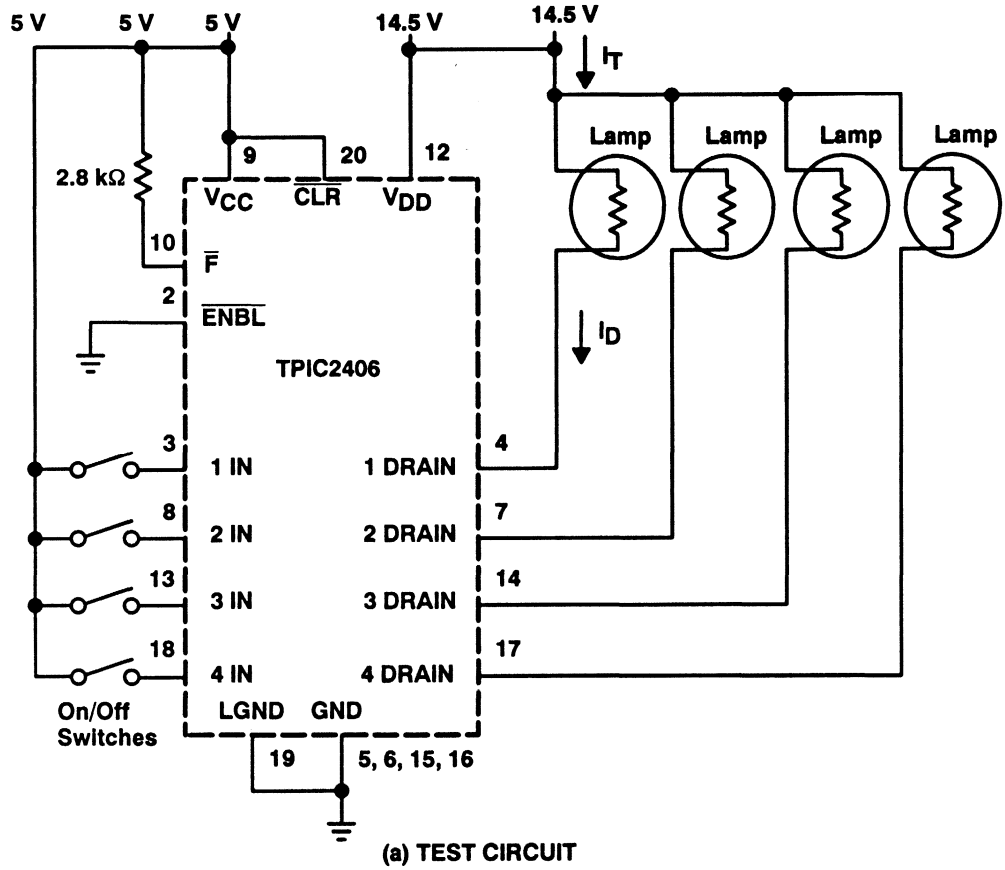
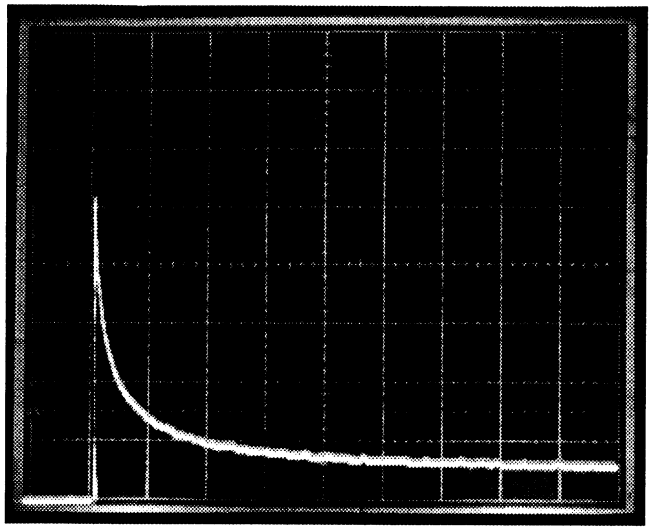
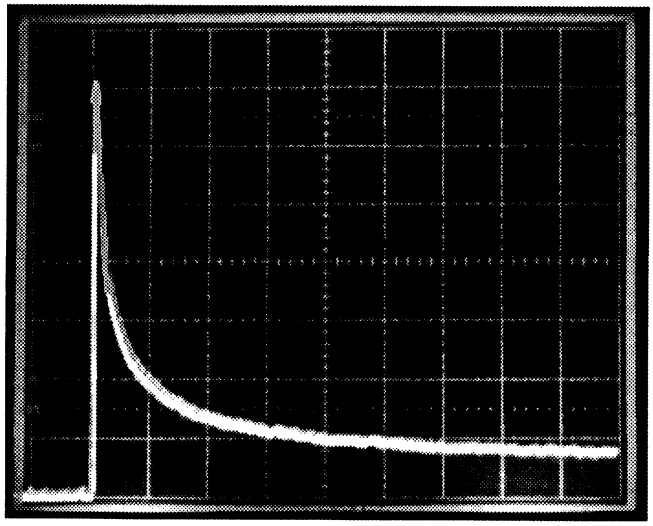


Figure 9. Directly Driven Automobile Incandescent Lamps



Vertical: 0.5 A/cm
Horizontal: 10 ms/cm

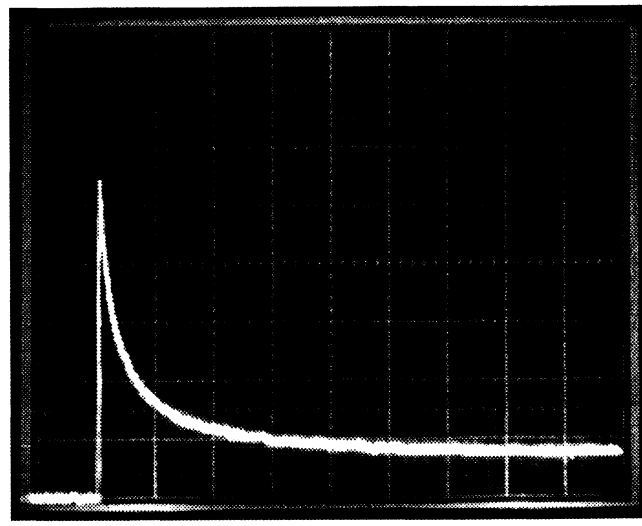
(c) LAMP TYPE 194
LAMP CURRENT TURN-ON WAVEFORM



Vertical: 0.5 A/cm
Horizontal: 10 ms/cm

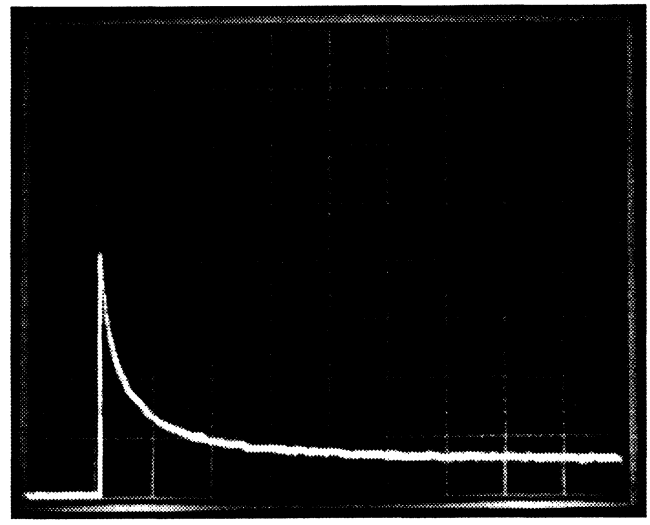
(d) LAMP TYPE 168
LAMP-CURRENT TURN-ON WAVEFORM

Figure 9. Directly Driven Automobile Incandescent Lamps (continued)



Vertical: 1 A/cm
Horizontal: 10 ms/cm

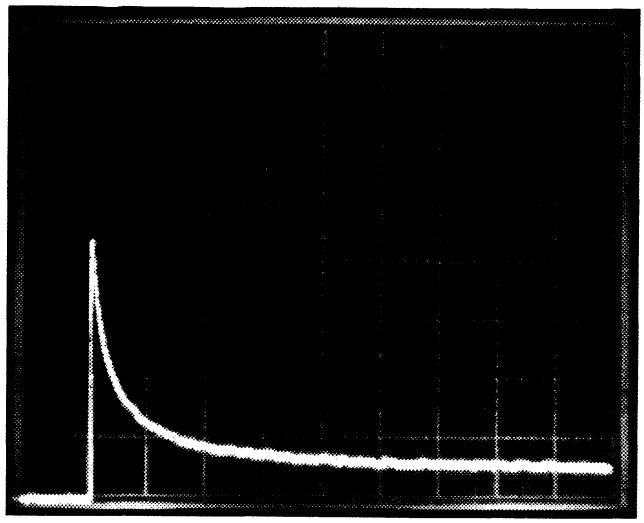
(e) LAMP TYPE 631
LAMP CURRENT TURN-ON WAVEFORM



Vertical: 2 A/cm
Horizontal: 10 ms/cm

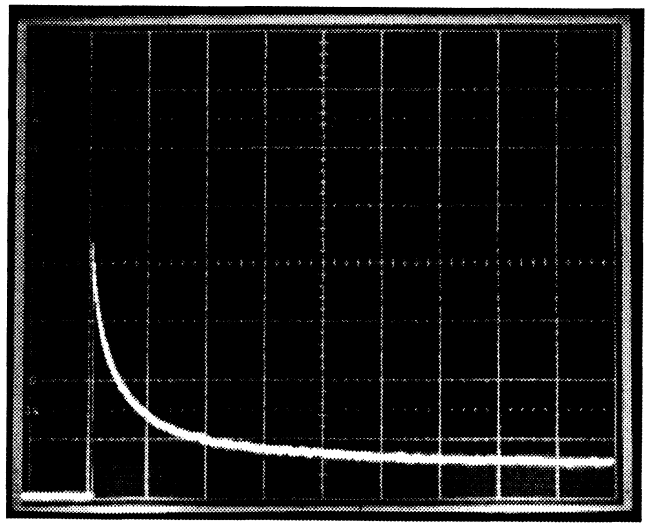
(f) LAMP TYPE 1003
LAMP-CURRENT TURN-ON WAVEFORM

Figure 9. Directly Driven Automobile Incandescent Lamps (continued)



Vertical: 2 A/cm
Horizontal: 10 ms/cm

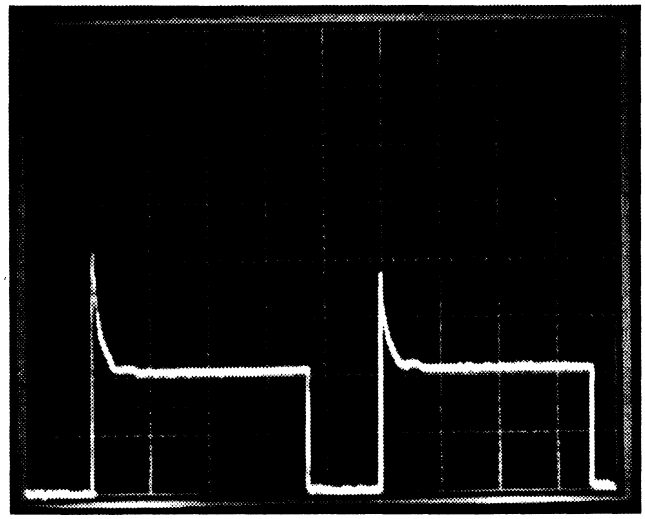
(g) LAMP TYPE 1004
LAMP-CURRENT TURN-ON WAVEFORM



Vertical: 2 A/cm
Horizontal: 10 ms/cm

(h) LAMP TYPE 211-2
LAMP-CURRENT TURN-ON WAVEFORM

Figure 9. Directly Driven Automobile Incandescent Lamps (continued)



Vertical: 2 A/cm
Horizontal: 200 ms/cm

(i) LAMP TYPE 211-2
TOTAL LAMP CURRENT OF ALL FOUR OUTPUTS

Figure 9. Directly Driven Automobile Incandescent Lamps (continued)

Stepping-Motor Driver

Stepping motors, due to their digital drive requirements, are natural motion providers for microprocessor or ASIC-based systems. The TPIC2406 provides a simple solution to the problem of translating logic-level timing to the high voltage and current requirements of stepping motors.

The permanent magnet-rotor stepping motor has two forms of stator winding. The bipolar stepping motor has a single winding on each stator pole and uses a full bridge to drive each phase winding. In the unipolar stepping motor, the flux reversal is accomplished by individually driving a bifilar winding on each pole. The windings are phased such that when current is passed through one winding, a given flux direction is generated. By passing current through the other winding, the opposite flux polarity is produced. Thus, the overall magnetic effect is the same as the bipolar motor, but the phase windings can be more economically driven by devices with open-drain outputs such as the TPIC2406.

Printers are one major application of stepping motors because the stepping motor is ideally matched to the needs of paper feeding. In this application, the paper is required to be moved in well-defined increments, which, through gearing, equates to fixed numbers of motor steps. There is also not a need for positional feedback as the paper position is initialized by the user or at paper loading. Therefore, the motion system is an open loop, and the paper is advanced by stepping the motor's rotor a given amount.

In the following example, a TPIC2406 replaces a collection of discrete components used to drive the paper-feed motor in an existing printer. Figure 10 shows the circuit.

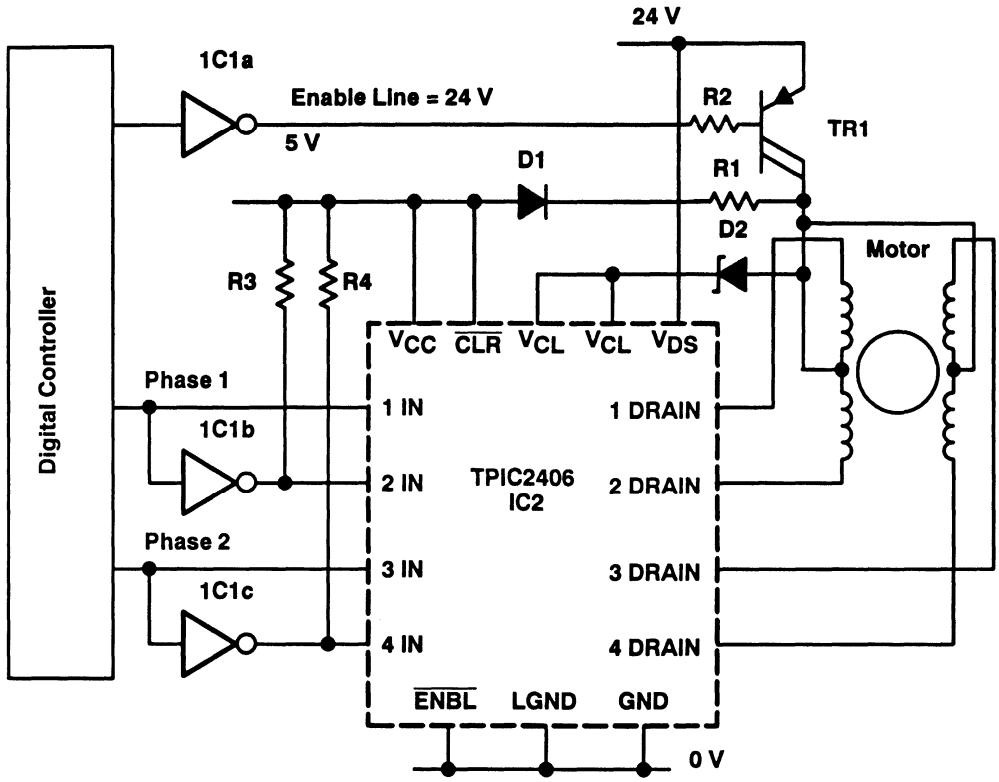


Figure 10. Stepping-Motor Drive

By virtue of their permanent magnet rotor, stepping motors have a degree of detent; that is, the motor naturally aligns to one of its step positions. For small external torques, this detent is sufficient to hold the rotor in position, but in printer applications, the motor's detent needs to be increased. This increase is to avoid paper movement when printing by feeding current through the appropriate windings. Only a low level of current is required, about 30 mA, which is most efficiently sourced from the 5-V logic rail via diode D1 and resistor R1. To provide the return path, the outputs have to be left in the same state that caused the last rotor step. In this particular design, $\overline{\text{CLR}}$ (which turns all outputs off) and $\overline{\text{ENBL}}$ functions are not used, and they are logically strapped high and low, respectively.

Two things must happen to cause the motor to step. The first is to supply 24 V to the winding center tap and then to toggle the four outputs to step the motor in the appropriate direction.

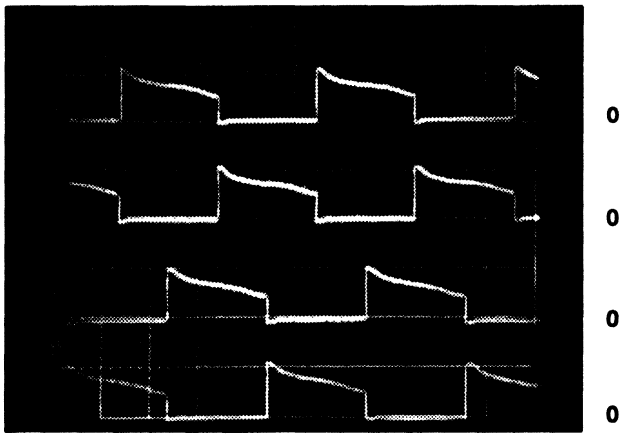
One pin of the digital controller switches on the output of an inverting open-drain buffer, IC1a. This, in turn, switches on the Darlington transistor, TR1, via resistor R2 to apply the 24-V supply to the motor. When this happens, the low current to supplement the motor's detent is terminated by diode D1, which becomes reverse biased.

When the motor is stepping, the four outputs produce square-wave waveforms as seen in Figure 11(a). These waveforms consist of two square waves, one displaced 90° from the other in both true and inverted forms.

Pin count is often at a premium on digital controllers, and in this solution, only two pins are used to provide the basic square waves that are applied to inputs 1 and 3. Two inverting buffers provide the drives for inputs 2 and 4.

When the motor stalls or starts rotation, the peak winding current is limited by the winding resistance. Figure 11(b), taken at motor start up, shows the peak winding current is limited to about 400 mA, which is well within the output current capability.

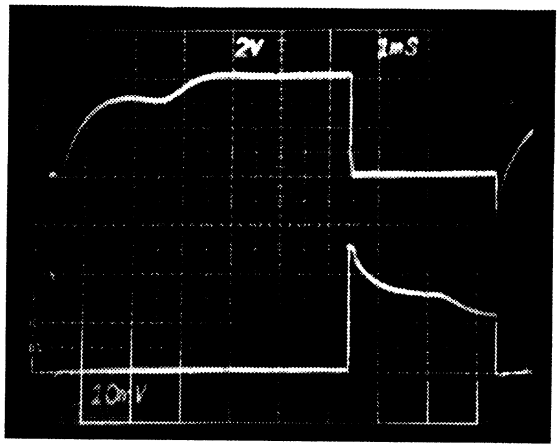
Figure 11(c) shows the current and voltage waveforms of a particular phase winding. Assessing the maximum possible power dissipation in the output involves summing the source-drain diode loss (when the current is negative), the $r_{DS(on)}$ loss (when the current is positive), and the clamp-diode loss when the voltage overshoot is limited. The peak output drain voltage is limited by connecting the clamp diodes back to the motor center tap via a 27-V zener diode, D2. Since the average current in this diode is only 6 mA, a 250-mW component could be used.



Vertical: 50 V/cm
Horizontal: 1 ms/cm

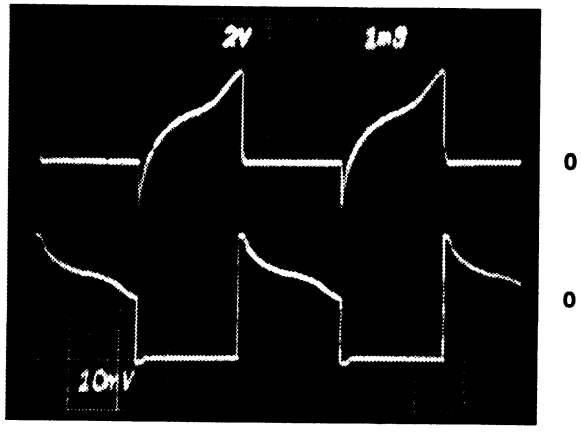
(a) STEPPING-MOTOR WINDING VOLTAGES

Figure 11. Stepping-Motor Oscilloscope Waveforms



Vertical: Top 200 mA/div
Bottom 20 V/div
Horizontal: 1 ms/div

(b) WINDING START-UP CURRENT AND VOLTAGE



Vertical: Top 200 mA/div
Bottom 20 V/div
Horizontal: 1 ms/div

(c) NORMAL RUNNING WINDING VOLTAGE AND CURRENT

Figure 11. Stepping-Motor Oscilloscope Waveforms(continued)

By linearizing the diode VI characteristic to a fixed starting voltage (V_T) and a slope resistance (R_d), the diode power loss can easily be derived. Considering the current flowing during the conduction period, it can be shown that the power loss at a fixed voltage (V_T) is the voltage multiplied by the mean current, I_{MEAN}. The power loss in a resistance is mean square current, I_{RMS}^2, multiplied by the resistance, R_d. The calculation for power loss of the diode is:

$$P_{diode} = (\text{conduction duty cycle})(V_T I_{mean} + R_{diode}(I_{rms})^2 \quad (19)$$

At 1.25 A, the source-drain and clamp diodes have maximum forward-voltage values of 1.5 V and 1.6 V, respectively. Choosing a V_T value of 0.7 V gives slope resistances for the source-drain and clamp diodes of 0.64 Ω and 0.72 Ω, respectively. Detailed examination of the drain-source diode's conduction shows it has a mean current of 0.095 A and an rms current of 0.11 A. The power loss for the drain-source diode is:

$$P_{d-s\ diode} = 0.033[0.7 \times 0.095 + 0.64(0.11)^2] \simeq 2.5\ mW \quad (20)$$

Similarly for the clamp diode, the mean current is 0.065 A, the rms current is 0.075 A, and a duty cycle of 0.022, which leads to a clamp-diode power loss of:

$$P_{clamp\ diode} = 0.022[0.7 \times 0.065 + 0.72(0.075)^2] \simeq 1.1\ mW \quad (21)$$

As can be seen, the diode losses in this application are extremely small.

The last output loss to be considered is due to $r_{DS(on)}$. At 125°C and 1.25 A, the maximum value of $r_{DS(on)}$ is 1 Ω. Graphically, integrating the square of the drain-current values gives a mean square current of 0.053 A^2 (0.23 A rms), which leads to a power loss of:

$$P_{MOSFET} = 1 \times 0.053 \simeq 53\ mW \quad (22)$$

The total loss of four outputs will be:

$$P_{output} = 4(53 + 1.1 + 2.5) \simeq 230\ mW \quad (23)$$

Finally, the power loss of the logic and driver circuits needs to be added to arrive at the total worst-case power loss of the TPIC2406. The data sheet maximums of 10 mA and 6 mA, respectively, are measured at 25°C. These values fall by about 30% at high temperatures; the worst-case high-temperature power loss becomes:

$$P_{total} = 230 + (5 \times 10 \times 0.7) + 24(6 \times 0.7) \simeq 366\ mW \quad (24)$$

Since the junction-to-ambient thermal resistance is 50°C/W, the maximum permissible ambient for the above dissipation becomes:

$$T_{A(max)} = 125 - 50 \times 0.366 = 107°C \quad (25)$$

This example illustrates the low operating losses of the TPIC2406.

A further application is a color changer for a dot matrix printer. In order to bring the different colored bands on the ribbon opposite the print head needles, either the ribbon or the whole ribbon cartridge is moved. These fixed mechanical movements can be implemented easily using a stepping motor.

Such a system can be economically added to the circuit of Figure 10(a) by using one extra pin on the digital controller for control of the supply rail to the changer motor. Paper feed and ribbon color change can be asynchronous so that the color change and paper feed motors do not need to step at the same time. Therefore, the inputs of the two drivers are connected in common and the individual drivers activated by use of $\overline{\text{ENBL}}$. This drive for $\overline{\text{ENBL}}$ comes from the 24-V enable line for that particular motor. When the motor supply is switched off, so is that particular $\overline{\text{ENBL}}$. This latches the outputs in their last step condition, which is required to increase the detent. When the motor stalls or starts rotation, the peak winding current is limited by the winding.

Conclusion

The TPIC2406 is an intelligent-power device that contains four 0.77-A/60-V self-protected low-side power MOSFET switches packaged in a 20-pin NE DIP package. Each output is controlled by an input storage latch with common clear and enable controls. All inputs accept standard TTL- and CMOS-logic levels.

The capability to extend the output switch 0.77-A load current by parallel switch operation is illustrated by the measurement data shown in Table 3, where data showing up to a 3.2-A load is switched by four parallel connected output switches.

The unclamped avalanche energy rating of 50 mJ per output switch greatly enhances its value as an inductive load driver. To illustrate this capability, Figure 7 shows the test circuit and waveforms switching four 25.7-mJ inductive loads (102.8-mJ total energy).

Self-protection capability is illustrated by the measurement data shown in Table 4. Independent thermal shutdown circuits monitor each output and disable all outputs when the maximum temperature is reached, typically 155°C.

This device provides a simple solution to the problem of translating logic-level timing to the high-voltage and current requirements of stepping motors. The Application Design example, *TPIC2406 Stepping-Motor Driver*, explains how a TPIC2406 is used to replace a collection for discrete components used to drive the paper-feed motor in an existing printer.

Acknowledgment

The author, Joe Mings, wishes to thank Mick Maytum for contributing to the Application Section, "Stepping-Motor Driver".

Also, thanks is given to Dave Cotton, Dave Baldwin, Ira Frost, and Ken Echelberger for their important technical contributions.

TPIC2801 Intelligent-Power Device With Serial Input and Eight 1-A/30-V, Low-Side Power Switches

TEXAS INSTRUMENTS

Contents

List of Illustrations

Introduction

The TPIC2801 is a monolithic, intelligent-power device that contains eight 1-A/30-V low-side power switches packaged in a 15-pin single-in-line package (SIP). The eight switches are controlled from a single input, SI (serial input), by an 8-bit serial word. Diagnostics are provided through the output, SO (serial output), which permits a comparison of the serial input data with the serial output data. Data no-match indicates a fault condition.

The independent overvoltage and overcurrent protection provided to all eight switches allows the TPIC2801 to switch in harsh electrical and thermal environments. Also, the eight switches are equipped with an internal 35-V collector-to-base zener clamp that greatly enhances their capability to switch unclamped inductive loads. Since the clamp allows the power switch to be forward biased instead of avalanched during inductive-load turn off, a 40-mJ maximum unclamped inductive-energy capability can be achieved.

In addition to the direct drive of peripheral loads such as lamps, solenoids, relays, and motors, the TPIC2801 is also recommended for driving power bipolar and power MOSFET transistors. A power bipolar transistor, when switching amperes of load current, requires several hundred milliamperes of base current for saturated switching. A power MOSFET transistor, when switching at high speed, also requires several hundred milliamperes of peak gate drive current. The TPIC2801 can easily meet all of these requirements.

Functional Description

The TPIC2801 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit parallel latch, which independently controls each of the eight Y-output drivers (see Figure 1).

Data is entered into the device serially via SI and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic high bit at SI turns the corresponding output driver (Yn) off. A logic low bit at SI turns the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of SCLK (serial clock) input in 8-bit bytes with data for Y7 output (MSB) first and data for the Y0 output (LSB) last. Both SI and SCLK are active when $\overline{\text{SIOE}}$ (serial input-output enable) is low and disabled when $\overline{\text{SIOE}}$ is high.

Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal out-of-saturation threshold voltage reference level. The logic state of the comparator's output is dependent upon whether the Y-output is greater or smaller than the reference voltage level. An activated driver output is unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level except when the internal unlatch enable is low and disabled. The high-to-low transition of $\overline{\text{SIOE}}$ transfers the logic state of the comparator's output to the shift register.

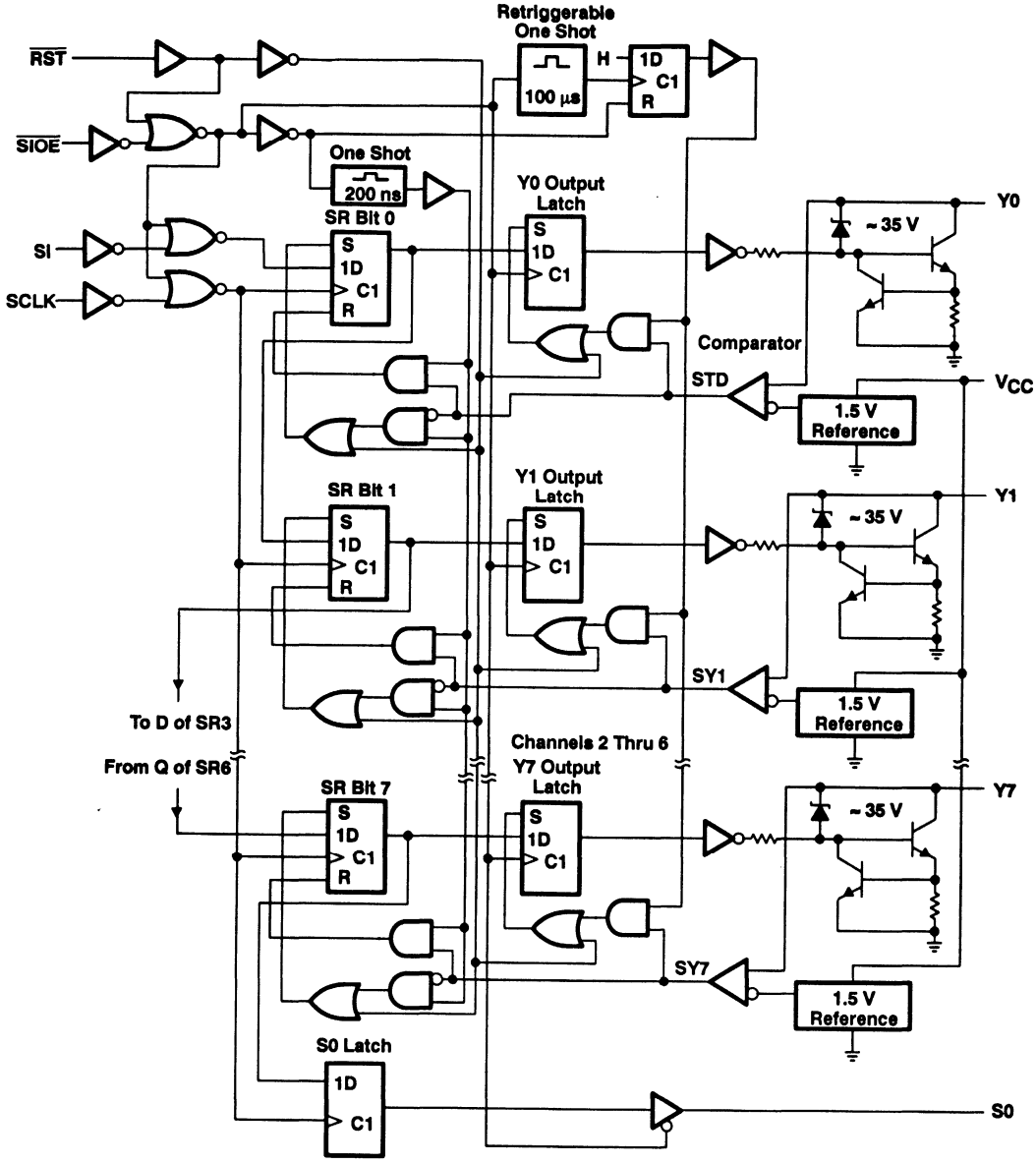
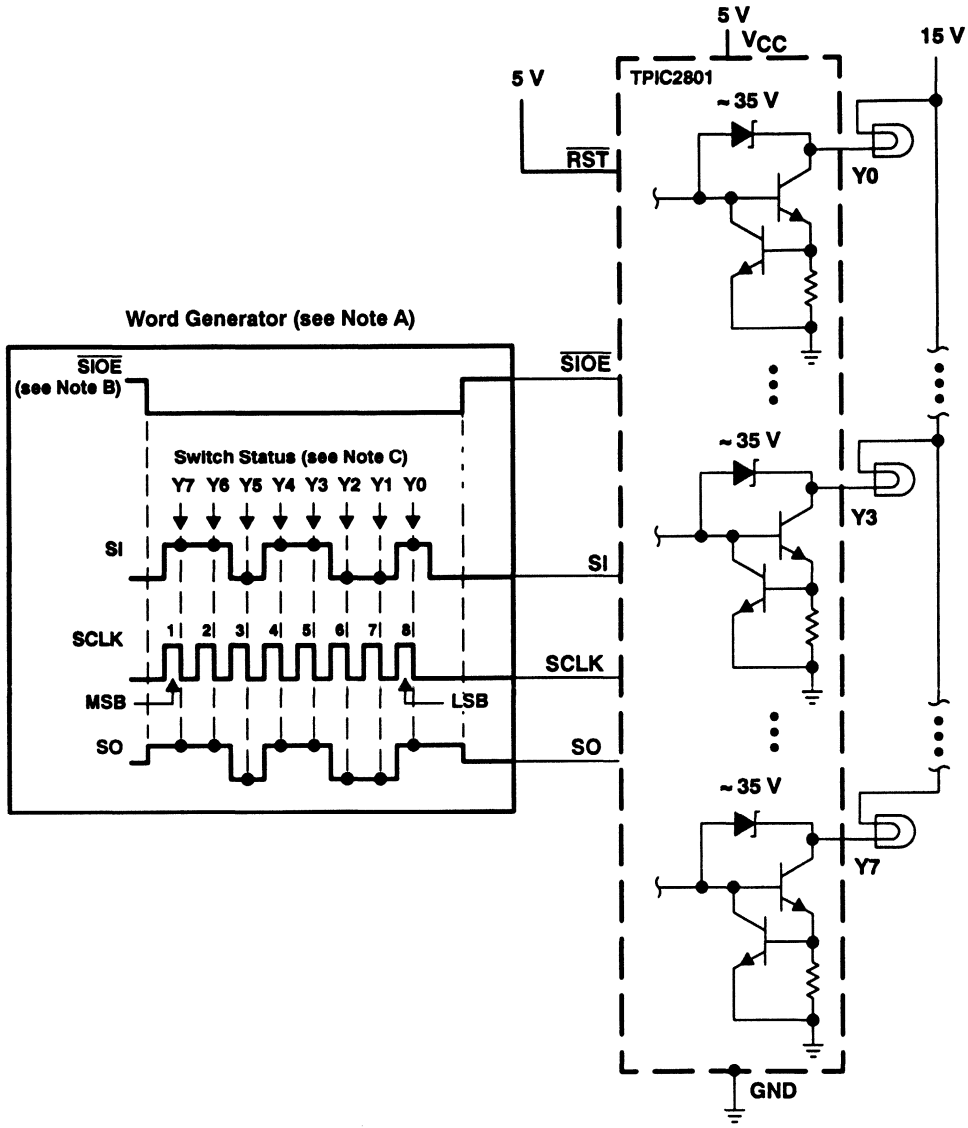


Figure 1. Functional Block Diagram

Figure 2 illustrates a switching operation. The figure contains a timing diagram that shows a controller programmed for latching on output switches Y5, Y2, and Y1 (serial input data word 11011001).



NOTES: A. Serial input word = 11011001

B. All outputs are latched during the positive-going $\overline{\text{SIOE}}$ edge; outputs Y1, Y2, and Y5 are latched on, and other outputs are latched off.

C. An SI high during the negative-going SCLK edge turns the corresponding output off; an SI low turns the corresponding output on.

Figure 2. Switching Operation

Application Design Considerations

Power and Thermal Considerations

Power dissipation of the individual switches is a function of the output load current and can be determined from the graph in Figure 3.

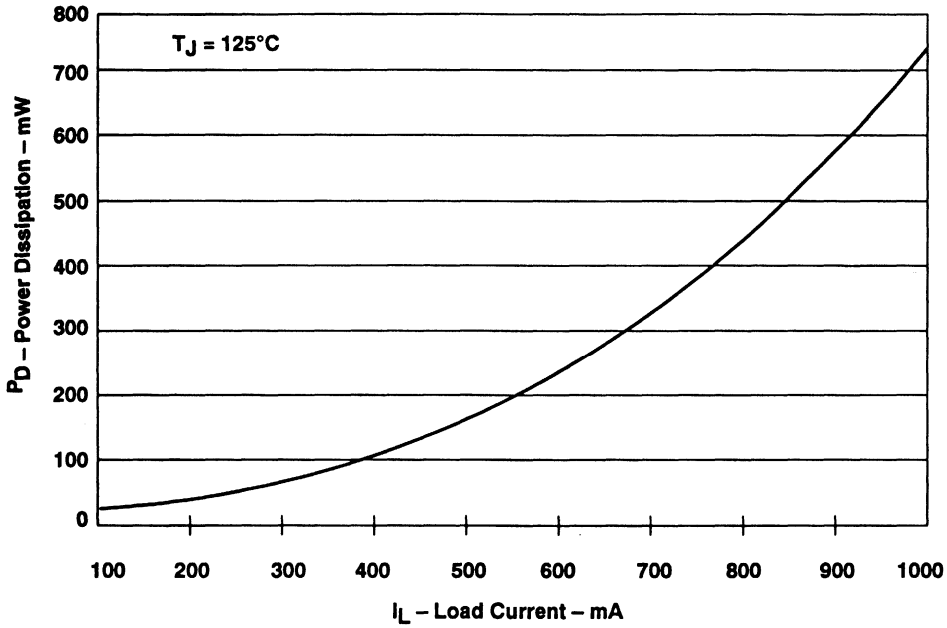


Figure 3. Power Dissipation vs Load Current

The requirement for external heat sinking is calculated from the device's total average power dissipation, maximum junction temperature, and ambient operating temperature as seen in equation (1).

$$R_{\theta SA} = \frac{T_J - T_A}{P_{T(AV)}} - \left| R_{\theta JC} + R_{\theta CS} \right| \quad (1)$$

Where:

$R_{\theta SA}$ = heat sink-to-ambient thermal resistance, °C/W
$R_{\theta JC}$ = device junction-to-case thermal resistance
= 3.0°C/W
$R_{\theta CS}$ = case-to-heat sink thermal resistance, °C/W
= 0.5°C/W typical with thermal joint compound
$P_{T(AV)}$ = total average power dissipation, W
T_J = junction operating temperature, °C
T_A = operating ambient temperature, °C

If the $R_{\theta SA}$ calculated is less than 35°C/W, an external heat sink is required. The size heat sink necessary to achieve the required $R_{\theta SA}$ can be determined from Figure 4 or from a heat-sink catalog.

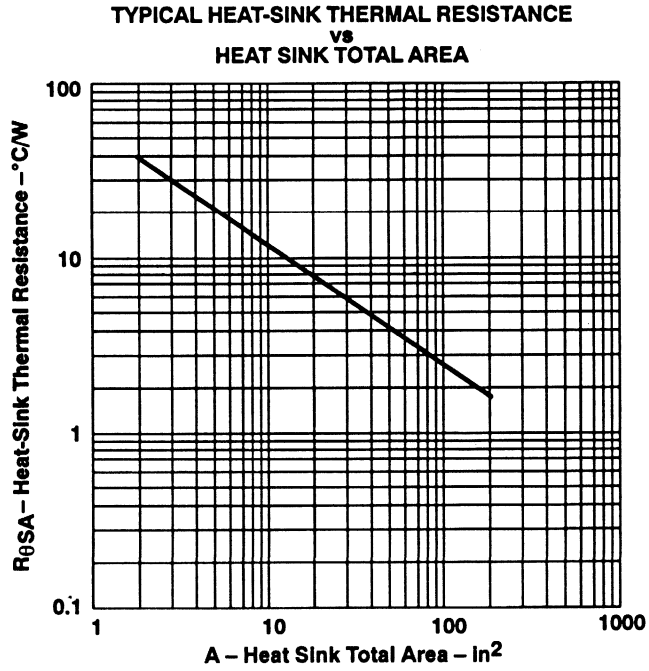


Figure 4

Example 1: Determining Heat-Sink Thermal Resistance and Size

Operating Conditions

T_A = 100°C
T_J = 125°C
Quiescent Current: I_{CC} = 0.25 A
Supply Voltage: V_{CC} = 5 V
Output Switches Y0 @ Y4: I_L = 0.5 A each, duty cycle = 0.5
Output Switches Y1 @ Y5: I_L = 0.7 A each, duty cycle = 0.8
Output Switches Y2 @ Y6: I_L = 0.8 A each, duty cycle = 1
Output Switch Y3: I_L = 0.5 A, duty cycle = 1
Output Switch Y7: I_L = 0.9 A, duty cycle = 1

The equations from Figure 3 are as follows:

P(Y0 @ Y4) = 0.15 W × 0.5 × 2 = 0.15 W
P(Y1 @ Y5) = 0.3 W × 0.8 × 2 = 0.48 W
P(Y2 @Y6) = 0.4 W × 1 × 2 = 0.8 W
P(Y3) = 0.15 W × 1 × 1 = 0.15 W
P(Y7) = 0.53 W × 1 × 1 = 0.53 W

From specification: P(QUIES) = 0.25 A × 5 V = 1.25 W

The total average power dissipation is calculated in equation (2).

$$P_{T(AV)} = P[(Y0 @ Y4) + (Y1 @Y5) + (Y2 @ Y6) + Y3 + Y7] + P(QUIES) \quad (2)$$
$$= 3.36 \text{ W}$$

This number is then used to calculate the heat-sink thermal resistance in equation (1).

$$R_{\theta SA} = \frac{T_J - T_A}{P_{T(AV)}} - \left| R_{\theta JC} + R_{\theta CS} \right| \quad (1)$$

$$= 3.94°C/W$$

From Figure 4, the heat sink total area (both sides) is A = 50 in^2. Using this number for the area, the heat sink dimensions, length = width = l, can be determined using equation (3).

$$l = \sqrt{\frac{A}{2}} = 5 \text{ in} \times 5 \text{ in} \quad (3)$$

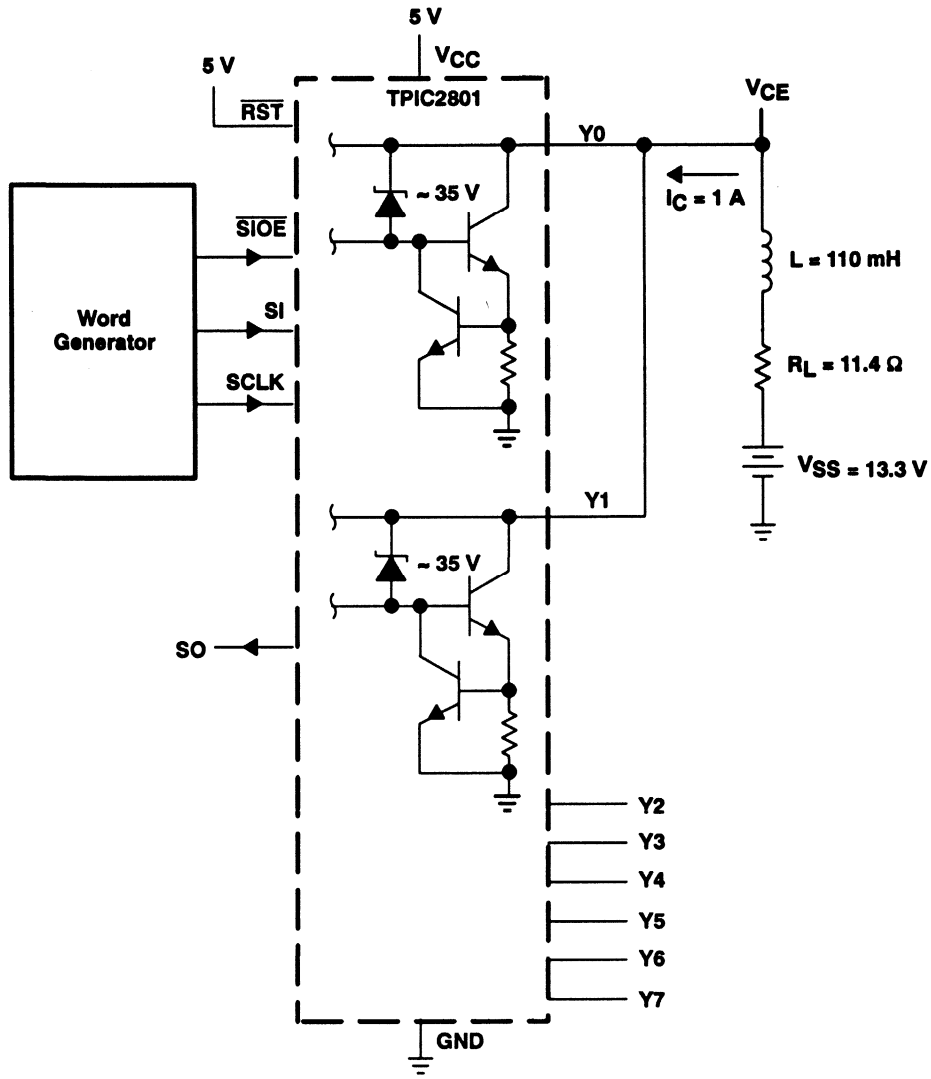
Switching Unclamped-Inductive Loads and Turn-Off Power Dissipation, P_{OFF}

A maximum energy rating of 40 mJ per power switch is achieved by providing each of the eight power switches with an internal 35-V collector-to-base voltage clamp. Therefore, for inductive loads equal to or less than 40 mJ, no external voltage clamp is required. The collector-to-base clamp forces energy to be absorbed by the TPIC2801 in the rugged forward-bias mode vs the unclamped, less rugged reverse-bias mode. The switches can also be operated in parallel to extend the capability of an individual switch.

Figure 5(a) shows two of the power switches connected in parallel switching a 110-mH/11.4-Ω/1-A load at a 50% duty cycle, 22-Hz repetition rate from a 13.3-V supply.

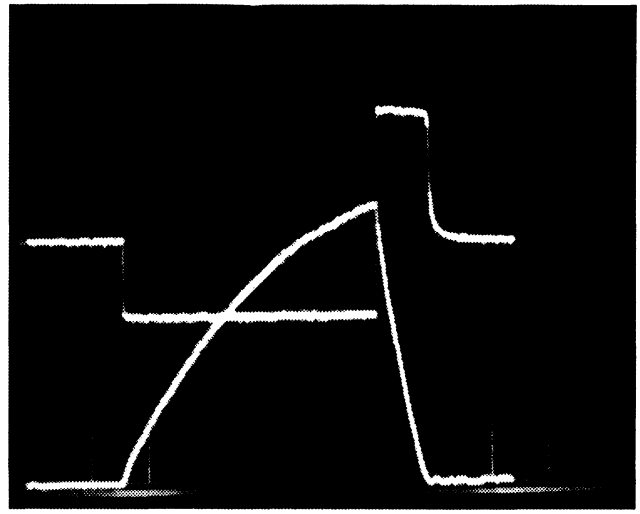
Figure 5(b) shows the total load current and parallel switch voltage waveform when the device is absorbing a calculated total inductive energy of 65.7 mJ (32.8 mJ per switch) using equation (4).

$$E_T = E_L + E_S - E_R = \frac{3 \times L_H \times I_P{}^2 \times V_{OK}}{6 \times V_{OK} - 6 \times V_{SS} + 4 \times R_L \times I_P} = 65.7 \text{ mJ} \quad (4)$$



(a) POWER SWITCHES CONNECTED IN PARALLEL

Figure 5. Intelligent-Power Switch



(b) TOTAL LOAD CURRENT AND PARALLEL SWITCH VOLTAGE WAVEFORM

Figure 5. Intelligent-Power Switch (continued)

The calculated turn-off power dissipation, P_{OFF}, that results solely from the inductive energy is 1.44 W using equation (5). Consequently, device heat sinking may be required (see the Power and Thermal Considerations section for more details).

$$P_{OFF} = E_T \times f = 0.0657\ J \times 22\ Hz = 1.44\ W \quad (5)$$

Where:

E_L	Inductive energy stored in inductor	55 mJ
E_R	Energy absorbed by resistance during turn-off transient	14.3 mJ
E_S	Energy from power supply during turn-off transient	25 mJ
E_T	Total energy absorbed during turn-off transient	65.7 mJ
f	Switching frequency	22 Hz
L_H	Load inductance	110 mH
I_P	Peak output load current	1 A
P_{OFF}	Turn-off power dissipation TPIC2801	1.44 W
R_L	Resistance of inductor	11.4 Ω
V_{OK}	Clamp voltage	35 V
V_{SS}	Load supply voltage	13.3 V

Based on "JEDEC Suggested Standard No. 10 for Power Transistors", paragraph 3.2.5, the TPIC2801 under test absorbs a total energy of 65.7 mJ maximum and dissipates a turn-off power of 1.44 W minimum per the test conditions specified above.

Parallel Operation of Output Switches for Extended Current Capability

If all eight output switches are not needed for an application and an output load current greater than 1 A is required, the switches can be connected in parallel for extended current capability. The current sharing capability of the switches is demonstrated in the Figure 6 circuit, while operating at T_A = 25°C on a 3.5- x 3.5-inch heat sink. The individual switch currents are listed in Table 1 when the device conducted a total current of 1) 4 A with eight switches on, 2) 3 A with six switches on, 3) 2 A with four switches on, and 4) 1 A with two switches on.

Table 1. Typical Load Current Data, Parallel Switch Operation

Tab Temp (°C)	$I_{(T)}$ (A)	V_{CE} (V)	$I_{(0)}$ (A)	$I_{(1)}$ (A)	$I_{(2)}$ (A)	$I_{(3)}$ (A)	$I_{(4)}$ (A)	$I_{(5)}$ (A)	$I_{(6)}$ (A)	$I_{(7)}$ (A)
40	4	0.53	0.6	0.52	0.45	0.43	0.45	0.46	0.51	0.58
35	3	0.47	0.58	off	0.45	0.43	off	0.46	0.51	0.57
31	2	0.41	off	0.51	off	0.46	off	0.47	off	0.56
28	1	0.39	off	off	off	0.5	0.5	off	off	off

Application Design Examples

Operation of Eight Lamps Featuring Soft-Start Circuit

Figure 7 shows the circuit switching eight No. 168 automotive lamps from a 15-V source and various waveforms.

Figure 7(a), with the clock operating at a frequency of 5 kHz, shows the input control waveforms $\overline{\text{SIOE}}$, SCLK, SI (00000000 for all eight outputs on), and the SO output. Figure 7(b) shows the initial lamp in-rush current decrease from a value slightly greater than 1.5 A to a value less than 0.5 A during a period of approximately 120 ms. Figure 7(c) shows the first $\overline{\text{SIOE}}$ pulse that follows the first data word and the lamp current, a 1.5-A/100-µs pulse that is coincident with the rising edge of the $\overline{\text{SIOE}}$ pulse.

The rising edge of the $\overline{\text{SIOE}}$ pulse following the data word is when shift register data is latched into the parallel latch and the output switches are activated by the new data. However, to allow the part to overcome high in-rush current such as lamp cold filament current, an internal 100-µs delay timer is started at the $\overline{\text{SIOE}}$ pulse rising edge. The switch overvoltage fault shutdown circuit is inhibited. During this 100-µs interval, the switch is protected by an internal current limiter, which is set to regulate the current to approximately 1.5 A to 1.8 A. Once the 100-µs delay period has elapsed, the output voltages are sensed by the comparators, and any output switch with voltage higher than 1.5 V is latched off. These current-limited, 100-µs, soft-start bursts of power not only protect the TPIC2801, but also protect the lamp filament from an otherwise filament degrading, high in-rush current.

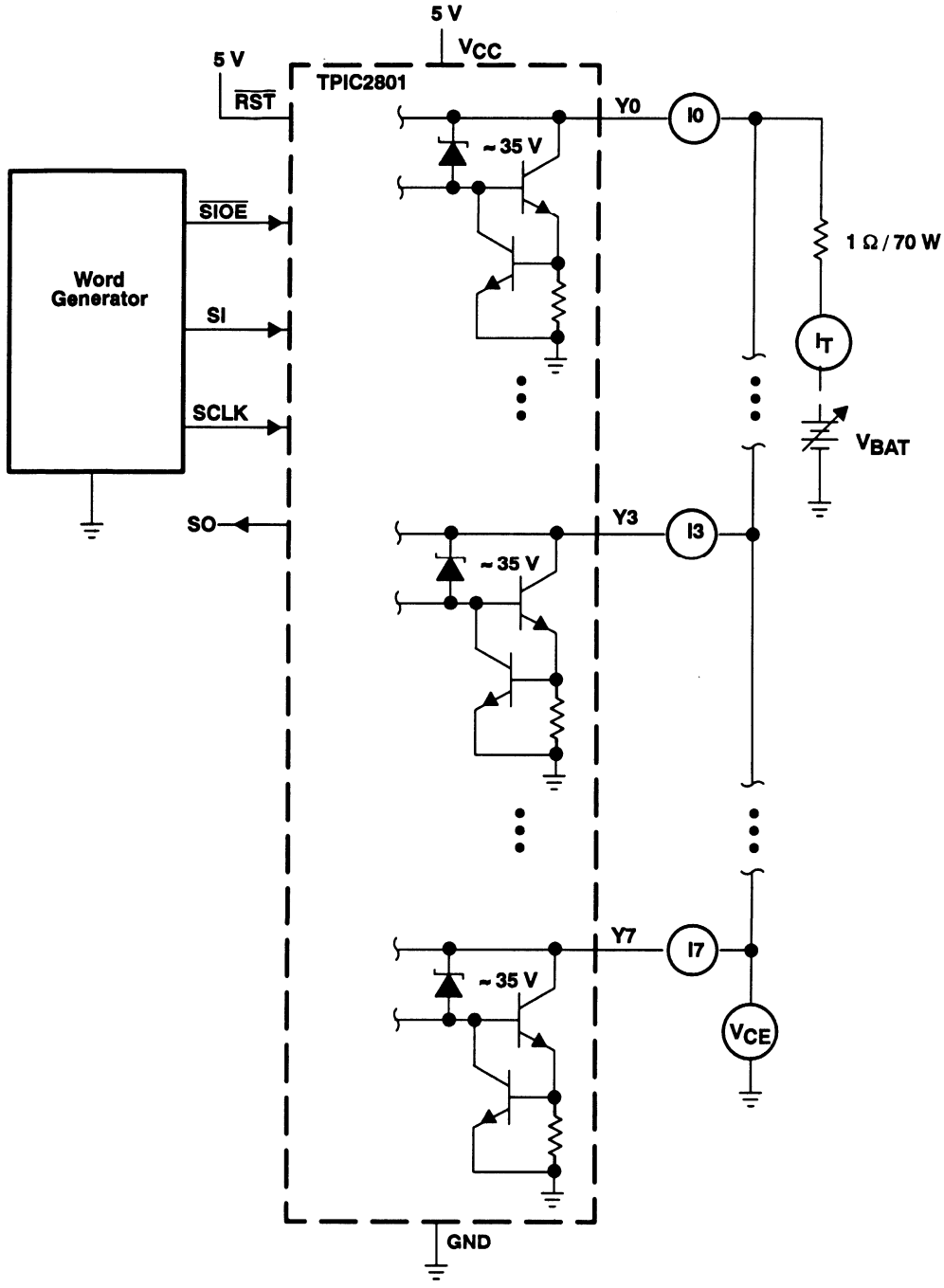
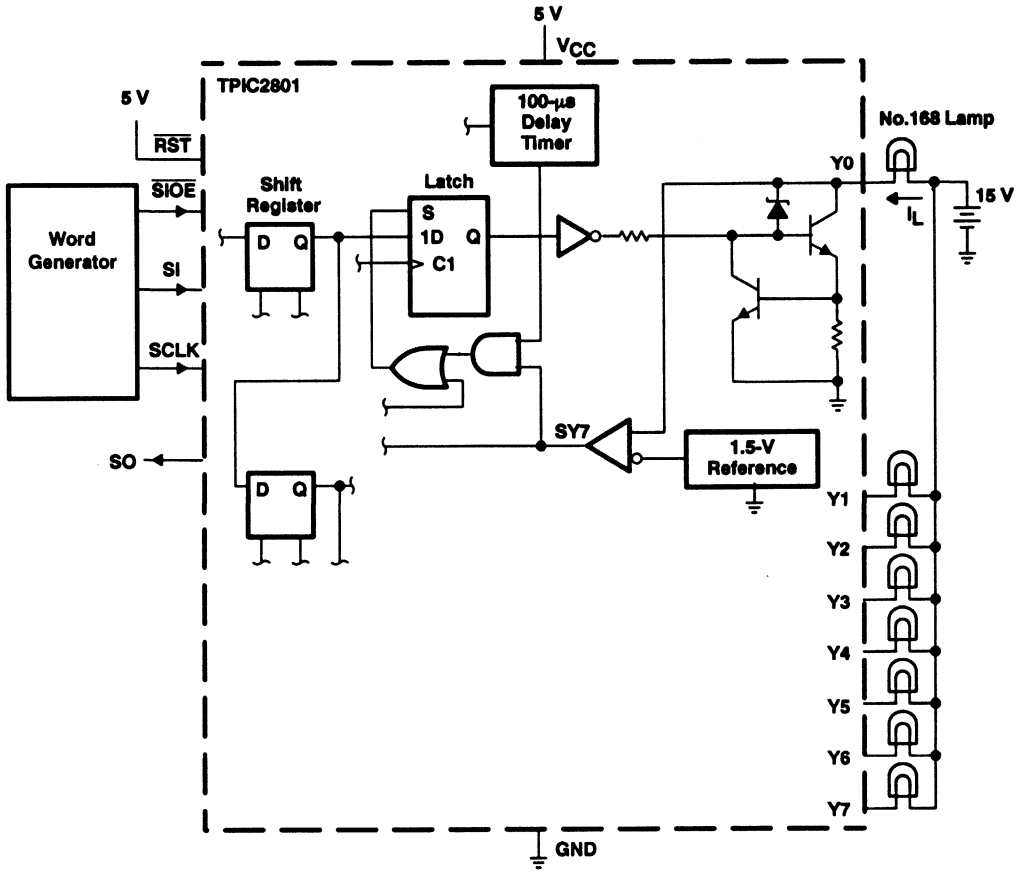
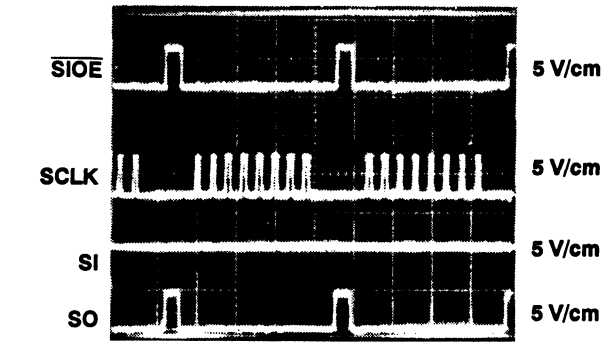


Figure 6. Parallel Operation of Output Switches for Extended Current Capability



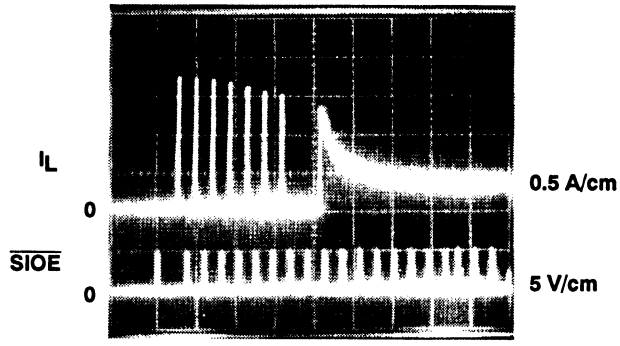
(a) AUTOMOTIVE LAMP SWITCHING TEST CIRCUIT

Figure 7. Simultaneous Switching of Eight Automotive Lamps



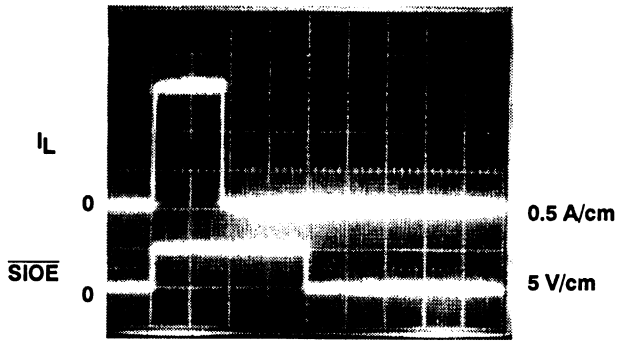
Horizontal = 5 ms/cm

(b) WORD GENERATOR AND SO



Horizontal = 20 ms/cm

(c) INITIAL LAMP IN-RUSH CURRENT PULSES



Horizontal = 50 ms/cm

(c) INITIAL $\overline{\text{SIOE}}$ AND LAMP CURRENT PULSE

Figure 7. Simultaneous Switching of Eight Automotive Lamps (continued)

Direct Drive of Automobile High-Impedance Fuel Injectors

Figure 8 shows the test circuit and oscilloscope waveforms of the TPIC2801 switching four automobile high-impedance fuel injectors (R = 13.3 Ω and L = 9 mH) from a 15-V source. The TPIC2801 provides 1-A rated current to each injector by the parallel operation of output switches Y0 || Y4, Y1 || Y5, Y2 ||Y6, and Y3 || Y7.

The calculated total inductive energy absorbed by each parallel switch combination is 5.3 mJ as seen in equation (4), which is considerably less than the 40 mJ per switch TPIC2801 rating. For more information, see the Switching Unclamped Inductive Loads section.

$$E_T = E_L + E_S - E_R = \frac{3 \times L_H \times I_P{}^2 \times V_{OK}}{6 \times V_{OK} - 6 \times V_{SS} + 4 \times R_L \times I_P} = 5.3 \text{ mJ} \quad (4)$$

The calculated turn-off power dissipation P_{OFF} is 0.47 W as seen is equation (5).

$$P_{OFF} = E_T \times f = 0.0053 \text{ J} \times 22 \text{ Hz} \times 4 \text{ loads} = 0.47 \text{ W} \quad (5)$$

Where:

E_L	Inductive energy stored in inductor	4.5 mJ
E_R	Energy absorbed by resistance during turn-off transient	1.1 mJ
E_S	Energy from power supply during turn-off transient	1.9 mJ
E_T	Total energy absorbed by TPIC2801 during turn-off transient	5.3 mJ
f	Switching frequency	22 Hz
L_H	Load inductance	9 mH
I_P	Peak output load current	1 A
P_{OFF}	Turn-off power dissipation (from L_H energy)	0.47 W
R_L	Resistance of inductor	13.3 Ω
V_{OK}	Clamp voltage	37 V
V_{SS}	Load supply voltage	15 V

Unipolar Stepper-Motor Drive

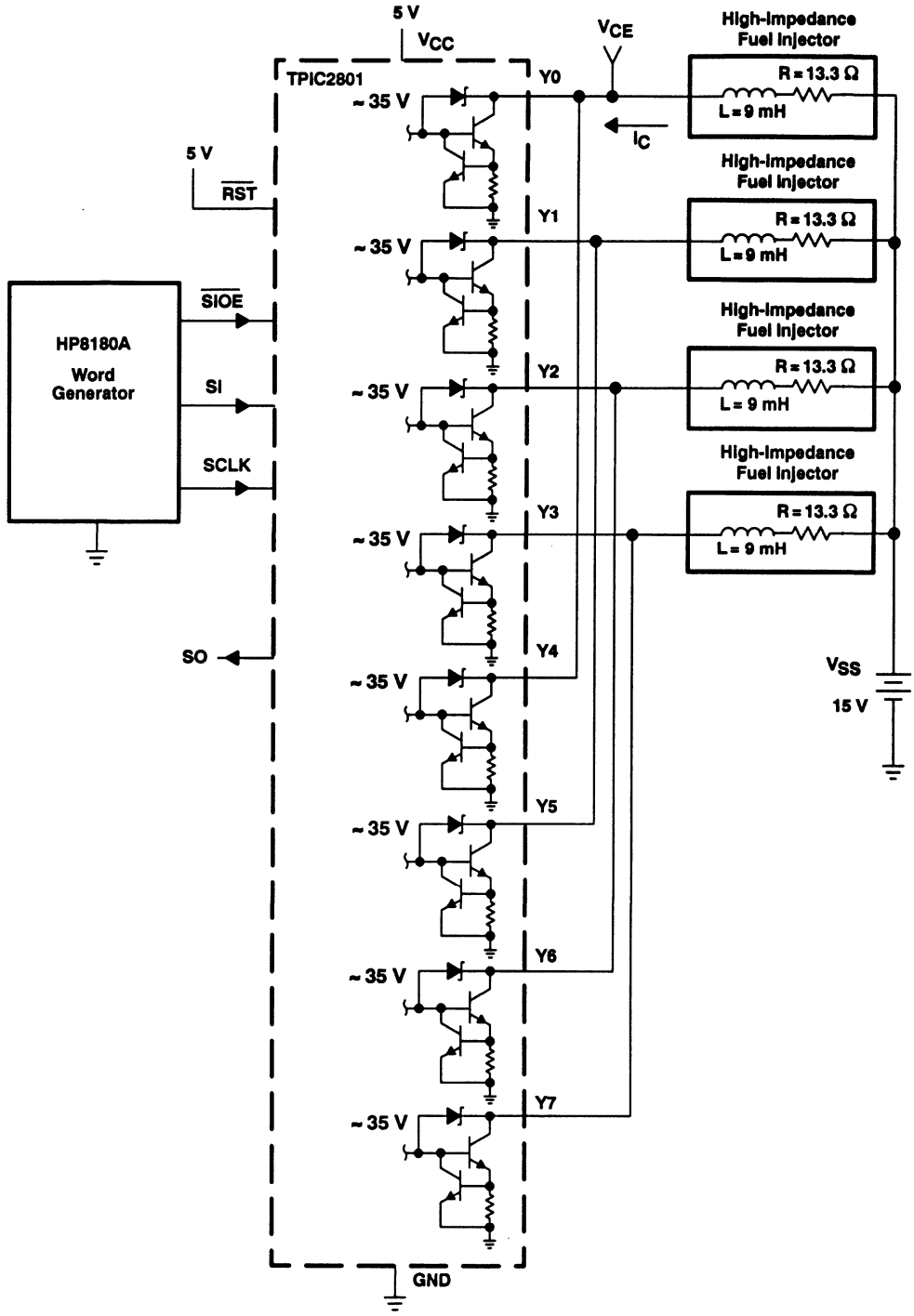
Figure 9 is a unipolar stepper-motor circuit illustrating the 1-A rated drive current to each of the four motor windings by parallel operation of output switches Y0 || Y4, Y1 || Y5, Y2 || Y6, and Y3 || Y7.

The input logic is normally provided by a microprocessor controller; however, for this design example, a Hewlett Packard HP8180A data generator is programmed to generate the input step logic (see Table 2).

Table 2. Word Generator Program (Four-Step Sequence)

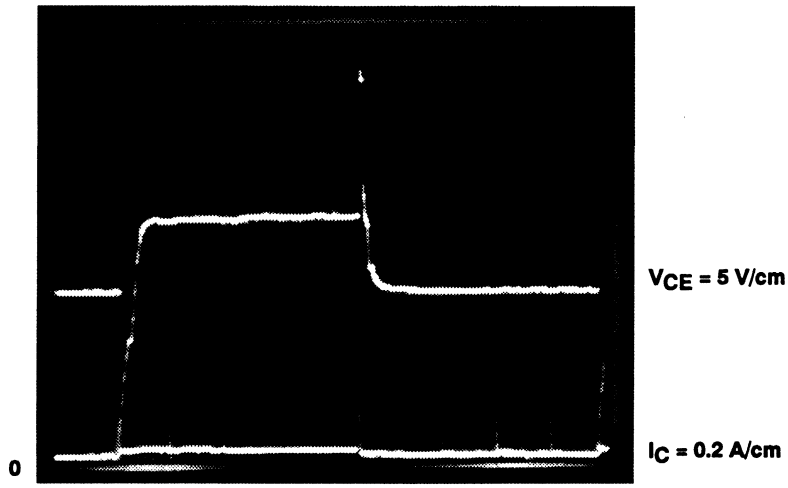
CW STEP†	SI INPUT DATA WORD	TPIC2801 SWITCHES ON
1	10101010	Y0 || Y4, Y2 || Y6
2	10011001	Y1 || Y5, Y2 || Y6
3	01010101	Y1 || Y5, Y3 || Y7
4	01100110	Y0 || Y4, Y3 || Y7
1	10101010	Y0 || Y4, Y2 || Y6

† For CCW rotation, read step sequence up from bottom.



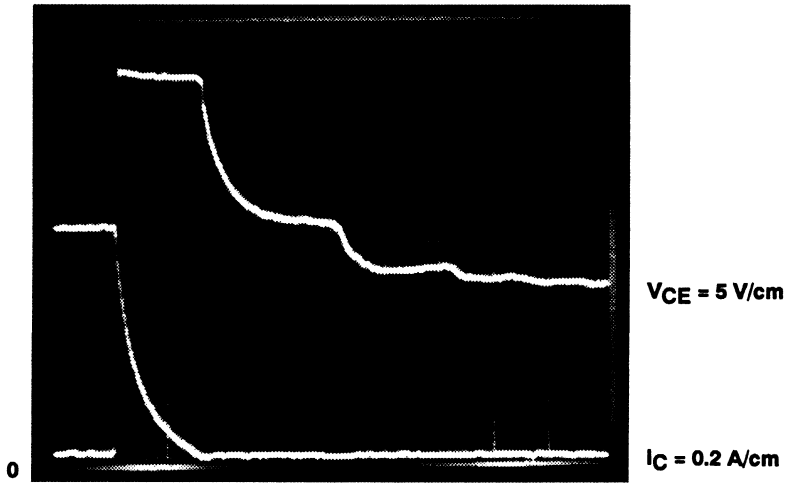
(a) AUTOMOTIVE FUEL-INJECTOR SWITCHING TEST CIRCUIT

Figure 8. Switching Multiple High-Impedance Fuel Injectors



Horizontal = 5 ms/cm

(b) OUTPUT VOLTAGE AND CURRENT WAVEFORMS



Horizontal = 0.2 ms/cm

(c) EXPANDED VIEW OUTPUT VOLTAGE AND CURRENT WAVEFORMS

Figure 8. Switching Multiple High-Impedance Fuel Injectors (continued)

The system clock is set for a frequency of 4 kHz based on time per motor step of 2.5 ms and based on a total of ten clock pulses required per each motor step as seen in equation (6), i.e., eight clock pulses for the data word plus one additional clock pulse before and after the data word.

$$t_{CLK} = \frac{2.5 \text{ ms/step}}{10 \text{ clock pulses step}} = 0.25 \text{ ms or } f_{CLK} = 4 \text{ kHz} \quad (6)$$

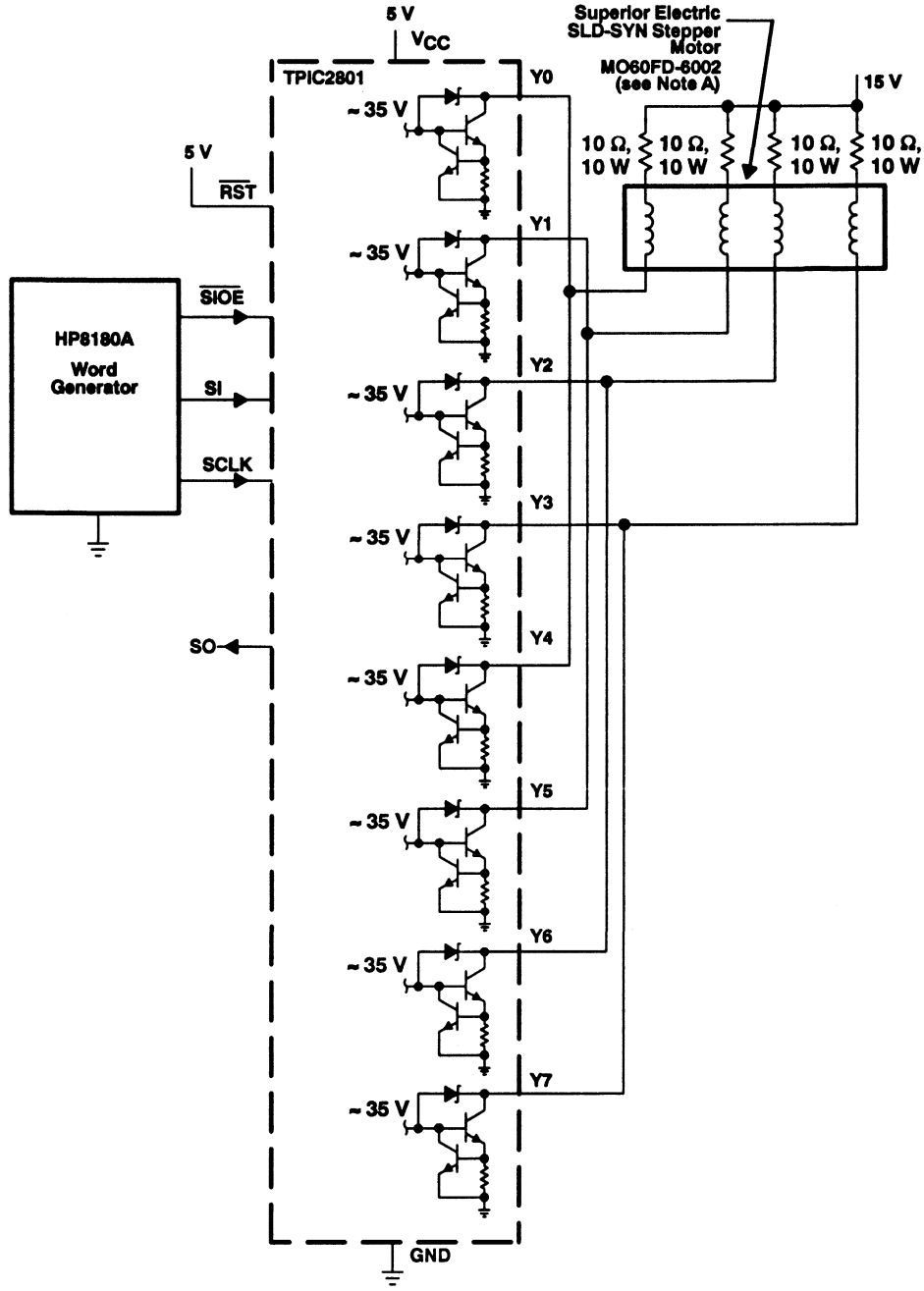
One important feature of the TPIC2801 as a stepper-motor driver is that it requires no external voltage clamps because all its outputs are protected by internal, high-energy, 35-V voltage clamps.

Cascade Operation of Multiple TPIC2801s

By shifting data into SI and out SO, TPIC2801s can be connected in cascade. Figure 10 shows two TPIC2801s connected in cascade. Also included is an example of SI timing of the16-bit data word for turning on the device no. 2's output switches Y6(2), Y4(2), Y2(2), and Y0(2). The device no. 1's output switches Y3(1), Y2(1), Y1(1), and Y0(1) are also turned on. Figure 10 is an oscilloscope waveform of device no. 1's operation per the conditions described.

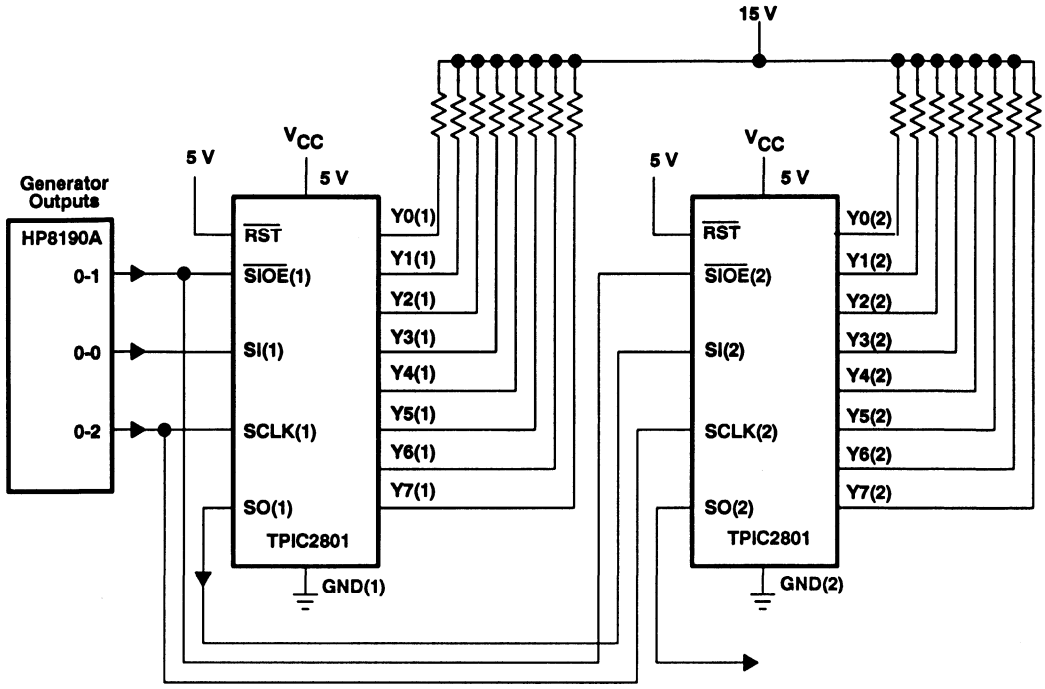
$\overline{\text{SIOE}}$ is pulled low at the beginning of the SI 16-bit data word and is pulled high at the end of the data word. In addition, SCLK should be low at both transitions of $\overline{\text{SIOE}}$ to avoid any false clocking of the shift register.

The HP8180A data generator data page for generating the example 16-bit timing diagram explained above is listed in Table 3.

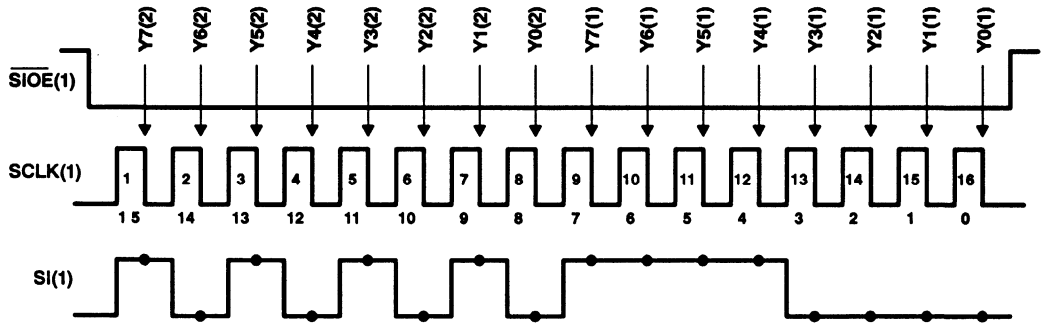


NOTE A: I = 1 A per phase, L = 10 mH per phase, R = 5 Ω per phase, T = 2.5 ms per step.

Figure 9. Unipolar Stepper-Motor Drive Circuit

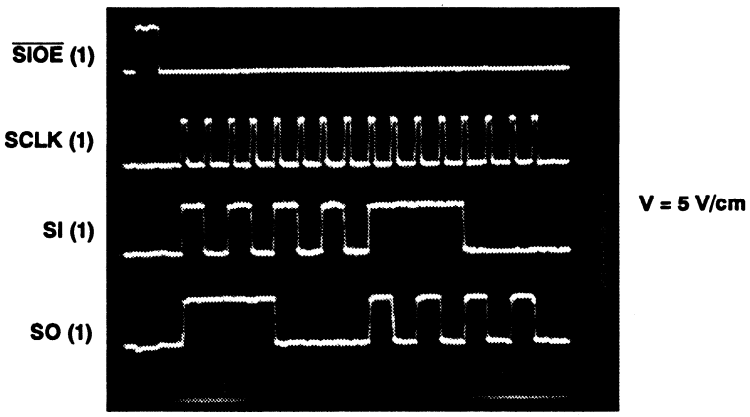


(a) TWO TPIC2801s CONNECTED IN CASCADE



(b) SI TIMING DIAGRAM OF 16-BIT DATA WORDS

Figure 10. Cascade Operation of Multiple TPIC2801s



(c) WAVEFORMS OF FIGURE 10(b) AND NO. 1 OUTPUT SO

Figure 10. Cascade Operation of Multiple TPIC2801s (continued)

Table 3. HP8180A Data Generator Data

ADDRESS	STR	DATA (for generator outputs)			
		0–3 Out (not used)	0–2 Out RZ† SCLK	0–1 Out NRZ SIOE	0–0 Out NRZ SI
0000	1	x	0	1	0
0001	0	x	0	0	0
0002	0	x	1	0	1
0003	0	x	1	0	0
0004	0	x	1	0	1
0005	0	x	1	0	0
0006	0	x	1	0	1
0007	0	x	1	0	0
0008	0	x	1	0	1
0009	0	x	1	0	0
0010	0	x	1	0	1
0011	0	x	1	0	1
0012	0	x	1	0	1
0013	0	x	1	0	1
0014	0	x	1	0	0
0015	0	x	1	0	0
0016	0	x	1	0	0
0017	0	x	1	0	0
0018	0	x	0	0	0

† The width is equal to 2.5 μs.

NOTE: The frequency is equal to 100 kHz.

Simultaneous Turn-on/Turn-off of Eight Inductors that Simulate Driving Solenoids Under Worst-Case Conditions

Figure 11 shows the test circuit and oscilloscope waveforms switching eight high-inductance inductors (R = 30 Ω and L = 250 mH) from a 15.5-V source. A 0.5-A current is provided to each inductor while each output switch absorbs an inductive energy of 36.7 mJ per switch cycle as seen in equation (4). This is the safe operating condition based on the TPIC2801's 40-mJ maximum unclamped energy rating.

$$E_T = E_L + E_S - E_R = \frac{3 \times L_H \times I_P{}^2 \times V_{OK}}{6 \times V_{OK} - 6 \times V_{SS} + 4 \times R_L \times I_P} = 36.7 \text{ mJ} \quad (4)$$

The calculated power dissipation P_{OFF} is 1.58 W, as seen in equation (5).

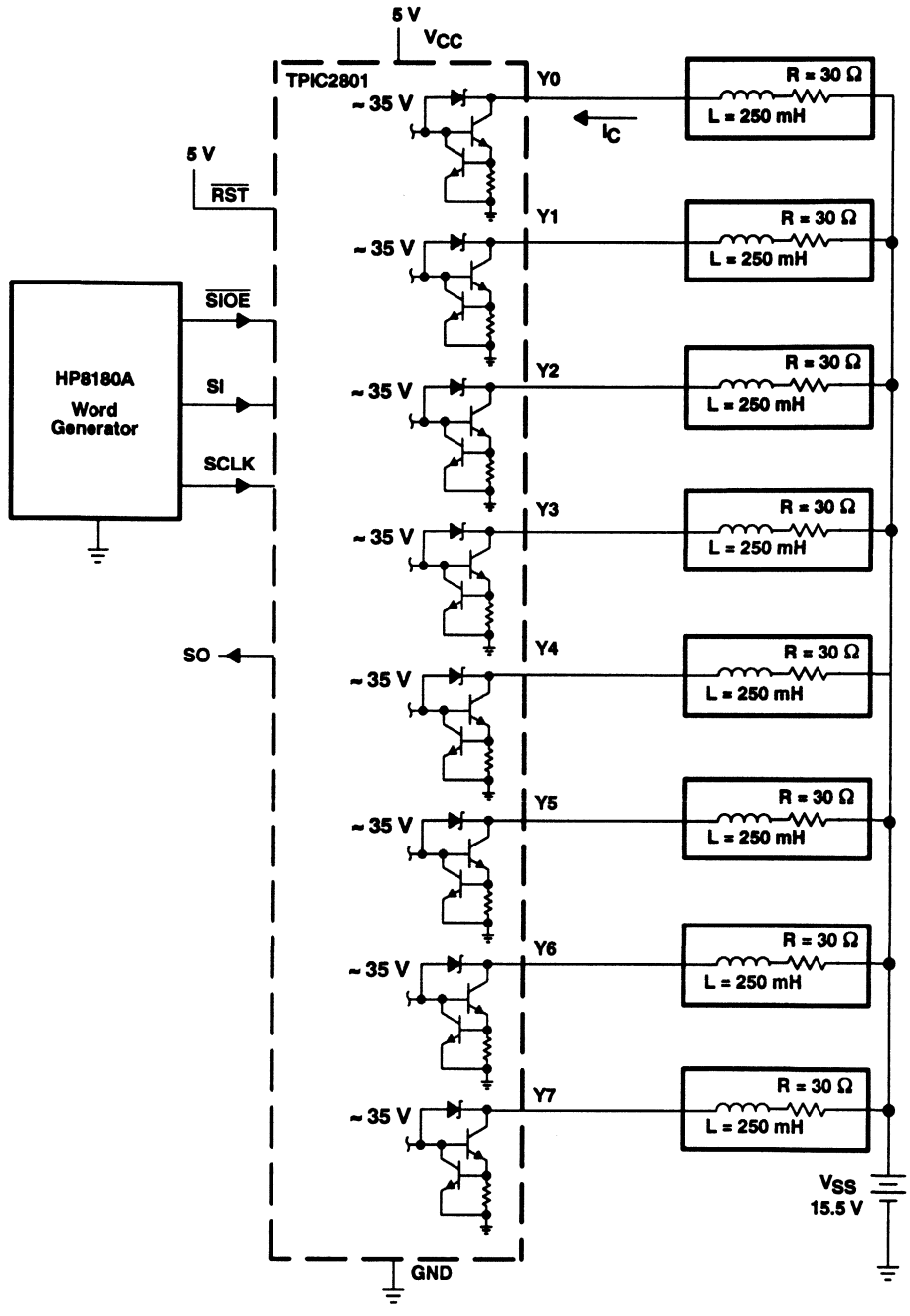
$$P_{OFF} = E_T \times f = 0.0367 \text{ J} \times 43 \text{ Hz} = 1.58 \text{ W} \quad (5)$$

Using equation (6), the calculated $P_{T(AV)}$ average total power dissipation is 14.49 W; therefore, external heat sinking is required. The energy and power calculations are as follows:

$$P_{T(AV)} = P_{OFF} \times N + P(QUIES) + P_{ON} \times d \times N \quad (6)$$
$$= 1.58 \text{ W} \times 8 + 0.25 \text{ A} \times 5 \text{ V} + 0.15 \text{ W} \times 0.5 \times 8 = 14.49 \text{ W}$$

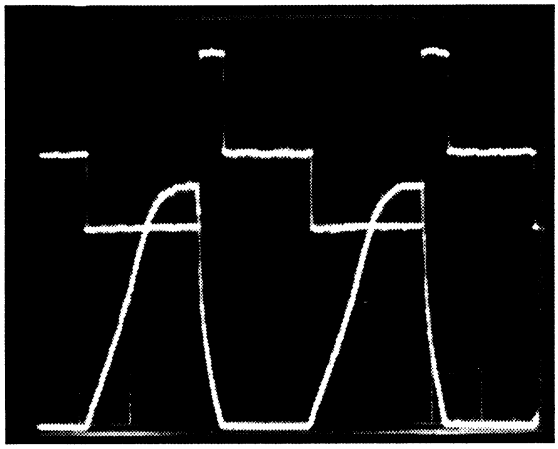
Where:

E_L	Inductive energy stopped in inductor	31.2 mJ
E_R	Energy absorbed by resistance during turn-off transient	9.9 mJ
E_S	Energy from power supply during turn-off transient	15.4 mJ
E_T	Total energy absorbed by each switch during turn-off transient	36.7 mJ
f	Switching frequency	43 Hz
d	Duty cycle	0.5
L_H	Load inductance	250 mH
I_P	Peak output load current	0.5 A
N	Number TPIC2801 switches operating	8
P_{OFF}	Turn-off power dissipation each switch	1.58 W
P_{ON}	On-state power dissipation each switch (see Figure 3)	0.15 W
P(QUIES)	Bias power dissipation	1.25 W
$P_{T(AV)}$	Average total power dissipation	14.49 W
R_L	Resistance of inductor	30 Ω
V_{OK}	Clamp voltage (measured, see Figure 11)	37 V
V_{SS}	Load supply voltage	15.5 V



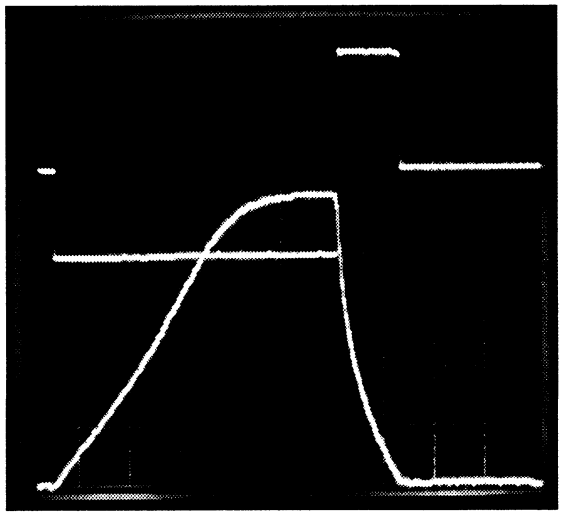
(a) SIMULTANEOUS TURN-ON/TURN-OFF CIRCUIT

Figure 11. Driving Solenoid Under Worst-Case Conditions



Horizontal = 5 ms/cm

(b) V_{CE} AND I_C WAVEFORMS OF TPIC2801 SWITCHING INDUCTIVE EIGHT HIGH-INDUCTIVE LOADS



Horizontal = 2 ms/cm

(c) EXPANDED VIEW OF V_{CE} AND I_C WAVEFORMS OF TPIC2801 SWITCHING EIGHT HIGH-INDUCTIVE LOADS

Figure 11. Driving Solenoid Under Worst-Case Conditions (continued)

Conclusion

The TPIC2801 is an intelligent-power device that contains eight 1-A/30-V self-protected low-side power switches packaged in a 15-pin single-in-line package (SIP). Control of the eight power switches is accomplished by an 8-bit parallel latch, which independently controls each of the eight power switches.

The self-protection capability of the TPIC2801 is illustrated by the design example shown in Figure 7. The current limiter limits the lamp's initial cold filament in-rush current to approximately 1.5. The output switch overvoltage shutdown circuit permits fault operation of a 100-μs delay period and then turns off the output switch if the switch output voltage still exceeds 1.5 V. These current-limited, 100-μs, soft-start bursts of power not only protect the TPIC2801, but also protect the lamp filament from an otherwise filament degrading, high in-rush current.

The capability to extend the TPIC2801 output switch 1-A load current by parallel switch operation is illustrated by the measurement data shown in Table 1. Data shows up to a 4-A load switched by eight parallel-connected output switches.

The TPIC2801 is also well suited to switch high energy unclamped inductive loads, since each of the eight power switches is equipped with an internal 35-V collector-to-base voltage clamp. To illustrate this capability, Figure 11 shows the test circuit and oscilloscope waveforms switching eight 36.7-mJ inductive loads (293.6 mJ total energy).

The self-protection features combined with the internal 35-V voltage clamps make the TPIC2801 an extremely reliable device. It is well suited to driving high energy loads requiring up to a few amperes of current in harsh environments, such as an automobile.

Acknowledgment

The author, Joe Mings, wishes to thank Ira N. Frost of the Texas Instruments Power Integrated Circuits Lab for building the circuits described in this report, as well as his valuable technical suggestions and assistance in the project.

Also, thanks is given to Dave Cotton and Arden Douce for their important technical contributions.

TPIC6595 Power+ Logic™ Eight-Bit Shift Register With Low-Side Power DMOS Switches

TEXAS INSTRUMENTS

Contents

List of Illustrations

Introduction

The TPIC6595 is a monolithic Power+ Logic™ device that contains eight 1.5-A peak/45-V low-side DMOS power switches packaged in a 20-pin dual-in-line plastic package. The logic functions of the TPIC6595 consist of the logic functions existing in the high-speed CMOS (HCMOS) SN74HC595 catalog parts except the outputs are inverted relative to the HCMOS version. The eight DMOS switches are controlled from a single input, SER IN (serial input), and by an 8-bit serial word. Data is transferred through an 8-bit shift register on the rising edge of SRCK. SER OUT is provided at the last bit of the shift register to allow cascading in applications requiring more than eight DMOS switches.

Each of the eight DMOS switches are equipped with an internal 45-V drain-to-gate zener clamp that greatly enhances their capability to switch unclamped inductive loads. Since the zener clamp causes the DMOS switch to be forward biased instead of being avalanched during inductive-load turn off, a power switch avalanche energy rating of 75 mJ maximum is achieved.

This device provides a cost-effective single-chip solution for direct control of motors, relays, solenoids, and other high-energy, high-electrical stress loads including lamps. Since the device implements a direct control link between the microcontroller and the system electrical loads, use of multiple logic integrated circuits and discrete power devices are eliminated. The reduction of discrete devices not only reduces cost, but saves circuit space and improves system reliability by the reduction of active components.

Functional Description

The TPIC6595 is an 8-bit serial-in-to-parallel-out power driver having separate power and logic ground pins. A functional block diagram is shown in Figure 1. Data is transferred through an 8-bit shift register on rising edges on SRCK. The data in the shift register is latched to the outputs by the rising edge on RCK. All outputs are placed in a high-impedance mode with a high level on $\overline{G}$, but the data is not cleared from the storage register latches. $\overline{SRCLR}$ clears all data in the shift register only. SER OUT is provided at the last bit of the shift register to allow for cascading in applications requiring more than eight output bits.

The logic used is specified within the data sheet to operate from 4.5 V to 5.5 V, but it is capable of operation down to 3 V and up to an absolute maximum voltage of 7 V. The CMOS transistors used in the digital logic have small feature sizes and short channel lengths as well as tightly controlled, low threshold voltages. Due to these characteristics, the CMOS gains are high, and the parasitic capacitance is minimized. Because of this, the logic is able to function at greater than 25-MHz operation over the full V_{CC} range of 3 V to 7 V and over the temperature range of −40°C to 125°C. Another result of using primarily CMOS-type transistors in the design of the power logic is a low quiescent current (I_{CC}).

The predrive circuitry is a CMOS buffer stage that provides adequate sink/source drive to the gate of the output power DMOS. A series resistor has been added between the buffer stage and the gate of the DMOS in order to provide a more controlled gate-drain capacitor charging current than could be achieved with a CMOS buffer alone. The current-limit resistor serves two purposes: first, it limits power dissipation in the

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drain-to-gate zener clamp structure under inductive transient conditions, and second, it controls the voltage rise and fall of the DMOS gate. This reduces radio frequency interference (RFI) during output switching. The rise and fall times at the gate are controlled by the effective RC time constant, which consists of the series resistor and the C_{iss} of the DMOS.

The DMOS outputs are designed to have a typical static drain-source on-state resistance of 1.3 Ω with a continuous output current of 250 mA at 25°C and V_{CC} of 5 V. The DMOS transistors are designed to have a low threshold voltage. The low threshold voltage along with the high gain of the devices allow the gates to be driven without the aid of any additional supply voltage above V_{CC}. Thus a charge pump or additional level shifting voltage supply is not necessary. The elimination of a charge-pump circuit reduces turn-on times, thereby minimizing power dissipation in the outputs during switching. The use of a charge pump also increases the susceptibility of generating RFI due to the need for an internal oscillator. An oscillator provides little interference due to its low power, but the DMOS may serve as a transconductance amplifier for the oscillator circuit, especially when switching small resistive loads.

Variation of the output characteristics is primarily a function of temperature and V_{CC}. With the CMOS predrive buffer used, the V_{GS} of the output DMOS varies directly with V_{CC}. A typical $r_{DS(on)}$ of 1.8 Ω at 25°C can be achieved with a V_{CC} of 3 V. This low static drain-source on-state resistance is directly attributable to the low DMOS threshold voltage in the process. Output $r_{DS(on)}$ primarily consists of the intrinsic DMOS resistance, the series resistance of the source and drain lead busing, bonding resistance, and lead frame resistance. All of these resistances have a positive temperature coefficient.

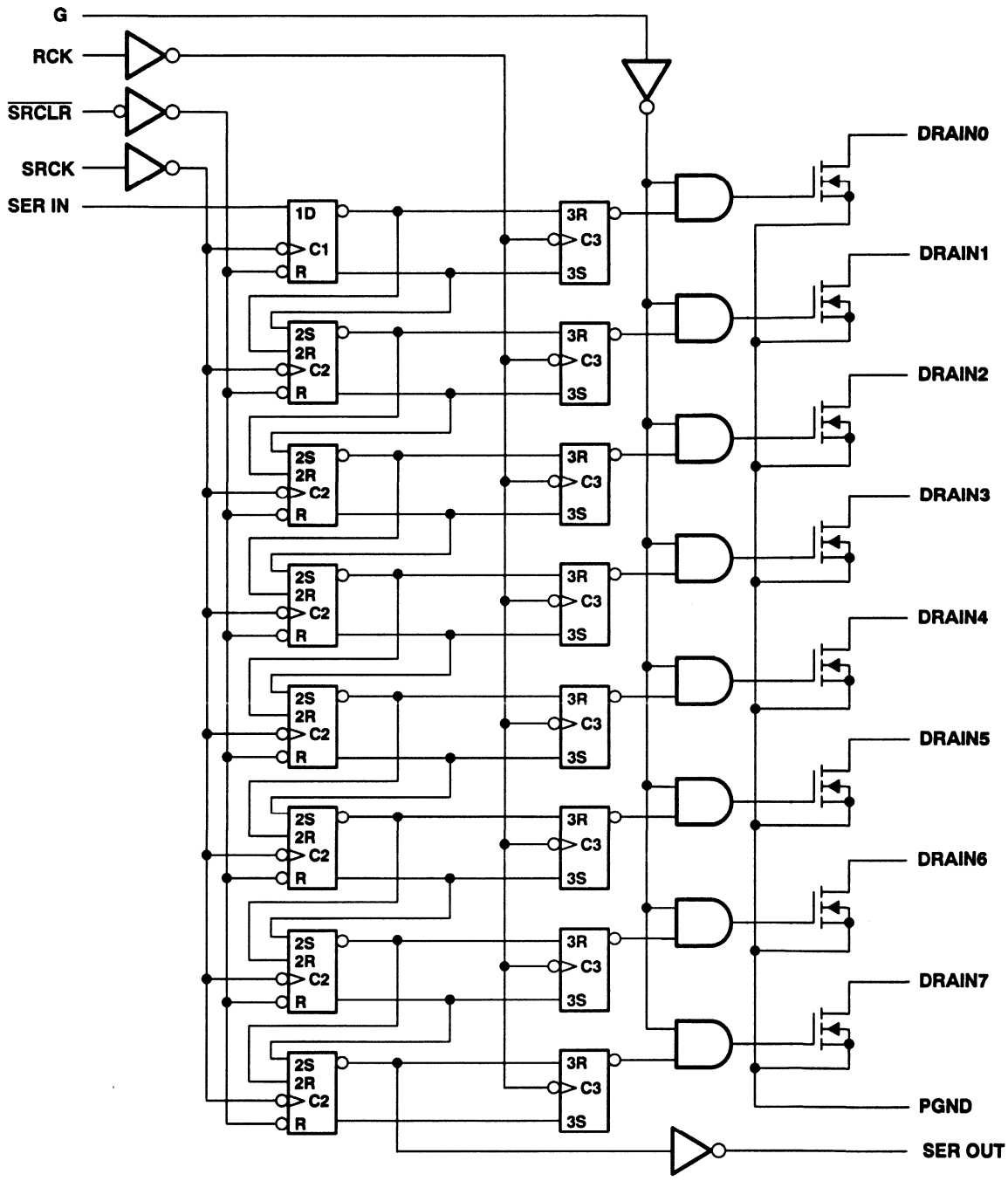


Figure 1. Functional Block Diagram

Application Design Considerations

Power and Thermal Considerations

Three important application considerations for a power device are the power, thermal, and inductive energy ratings with respect to the operational load demands. The following illustrate analytical approaches that ensure that the device is operating within these maximum ratings.

To calculate the current I_D for a single output with n outputs conducting equal current, use equation (1)

$$I_D = \sqrt{\frac{T_J - T_A}{R_{\theta JA} \times r_{DS(on)} \times 8}}\ K_n \qquad (1)$$

Where:

K_n = current coefficient for the current of a single output with n outputs simultaneously conducting equal current
$R_{\theta JA}$ = thermal resistance or junction-to-ambient, 90°C/W
$r_{DS(on)}$ = static drain-source on-state resistance at 150°C (worst case) 3.5 Ω
T_J = junction operating temperature, °C
T_A = operating ambient temperature, °C

Table 1. Values for the Current Coefficient K_n

Total Outputs On n	Current Coefficient K_n
1	2.67
2	1.95
3	1.61
4	1.40
5	1.26
6	1.50
7	1.07
8	1.00

The current coefficient values, K_n, shown in Table 1 are derived from the thermal model shown in Figure 2 and the TPIC6595 data sheet thermal resistance values.

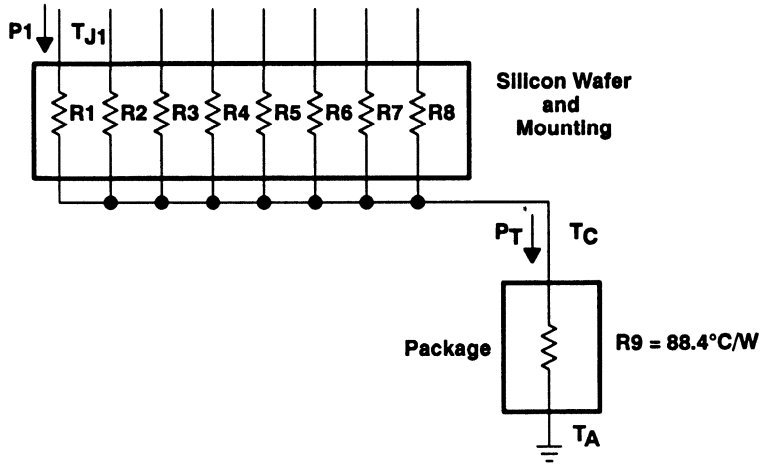


Figure 2. Thermal Model-Thermal Equilibrium, No Heat Sink

The following equations apply for the thermal model in Figure 2:

$R1 \parallel R2 \parallel R3 \parallel R4 \parallel R5 \parallel R6 \parallel R7 \parallel R8 + R9 = 90°C/W$
$R1 \parallel R2 \parallel R3 \parallel R4 \parallel R5 \parallel R6 \parallel R7 \parallel R8 = 1.6°C/W$
$R_{n,\ n = 1–8} = 12.8°C/W$
$R9 = 88.4°C/W$
$T_{J(n)}$ = junction temperature of an individual output with n outputs conducting equal current
$P1 = P2 = P3 = P4 = P5 = P6 = P7 = P8$

Therefore:

$$T_{J(n)} = P1R1 + nP1R9 + T_A$$

From the thermal model in Figure 2, P1 can be calculated using equation 1.

$$P_1 = \frac{T_{J(n)} - T_A}{R1 + nR9} = I_D^2\, r_{DS(on)} = I_D^2\, 3.5\ \Omega \qquad (2)$$

Switching Unclamped-Inductive Loads and Turn-Off Power Dissipation, P_{OFF}

The data sheet shows an energy rating of 75 mJ. This energy rating is a specific point on the curve shown in Figure 5 on the data sheet, which is repeated here as Figure 3 for clarity.

The energy capability of the device in Figure 3 is not described in a traditional manner but as a graph of peak-switching current versus avalanche time for a starting junction temperature of 25°C.

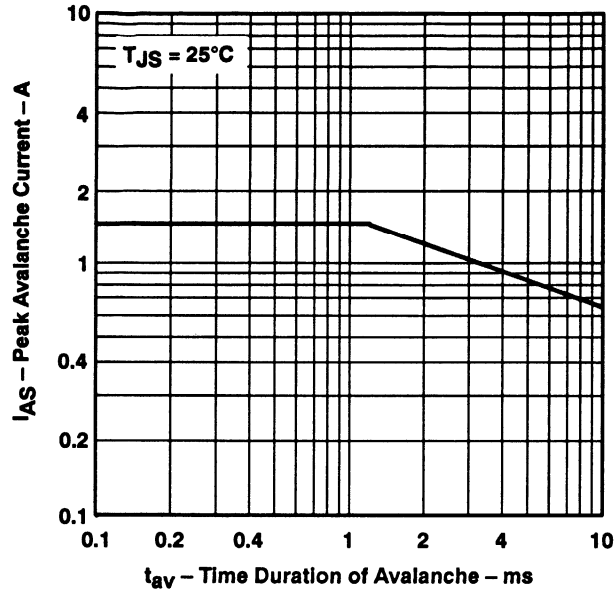


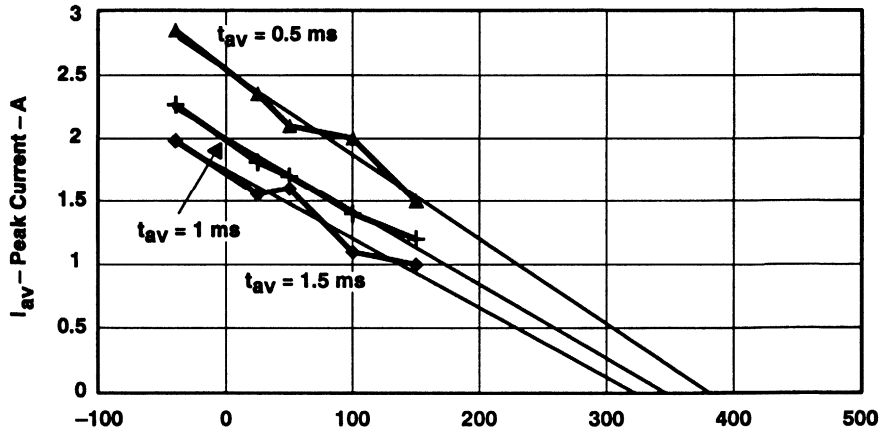
Figure 3. Peak Avalanche Current Versus Time Duration of Avalanche

It has been established that the energy limitations of these devices during inductive switching is due to the self heating of the silicon structure. Figure 4(a) shows the measurements of the peak-switching current versus starting junction temperature and idealized inductive switching waveforms. The power absorbed by the device during switching is proportional to the peak switched current, I_{av}. If the failure mechanism is thermal, the power capability of the device is related to the transient thermal impedance, starting temperature of the device, and maximum physical temperature that the silicon can withstand. It is well known[1] that for the typical resistivities used in the manufacture of these devices, the maximum temperature that silicon can operate at is in the range of 400°C. Therefore, if the peak switching temperature is plotted as a function of starting temperature, the relationship should be linear and intercept the temperature axis at 400°C. Study of Figure 4(a) shows that the 0.5-ms line has an intercept with the starting temperature axis of approximately 380°C. It can also be seen that longer pulse-width durations intercept at a lower temperature. This effect is due to self heating of the package, which has the effect of laterally translating the line. This good performance is directly attributable to the zener diode that has been integrated between the drain and the gate of the device. The zener diode forces the whole DMOS structure to be active during voltage clamping and therefore gives the maximum possible energy absorption capability.

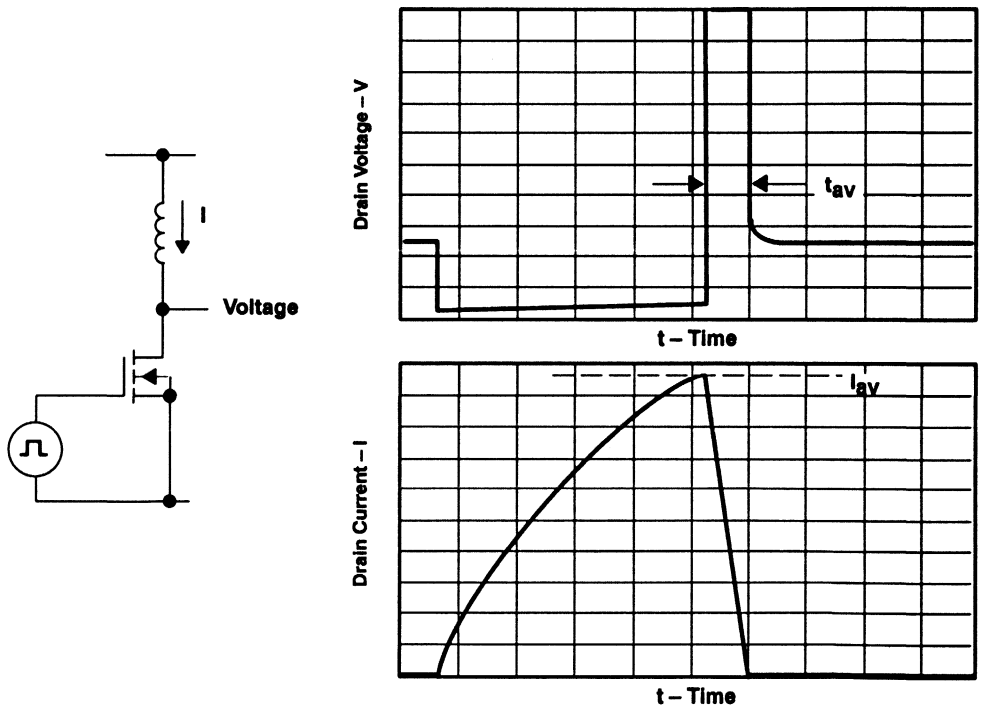
As a consequence of a thermally-limited failure mechanism, the concept of a single energy rating for the device does not fully characterize its capabilities, since the maximum energy capability is related to the time duration over which the energy is absorbed. Consequently, the inductive switching energy characterization of the TPIC6595 has been expanded to show peak switching current, I_{as}, versus avalanche time for the device, t_{av}.

The equation, $|V| = L\,di/dt$, can be used to relate this curve to a practical application circuit. Given a supply voltage, V_{DD}, and an internal clamp voltage of $V_{BR(DSX)}$ the avalanche time, t_{av}, is given by $(V_{(BR)DSX} - V_{DD})/L$, and the peak switching current I_{av} is simply the maximum current at switch off.

[1]Physics of Semiconductor Devices, Second Edition. Sze. John Wiley & Sons, pp. 19–26.



(a) PEAK SWITCHING CURRENT VERSUS JUNCTION TEMPERATURE



(b) IDEALIZED INDUCTIVE SWITCHING WAVEFORMS

Figure 4. Peak Switching Current Versus Starting Junction Temperature

If the maximum power dissipation of the device is not exceeded, it is possible to drive an inductive load by operating a number of the devices in parallel. This is due to the close matching of the gate-drain zener diodes.

Figure 5(a) shows four switches operating in parallel while driving a 105-mH/11.5-Ω load at 1 A. The power absorbed during switching is often greater than the power dissipated during the on period.

$$E_{off} = \frac{3L_H I_{DM}^2 BV_{(BR)DSX}}{\left[6(V_{(BR)DSX} - V_{DD}) + 4R_L I_{DM}\right]} \quad (3)$$

where:

E_{off}	Total energy absorbed by TPIC6595 during turn-off transient	59.6 mJ
f	Switching frequency	25 Hz
L_H	Load inductance	105 mH
I_{DM}	Peak output load current	1 A
P_{off}	Turn-off power dissipation	1.26 W
R_L	Inductor resistance	11.5 Ω
$V_{(BR)DSX}$	Clamp voltage	45 V
V_{DD}	Load supply voltage	13 V

$$P_{off} = E_{off} f = 1.49 \text{ W} \quad (4)$$

In the above example, switching frequency of only 25 Hz can result in a power dissipation that is greater than the package rating device. If it is assumed that T_A = 25°C and T_J = 150°C, the maximum power dissipation, P_{max}, is given by

$$P_{max} = (T_{Jmax} - T_A)/R_{\theta JA}$$

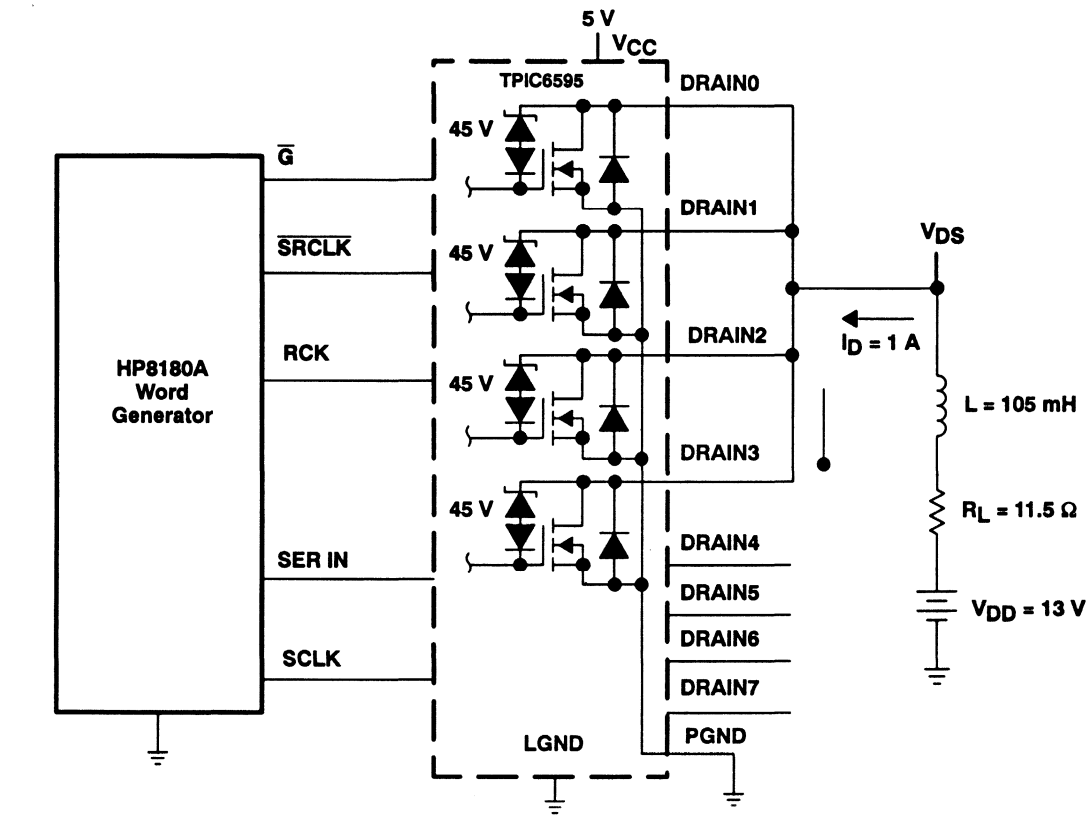
where

T_{Jmax} is the maximum junction temperature,
T_A is the ambient temperature, and
$R_{\theta JA}$ is the thermal resistance.

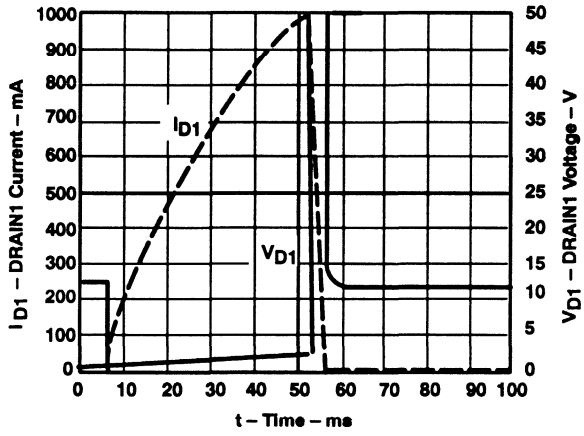
Thus

P_{max} = (150−25)/90 = 1.39 W and at a switching speed of 25 Hz,
P_{off} = 59.6 mJ × 25 Hz = 1.49 W

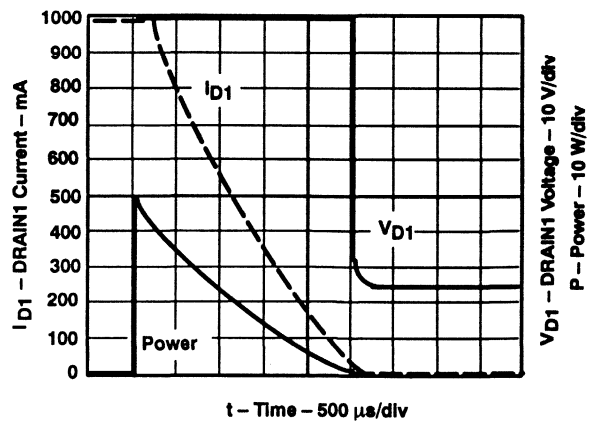
The above example demonstrates that the power dissipation associated with load turn off is often significantly greater than during the on period.



(a) POWER SWITCHES CONNECTED IN PARALLEL



(b) FULL CYCLE INDUCTIVE LOAD SWITCHING



(c) TURN-OFF INDUCTIVE LOAD SWITCHING

Figure 5. Power Switches Connected in Parallel

Parallel Operation of Output Switches for Extended Current Capability

If all eight output switches are not needed for an application and a continuous output load current greater than 0.25 A is required, the switches can be connected in parallel for extended current capability. The current-sharing capability of the switches is demonstrated in a circuit while operating at T_A = 40°C (see Figure 6). The individual switch current, I_D, is determined by equation (5).

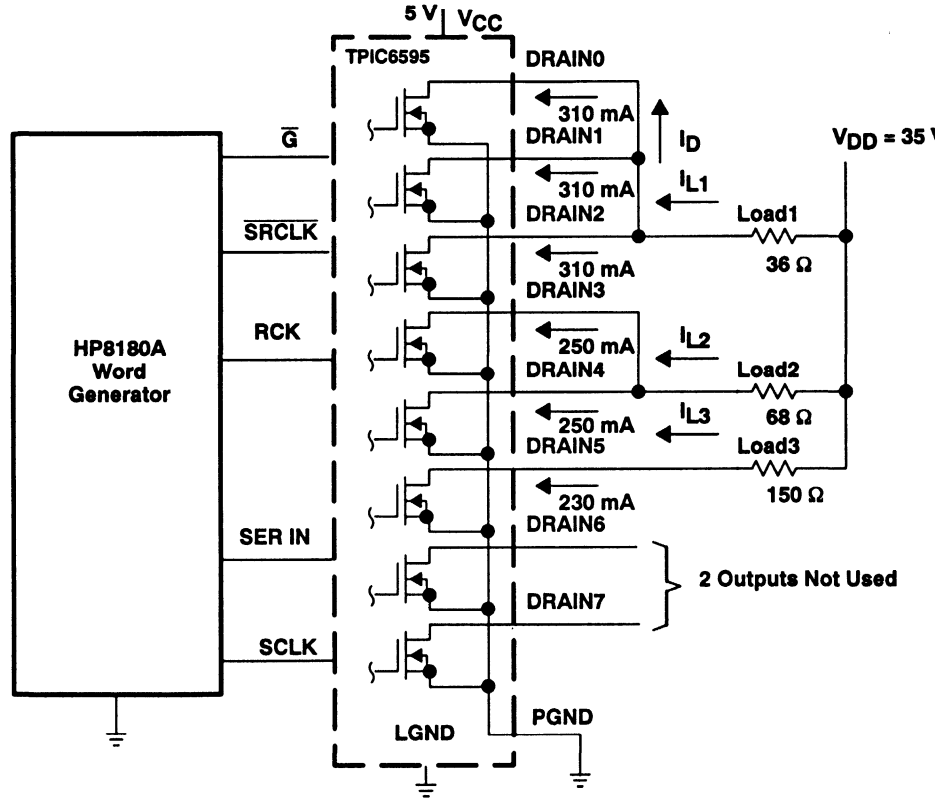


Figure 6. Parallel Operation of Output Switches for Extended Current Capability

$$I_D = \sqrt{\frac{T_J - T_A}{R_{\theta JA} \times r_{DS(on)} \times 8}}\ K_n \qquad (5)$$

K_n = current coefficient = 1.5, 6 outputs on

where:

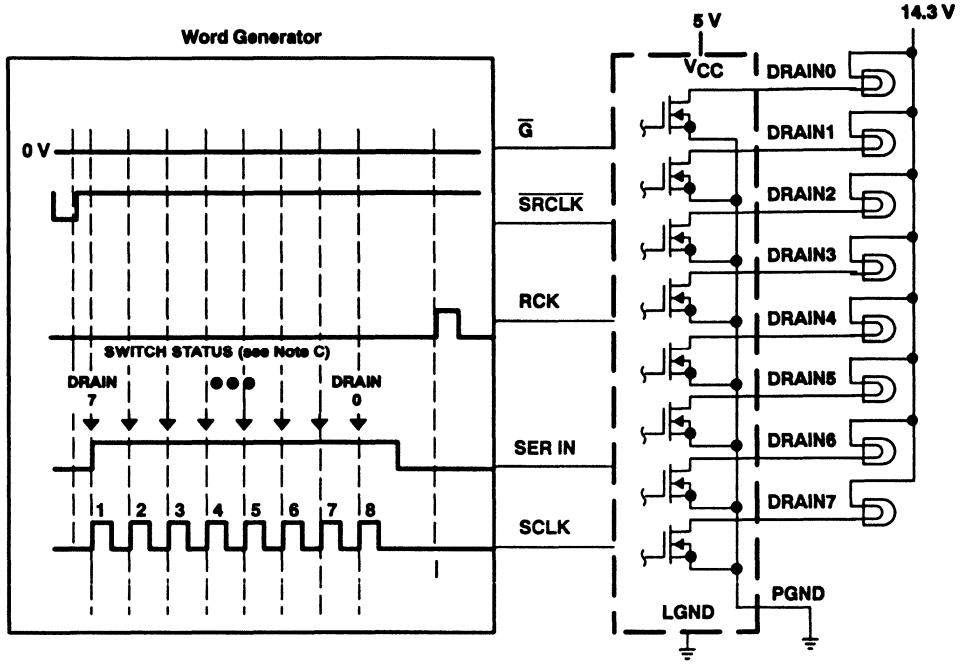
$$I_D = \sqrt{\frac{150^\circ C - 40^\circ C}{90^\circ C \times 3.5\ \Omega \times 8}}\ K_n$$

I_D = 0.209 A × 1.5 = 0.313 A each switch
I_{L1} = 3 X I_D = 0.940 A max current for Load1
I_{L2} = 2 X I_D = 0.627 A max current for Load2
I_{L3} = 1 X I_D = 0.313 A max current for Load3

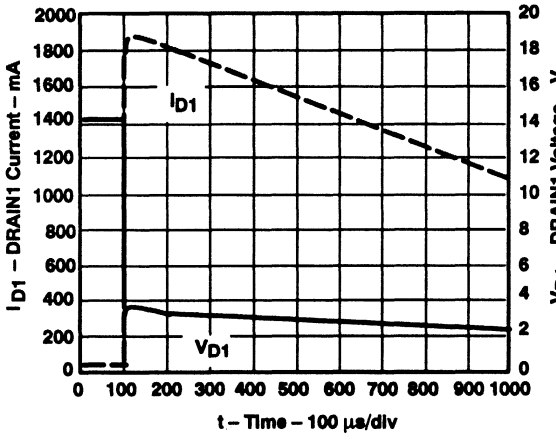
Application Design Examples

Direct Drive of Eight Lamps

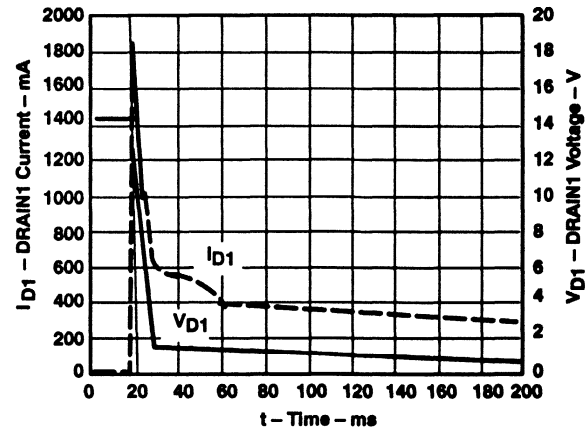
Figure 7 shows the TPIC6595 circuit simultaneously switching eight No. 194 automotive lamps from a 14.3-V source and various waveforms, which demonstrate the internal current limiting at approximately 1.8 A.



(a) LAMP-SWITCHING TEST CIRCUIT



(b) INITIAL LAMP IN-RUSH CURRENT



(c) HOT FILAMENT LAMP CURRENT

Figure 7. Simultaneous Switching of Eight Lamps

The nature of an incandescent lamp is capacitive during turn on and represents an instantaneous short circuit. Previous measurements have indicated that the in-rush current (peak switching current) of the incandescent bulbs shown in Figure 7 is typically 2.6 A. As shown on the previous page, the TPIC6595 limits this current to approximately 1.8 A.

Direct Drive of Eight Relays

The worst-case power dissipation for continuous operation of all outputs is calculated as 0.438 W based on the device measurements.

maximum $r_{DS(on)} = 3.5\ \Omega$ ($T_J = 150°C$):

$I_{rms} \approx 0.125$ A (see Figure 9)

$P = I_{rms}^2 \times r_{DS(on)} \times 8$ outputs on

$P = (0.125\ A)^2 \times 3.5\ \Omega \times 8 = 0.438$ W

The power dissipation created by inductive energy is insignificant in this case because the resistance component of the load is large compared to the inductance. Based on $R_{\theta JA} = 90°C / W$ and $T_J = 150°C$, the maximum permissible ambient operating temperature (T_J) for driving the eight relays at continuous operation is 110°C.

$$T_A = T_J - PR_{\theta JA} = 150°C - 0.438 \times 90°C = 110°C.$$

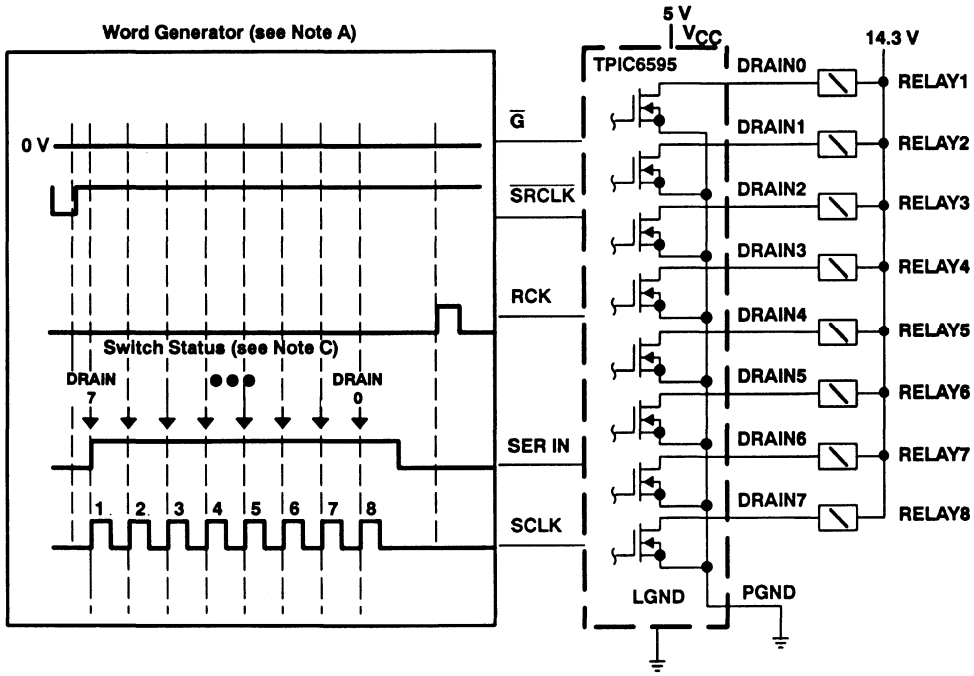


Figure 8. Simultaneous Switching of Eight 12-V, 10/20-A Relays

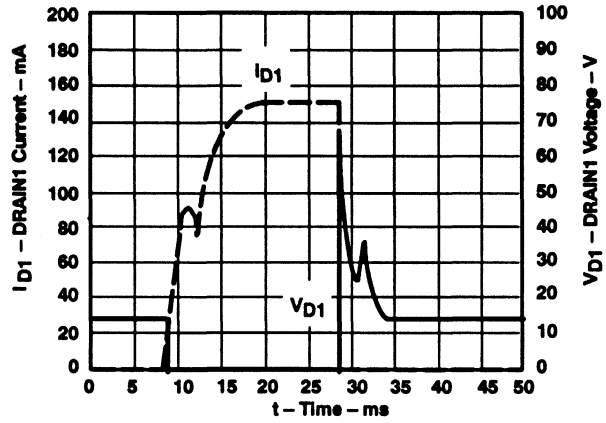


Figure 9. DRAIN1 Voltage and Current Waveforms of Figure 8 Application Circuit

Unipolar Stepper-Motor Drive

Stepping motors, due to their digital drive requirements, are natural motion providers for microprocessors or ASIC-based systems. The TPIC6595 provides a simple solution to the problem of translating logic-level timing to high-voltage and current requirements of stepping motors.

The permanent magnet stepping motor has two types of stator winding. The bipolar type has a single winding on each stator pole and uses a full bridge to drive each phase winding. In the unipolar type, the flux reversal is accomplished by individually driving a bifilar winding on each pole. The windings are phased such that when current is passed through one winding, a given flux polarity is generated. By passing current through the other winding, the opposite flux polarity is produced. The overall magnetic effect is the same as the bipolar motor, but the phase windings can be more economically driven by devices with open-drain outputs such as the TPIC6595.

Printers are one major application of stepping motors because the stepping motor is ideally matched to the needs of paper feeding. In this application, the paper is required to move in well-defined increments, which through gearing equate to fixed numbers of motor steps. Since the paper position is initialized by the user or at paper loading, there is no need for positional feedback. Therefore, the motion system is an open loop, and the paper is advanced by stepping the motor's rotor a given amount.

The system clock is set for a frequency of 4 kHz. This is based on time per motor step of 2.5 ms and a total of ten clock pulses required per each motor step. This is seen in equation (6), i.e., eight clock pulses for the data word plus one additional clock pulse before and after the data word.

$$t_{CLK} = \frac{2.5 \text{ ms/step}}{10 \text{ clock pulses step}} = 0.25 \text{ ms or } f_{CLK} = 4 \text{ kHz} \quad (6)$$

Figures 10, 11, and 12 illustrate two different techniques for driving a unipolar stepping motor with the TPIC6595. The motor is driven at its rated 1-A peak by operating two output DMOS transistors in parallel. In these examples the input logic, which would normally be provided by the system's microprocessor, is generated by a Hewlett Packard HP8180A Data Generator; the logic steps are shown in Table 2 and illustrated in Figure 10.

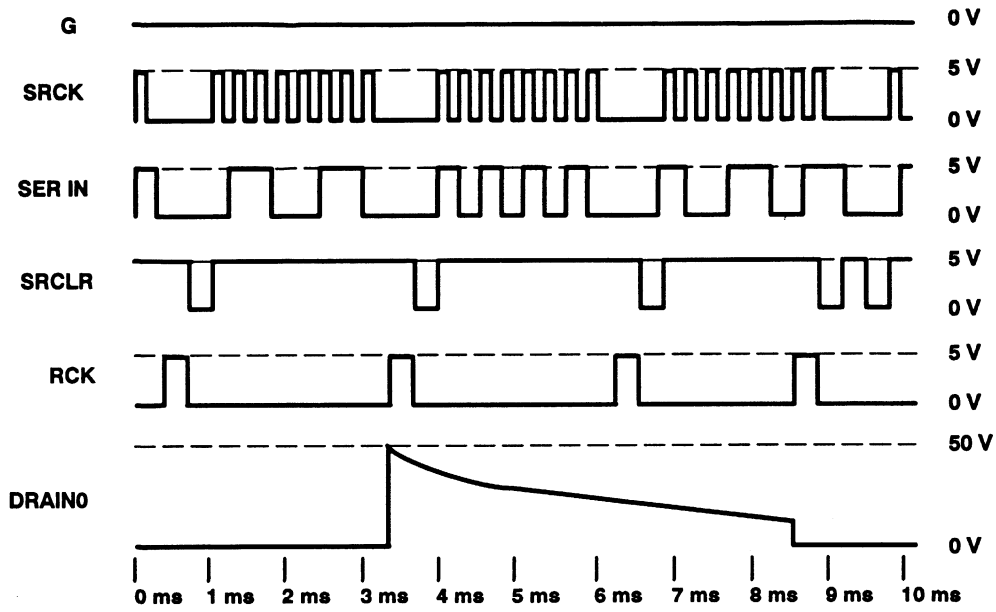


Figure 10. Logic and DRAIN0 Output Waveforms

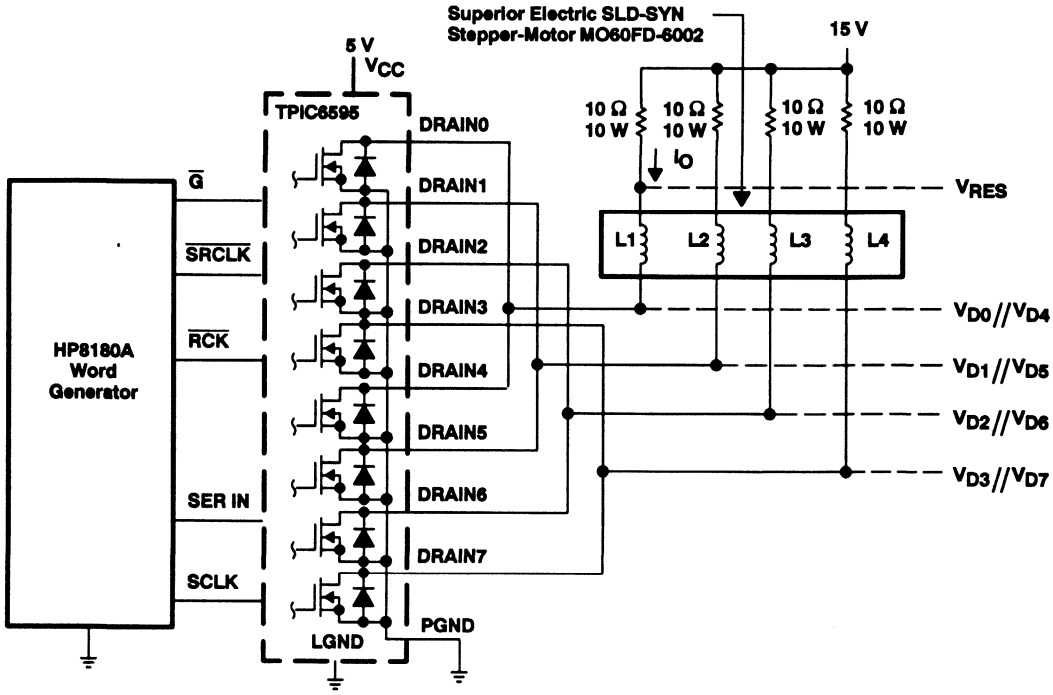
Table 2. Word Generator Program (Four-Step Sequence)

CW STEP†	SER IN INPUT DATA WORD	TPIC6595 SWITCHES ON
1	01010101	DRAIN0 | | DRAIN4, DRAIN2 | | DRAIN6
2	01100110	DRAIN1 | | DRAIN5, DRAIN2 | | DRAIN6
3	10101010	DRAIN1 | | DRAIN5, DRAIN3 | | DRAIN7
4	10011001	DRAIN0 | | DRAIN4, DRAIN3 | | DRAIN7
1	01010101	DRAIN0 | | DRAIN4, DRAIN2 | | DRAIN6

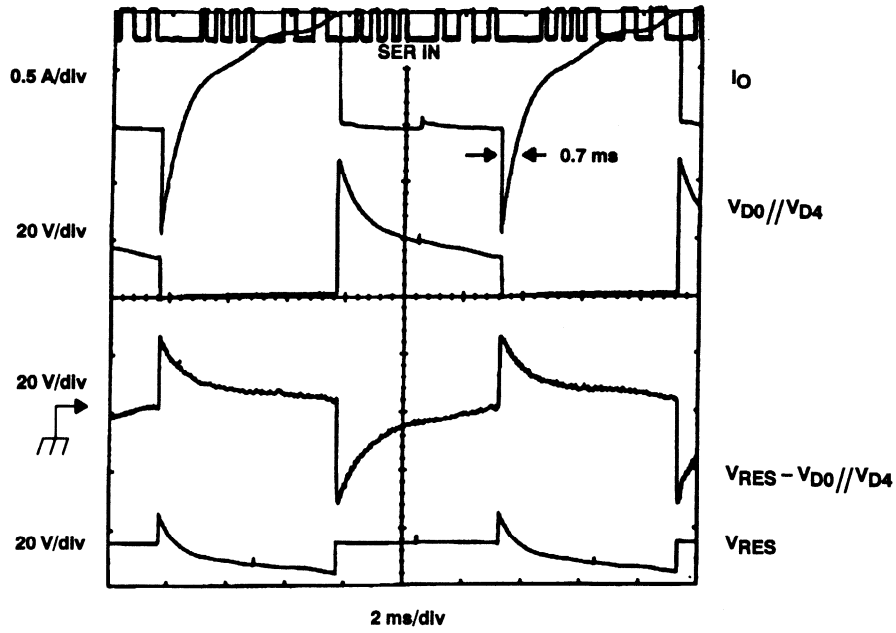
† For CCW rotation, read step sequence up from bottom.

In Figure 11(a), the construction of a stepper motor results in strong magnetic coupling between the stator windings. Consequently, a change in magnetic flux that occurs when the current in winding L1 is interrupted results in an induced current within winding L2. The timing of this motor is such that when D1 parallel with D5 are switched off, D0 parallel with D4 are switched on. The current that is induced in winding L1 is in the negative direction and first flows through the body-drain diode of the DMOS transistors, decays to zero, and then increases in a positive manner. The voltage and current waveforms are shown in Figure 11(b), where it can be seen that the decay time for the negative current is approximately 700 μs. Consequently, the nature of a stepper-motor load causes both positive and negative current to flow through the DMOS power transistor.

It is possible to block the recirculating negative current by placing a diode in series with each pole winding. This is shown in Figure 12(a). In this circuit, the drain is allowed to fly to its clamp voltage, since no current is induced in another motor pole winding. The decay time of the current is now reduced to approximately 310 μs, which is considerably faster than in the previous example. However, since the energy of the pole winding is not transferred to another pole, it must be absorbed by the DMOS transistor. The device then runs considerably warmer than in the previous case. This technique can only be used in an application that does not result in the device's thermal rating being exceeded.

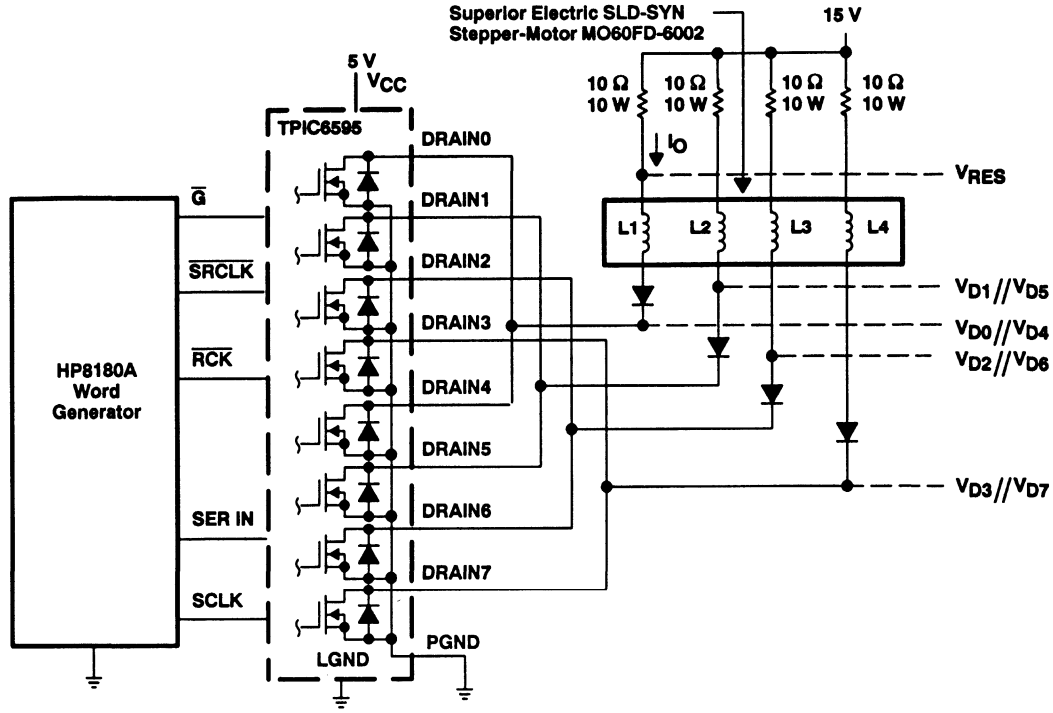


(a) MOTOR DRIVE CIRCUIT

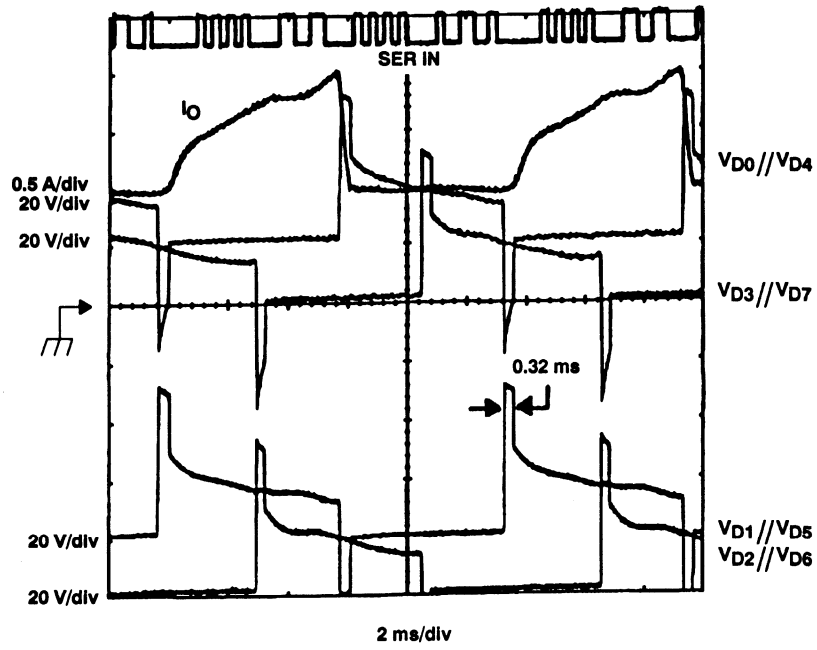


(b) VOLTAGE AND CURRENT WAVEFORMS AT NODES SHOWN IN FIGURE 11(a)

Figure 11. Unipolar Stepper-Motor Drive Circuit



(a) MOTOR DRIVE CIRCUIT



(b) VOLTAGE AND CURRENT WAVEFORM AT NODES SHOWN IN FIGURE 12(a)

Figure 12. Current and Voltage Waveforms That Occur in the Winding L1

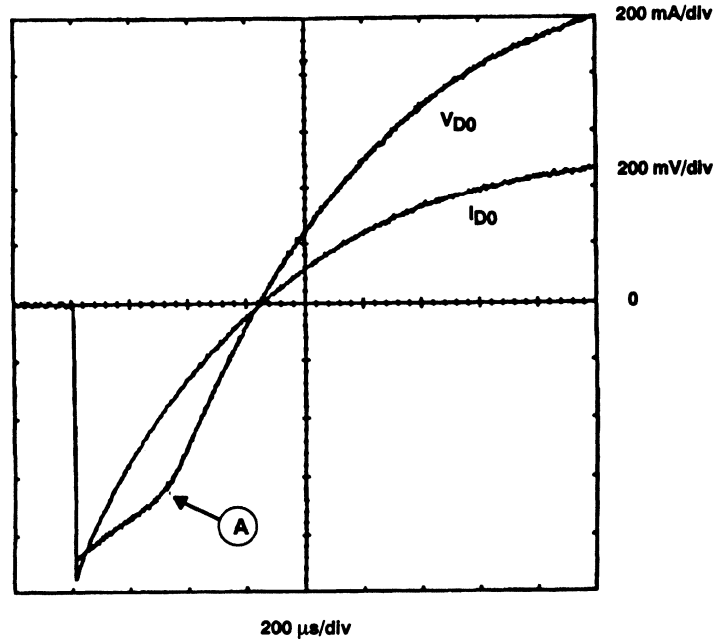


Figure 13. Expansion of Body Diode Reverse-Current Waveform From Figure 10(b)

The current waveform shown within Figure 11 shows that during each winding pulse, both negative and positive current flows through the power switch. A time expansion of the negative current flow region is given in Figure 13.

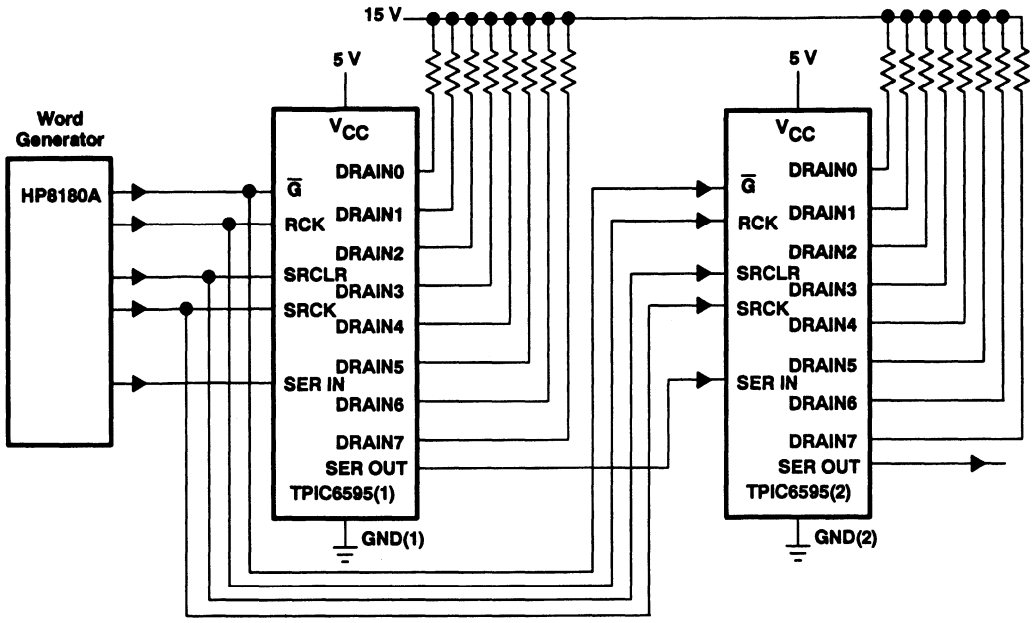
Figure 13 reveals an inflection point (denoted as point A) in the voltage waveform at approximately −700 mV. When the voltage across the device is less than 700 mV, the DMOS transistor is conducting in the reverse direction, and the power dissipation is given by the product of $R_{DS(on)}$ and the square of the drain current. When the voltage across the device is greater than 700 mV, the current flow is split between the source-drain diode and the power DMOS transistor.

A feature of power integrated circuits that is often neglected is their ability to conduct current in the reverse direction. When driving inductive loads, the body drain diode is forced to conduct in the reverse direction and the resulting current flow through this device can have effects on the integrated drive logic, causing functional problems within the device. Special consideration to these problems has been given during the design phase of the TPIC6595, and no susceptibility to this type of problem has been found to exist.

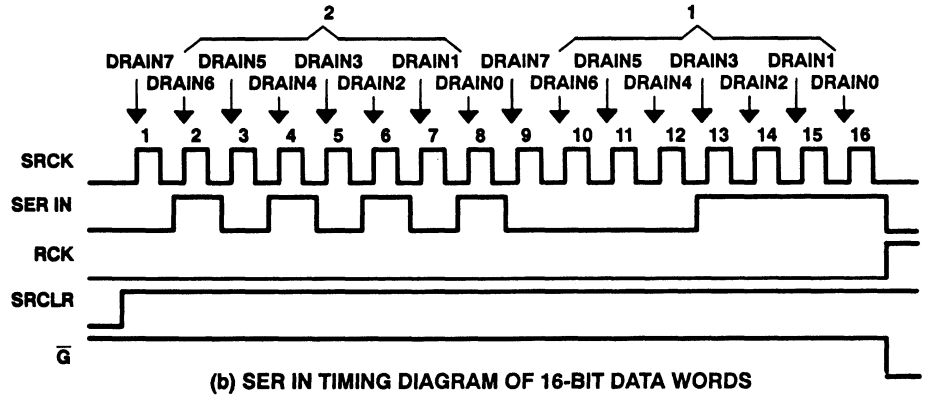
Cascade Operation of Multiple TPIC6595s

By shifting data into SER IN and out SER OUT, TPIC6595s can be connected in cascade. Figure 14 shows two TPIC6595s connected in cascade including an example SER IN timing diagram of the 16-bit data word for turning on the device number 2's output switches DRAIN6(2), DRAIN4(2), DRAIN2(2), and DRAIN0(2) and the device number 1's output switches DRAIN3(1), DRAIN2(1), DRAIN1(1), and DRAIN0(1). Also, Figure 14(b) is an oscilloscope waveform of device number 1's operation per the conditions described.

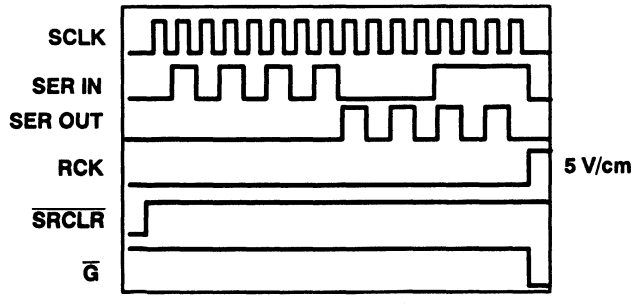
The HP8180A data generator data page for generating the example 16-bit timing diagram explained above is listed in Table 3.



(a) TWO TPIC6595s CONNECTED IN CASCADE



(b) SER IN TIMING DIAGRAM OF 16-BIT DATA WORDS



Horizontal = 20 μs/cm

(c) WAVEFORMS OF FIGURE 14(a) AND SER OUT

Figure 14. Cascade Operation of Multiple TPIC6595s

Table 3. HP8180A Data Generator Data

ADDRESS	STR	DATA (for generator outputs)				
		1–0 Out NRZ RCK	0–3 Out NRZ $\overline{\text{SRCLR}}$	0–2 Out RZ SRCK	0–1 Out NRZ $\overline{\text{G}}$	0–0 Out NRZ SER IN
0000	1	0	0	0	1	0
0001	0	0	1	0	1	0
0002	0	0	1	1	1	0
0003	0	0	1	1	1	1
0004	0	0	1	1	1	0
0005	0	0	1	1	1	1
0006	0	0	1	1	1	0
0007	0	0	1	1	1	1
0008	0	0	1	1	1	0
0009	0	0	1	1	1	1
0010	0	0	1	1	1	0
0011	0	0	1	1	1	0
0012	0	0	1	1	1	0
0013	0	0	1	1	1	0
0014	0	0	1	1	1	1
0015	0	0	1	1	1	1
0016	0	0	1	1	1	1
0017	0	0	1	1	1	1
0018	0	1	1	0	0	0

† The width is equal to 50 μs, delay 0.20 μs.
NOTE: The frequency is equal to 20 kHz.

Simultaneous Turn-on/Turn-off of Eight Inductors That Simulate Driving Solenoids Under Worst-Case Conditions

Figure 15 shows the test circuit and oscilloscope waveforms switching eight high-inductance inductors (R = 60 Ω and L = 250 mH) from a 15.6-V source. The device provides 0.25-A current to each inductor and dissipates 1.12 W as seen in equation (10), which is a safe-operating condition based on the 1.39-W continuous dissipation rating.

$$E_T = E_L + E_s - E_R = \frac{3L_H I_{DM}^2 V_{(BR)DSX}}{6\left[V_{(BR)DSX} - V_{DD}\right] + 4R_L I_{DM}} = 9\ \text{mJ} \quad (7)$$

The calculated power dissipation P_{OFF} is 1.58 W as seen in equation (5).

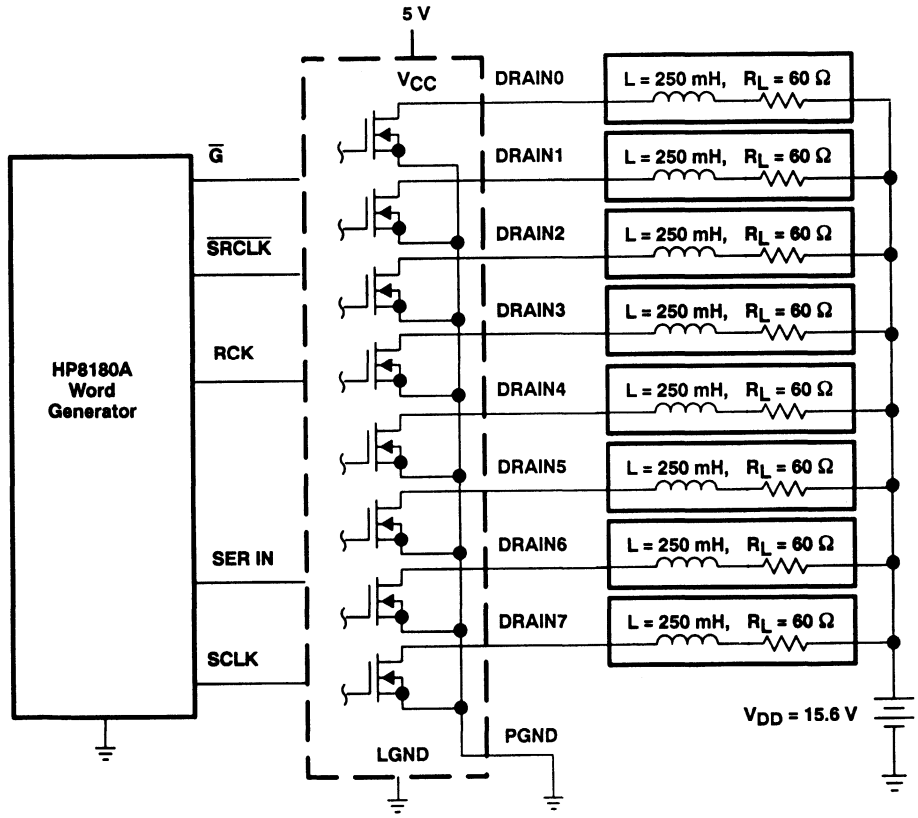
$$P_{OFF} = E_T \times f = 0.009\ \text{J} \times 10\ \text{Hz} = 0.087\ \text{W} \quad (8)$$

$$P_{ON} = I_{DM}{}^2 \times r_{DS(on)} = (0.25\ \text{A})^2\ 3.5\ \Omega = 0.219\ \text{W} \quad (9)$$

$$\begin{aligned} P_{T(AV)} &= P_{OFF} \times n + P(QUIES) + P_{ON} \times d \times n \\ &= 0.087 \times 8 + 0.0001 \times 5 + 0.219 \times 0.24 \times 8 \\ &= 1.12\ \text{W} \end{aligned} \quad (10)$$

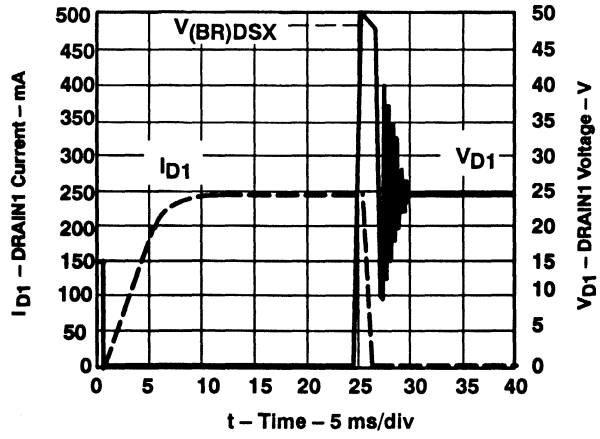
where:

E_L	Inductive energy stored in inductor	7.7 mJ
E_R	Energy absorbed by resistance during turn-off transient	1.7 mJ
E_S	Energy from power supply during turn-off transient	2.7 mJ
E_T	Total energy absorbed by each switch during turn-off transient	8.7 mJ
f	Switching frequency	10 Hz
d	Duty cycle	0.24
L_H	Load inductance	250 mH
I_{DM}	Peak output load current	0.25 A
N	Number of switches operating	8
P_{OFF}	Turn-off power dissipation each switch	0.087 W
P_{ON}	On-state power dissipation each switch (see equation 9)	0.219 W
P(QUIES)	Bias power dissipation	0 W
$P_{T(AV)}$	Average total power dissipation	1.12 W
R_L	Inductor resistance	60 Ω
$V_{(BR)DSX}$	Clamp voltage [measured, see Figure 15(b)]	50 V
V_{DD}	Load supply voltage	15.6 V
$r_{DS(on)}$	Static drain-source on-state resistance, T_J = 150°C	3.5 Ω



(a) SIMULTANEOUS TURN-ON/TURN-OFF CIRCUIT

Figure 15. Driving Solenoid Under Worst-Case Conditions



(b) SWITCHING EIGHT HIGH-INDUCTIVE LOADS

Figure 15. Driving Solenoid Under Worst-Case Conditions (continued)

Circuit Mechanical Layout Considerations

As in any application where power is being controlled by digital and/or analog signals, it is recommended that special attention be given to the circuit layout. There are a few standard layout techniques that eliminate false triggering of the logic inputs due to noise coupling from the power components. A suggested layout is given in Figure 16.

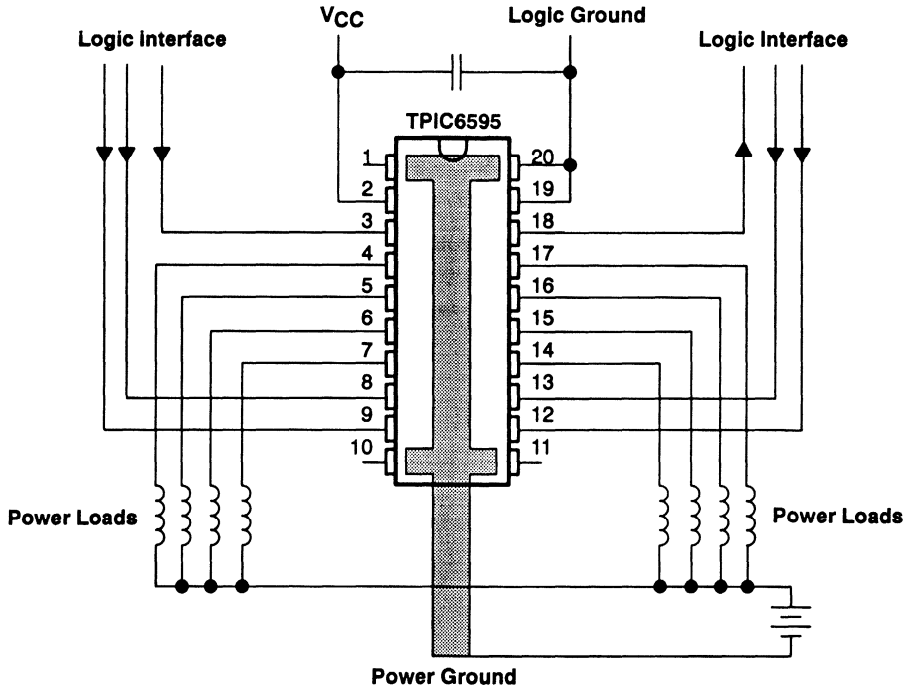


Figure 16. Mechanical Layout

A 0.1-μF ceramic bypass capacitor should be connected across V_{CC} and LGND and placed physically close to the TPIC6595.

A power ground bus should be created on the circuit board that is the return ground for the power loads. The PGNDs connect to the power ground bus.

The ground for the logic interface circuits should be routed separately from the power ground bus. The logic ground and power ground runs should tie in common at only one point; this one connection pin should be placed close to LGND.

The logic components that drive the TPIC6595 should be placed close to the IC.

Conclusion

The TPIC6595 is a monolithic power logic device that contains eight 1.5-A peak/45-V low-side DMOS power switches packaged in a 20-pin double-in-line plastic package (DIP). Control of the eight power switches is accomplished from a single input by an 8-bit serial word that independently controls each of the eight power switches. All inputs accept standard TTL- and CMOS-logic levels.

The TPIC6595 is a cost-effective single-chip solution for direct control of motors, relays, solenoids, and other high-energy, high-electrical stress loads. Since the device implements a direct control link between the microcontroller and the system electrical loads, use of multiple logic ICs and discrete power devices are eliminated. The reduction of discrete devices not only reduces cost but saves circuit space and improves system reliability by the reduction of active components.

Acknowledgment

The authors Joe Mings and Dave Cotton wish to acknowledge the contribution of Ross Teggatz and Joe Devore for the report section Functional Description, to Dale Skelton for the section Circuit Mechanical Layout Considerations, and to Ken Echelberger for building the application circuits described and preparing report artwork.

Contents

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as shown in the following example.

Example: **TL** **598M** **J** **/883B**

Prefix

MUST CONTAIN TWO OR THREE LETTERS

SN ..... TI Special Functions or Interface Products
TL, TLE ..... TI Linear Products
TLC ..... TI Linear Silicon-Gate CMOS Products

STANDARD SECOND-SOURCE PREFIXES

AD ..... Analog Devices
ADC, LF, LM, LP, or MP ..... National
LT or LTC ..... Linear Technology
MC ..... Motorola
NE, SA, or SE ..... Signetics
OP ..... PMI
RC, RM, or RV ..... Raytheon
uA ..... Fairchild/National
UC ..... Unitrode

Unique Circuit Description Including Temperature Range

MUST CONTAIN TWO OR MORE CHARACTERS
(From Individual Data Sheets)

Examples: 10 34070
592 1451AC
7757 2217-285

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DB, DW, FD, FK, FN, HS, J, JD, JG, KC, KK, KV, LP, N, NE, NS, NT, NW, P, PK, PW, U, W
(From Pin-Connection Diagrams on Individual Data Sheet)

MIL-STD-883B, Method 5004, Class B

Omit /883B When Not Applicable

ORDERING INSTRUCTIONS

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (J, JD, JG, N, NT, NS, NW, P)
– A-Channel Antistatic or Conductive Plastic Tubing

Small Outline (D, DW)
– Tape and Reel
– Antistatic or Conductive Plastic Tubing

Quad Flatpack (HS)
– Antistatic or Conductive Plastic Trays

Shrink Small-Outline (DB)
– Tape and Reel
Thin Shrink Small-Outline (PW)
– Tape and Reel

Chip Carriers (FD, FK, FN)
– Antistatic or Conductive Plastic Tubing

Flat (U, W)
– Milton Ross Carriers

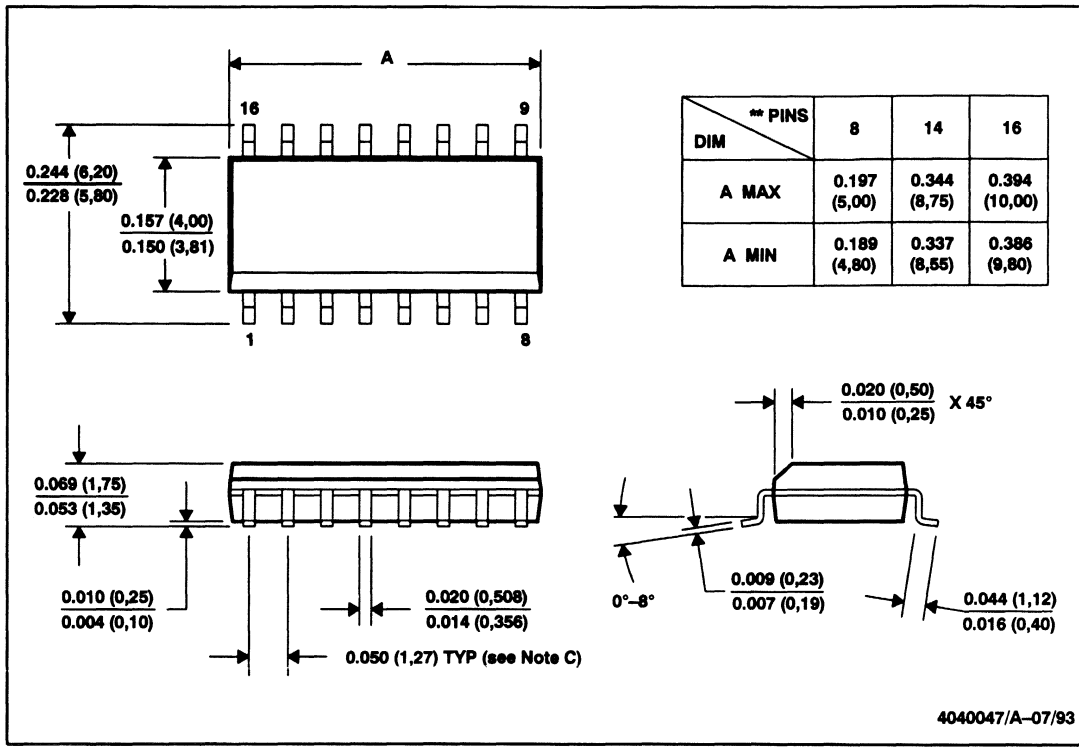
Plug-In (LP)
– Plastic Bag
– Tape and Reel

Power Tab (KC, KK, KV)
– A-Channel Antistatic or Conductive Plastic Tubing

D/R-PDSO-G**

PLASTIC NARROW-BODY SMALL-OUTLINE PACKAGE

16-PIN SHOWN

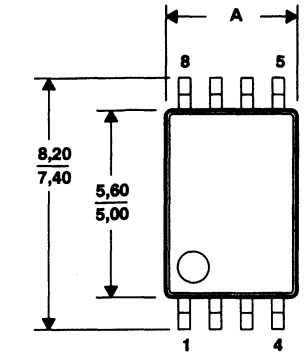


DIM \ ** PINS	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

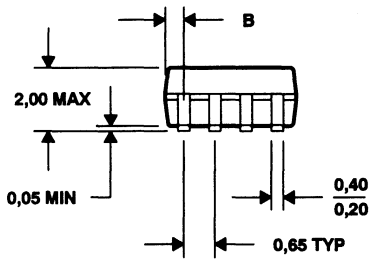
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,127) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold protrusion shall not exceed 0.006 (0,15).
F. Maximum deviation from coplanarity is 0.004 (0,10).

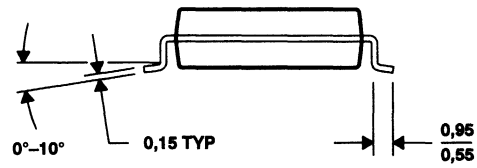
DB/R-PDSO-G** **PLASTIC SMALL-OUTLINE PACKAGE**

8-PIN SHOWN



DIM \ ** PINS	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30
B MAX	0,68	1,30	0,98	0,83	0,68	1,03	0,70	0,60



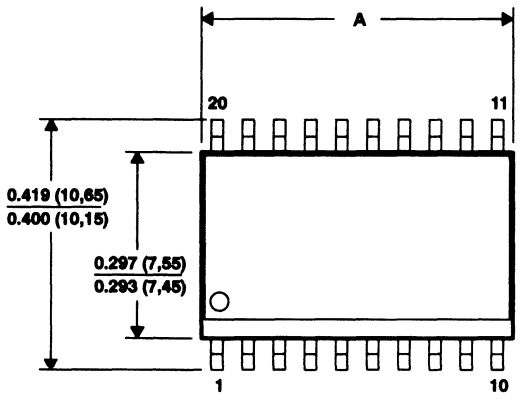


4040065/A–07/93

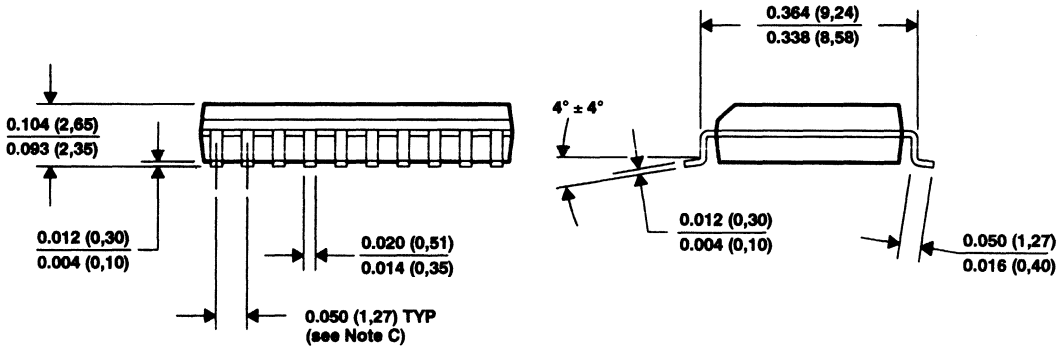
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

DW/R-PDSO-G**
20-PIN SHOWN

PLASTIC WIDE-BODY SMALL-OUTLINE PACKAGE



DIM \ ** PINS	16	20	24	28
A MIN	0.400 (10,16)	0.500 (12,70)	0.602 (15,29)	0.696 (17,68)
A MAX	0.408 (10,36)	0.508 (12,90)	0.610 (15,49)	0.704 (17,88)



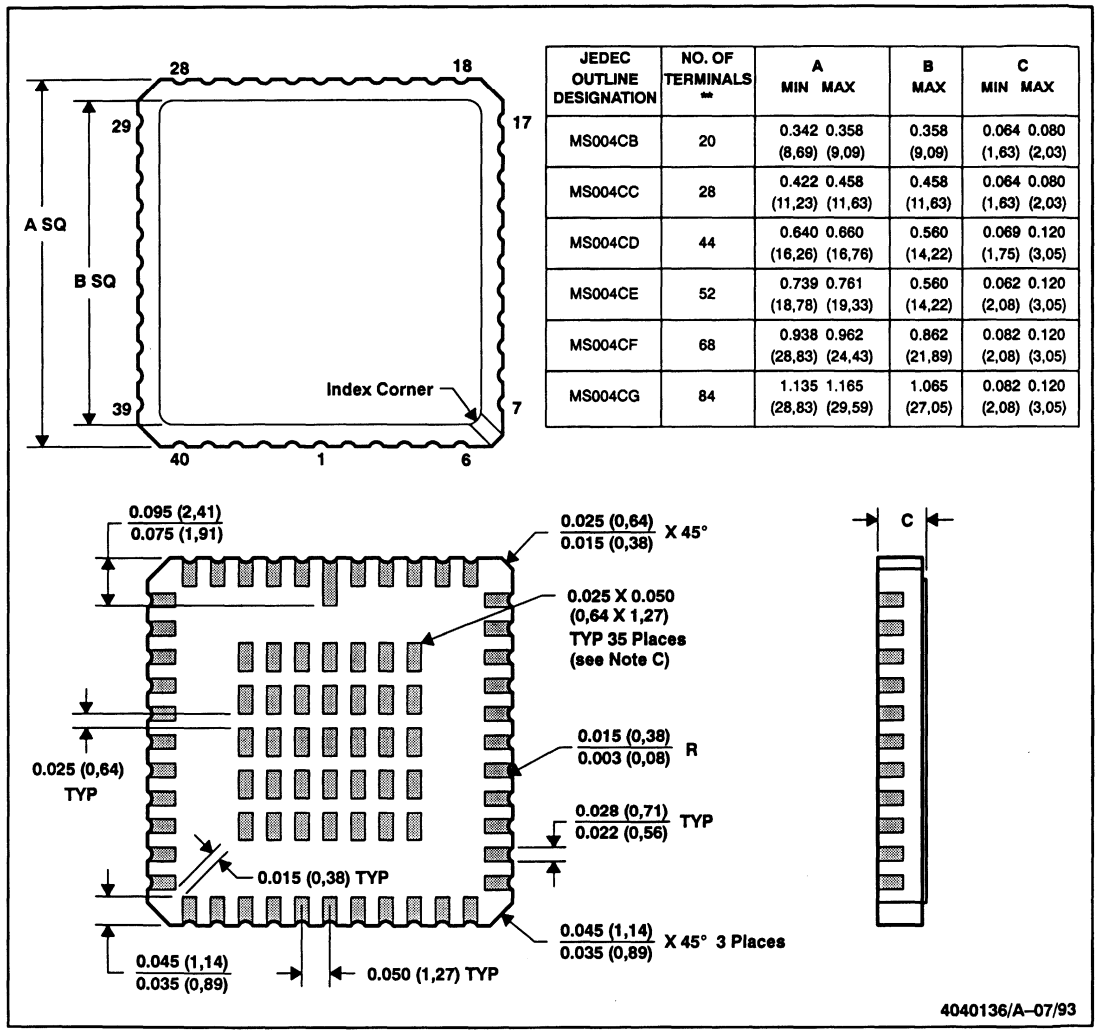
4040000/A–07/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.10 (0,25) radius of true postion at maximum material condition.
D. Body dimensions do not include mold flash or protrusion.
E. Mold flash or protrusion shall not exceed 0.006 (0,15).
F. Lead tips coplanar within ±0.004 (±0,10) exclusive of solder.

FD/S-CQCC-N**

LEADLESS CERAMIC CHIP-CARRIER PACKAGE

44-TERMINAL PACKAGE SHOWN



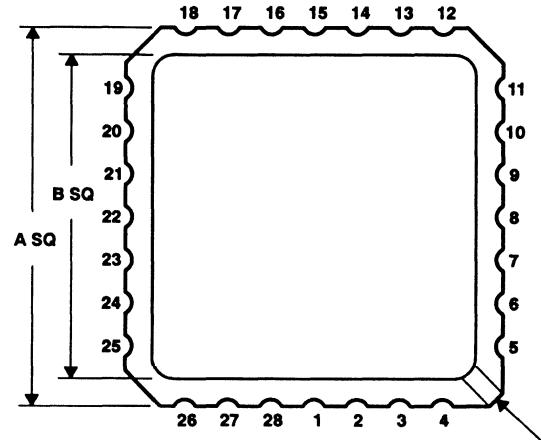
JEDEC OUTLINE DESIGNATION	NO. OF TERMINALS **	A MIN	A MAX	B MAX	C MIN	C MAX
MS004CB	20	0.342 (8,69)	0.358 (9,09)	0.358 (9,09)	0.064 (1,63)	0.080 (2,03)
MS004CC	28	0.422 (11,23)	0.458 (11,63)	0.458 (11,63)	0.064 (1,63)	0.080 (2,03)
MS004CD	44	0.640 (16,26)	0.660 (16,76)	0.560 (14,22)	0.069 (1,75)	0.120 (3,05)
MS004CE	52	0.739 (18,78)	0.761 (19,33)	0.560 (14,22)	0.062 (2,08)	0.120 (3,05)
MS004CF	68	0.938 (28,83)	0.962 (24,43)	0.862 (21,89)	0.082 (2,08)	0.120 (3,05)
MS004CG	84	1.135 (28,83)	1.165 (29,59)	1.065 (27,05)	0.082 (2,08)	0.120 (3,05)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The checkerboard pattern is aligned vertically with the contact pads and is symmetrical horizontally as shown.

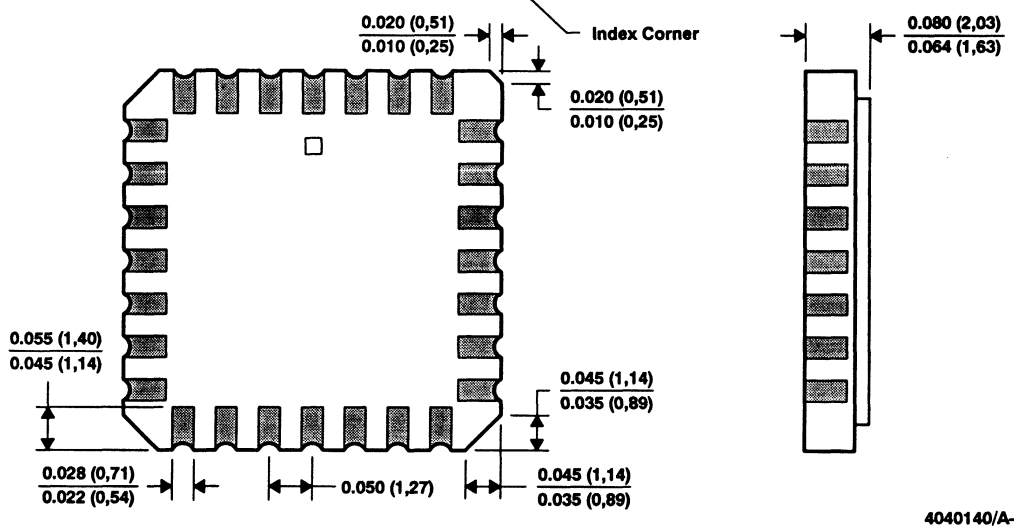
FK/S-CQCC-N**

28-PIN SHOWN

CERAMIC CHIP-CARRIER PACKAGE



JEDEC OUTLINE DESIGNATION	NUMBER OF ** TERMINALS	A		B	
		MIN	MAX	MIN	MAX
MS004CB	20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
MS004CC	28	0.422 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
MS004CD	44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
MS004CE	52	0.730 (18,78)	0.761 (19,32)	0.485 (12,58)	0.560 (14,22)
MS004CF	68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
MS004CG	84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



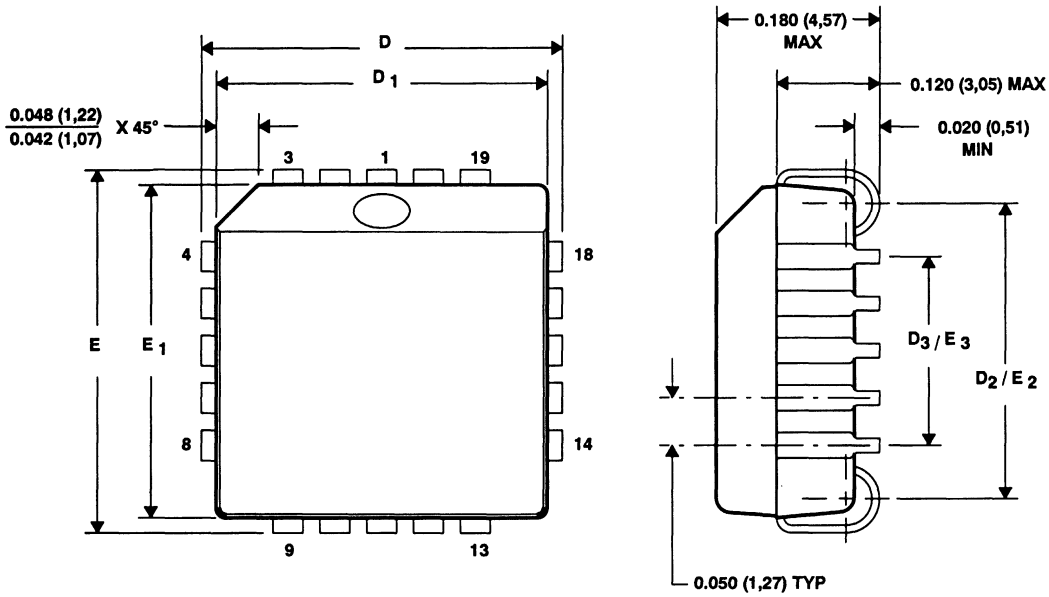
4040140/A–07/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Three-layer ceramic base with a metal lid and braze seal
D. FK package terminal assignments conform to JEDEC Standards 1, 2, and 11.
E. The packages are intended for surface mounting on solder lands on 0.050 (1,27) centers.

FN/S-PQCC-J **

PLASTIC J-LEADED CHIP-CARRIER PACKAGE

20-PIN SHOWN

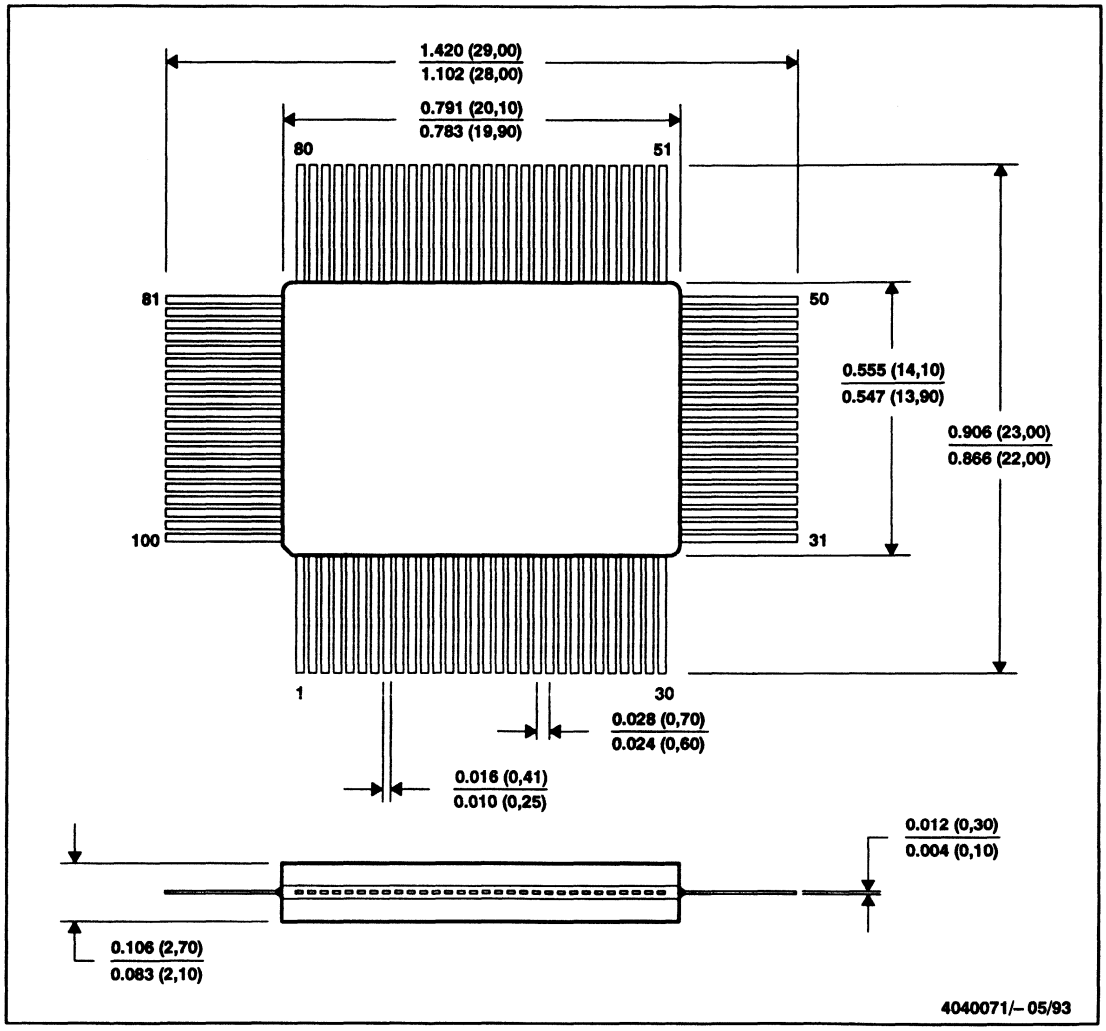


JEDEC OUTLINE	** NO. OF PINS	D / E		D_1 / E_1		D_2 / E_2		D_3 / E_3
		MIN	MAX	MIN	MAX	MIN	MAX	TYP
MO-047AA	20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.290 (7,34)	0.330 (8,38)	0.200 (5,08)
MO-047AB	28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.390 (9,91)	0.430 (10,92)	0.300 (7,62)
MO-047AC	44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.590 (14,99)	0.630 (16,00)	0.500 (12,70)
MO-047AD	52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.690 (17,53)	0.730 (18,54)	0.600 (15,24)
MO-047AE	68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.956 (24,28)	0.890 (22,61)	0.930 (23,62)	0.800 (20,32)
MO-047AF	84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	1.090 (27,69)	1.130 (28,70)	1.000 (25,40)

4040005/A–07/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0.010 (0,25) on any side.
D. All dimensions conform to JEDEC Specification MO-047.
E. Maximum deviation from coplanarity is 0.004 (0,10).

HS/R-GQFP-F100 **CERAMIC QUAD FLAT PACKAGE**

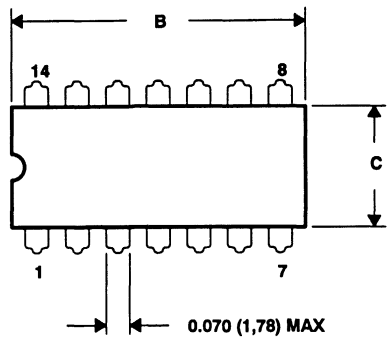


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

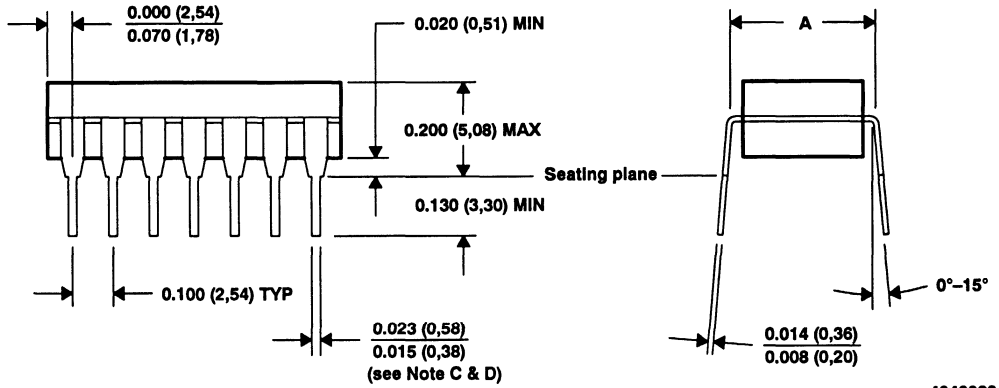
J/R-GDIP-T**

CERAMIC DUAL-IN-LINE PACKAGE

14-PIN SHOWN



DIM \ ** PINS	14	16	18	20	22
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.410 (10,41)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.390 (9,91)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)	1.100 (28,00)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)	—
C MAX	0.280 (7,11)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.388 (9,65)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	—



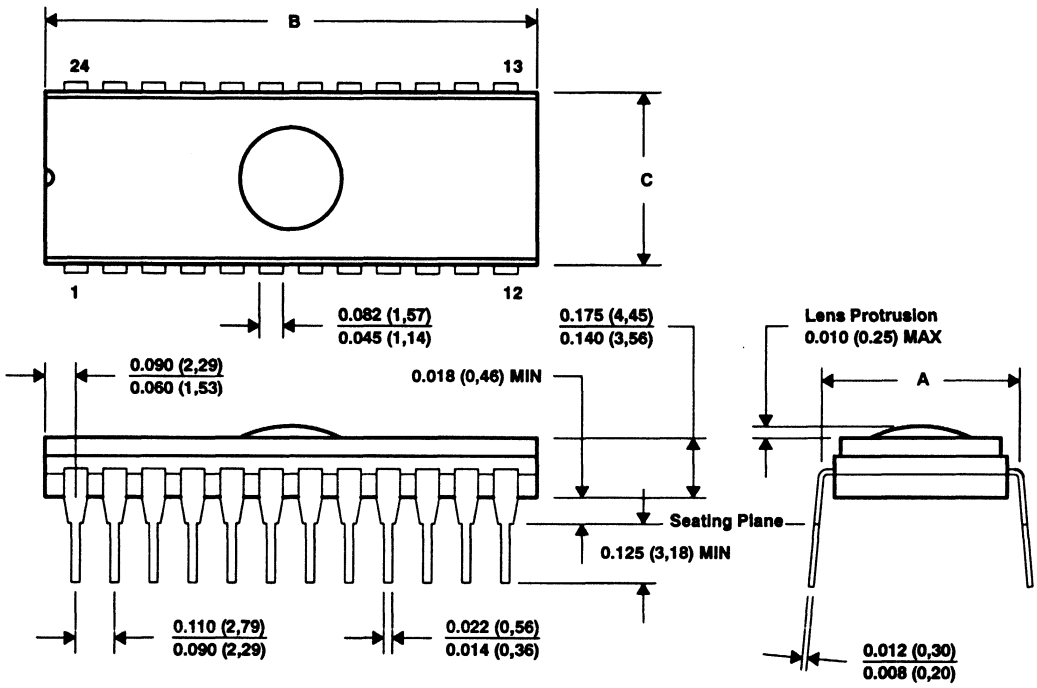
4040083/A–07/93

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This dimension does not apply for solder-dipped leads.
D. For solder-dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0.51) above seating plane.

J/R-CDIP-T**

600-MIL CERAMIC DUAL-IN-LINE PACKAGE

24-PIN SHOWN



DIM	PINS	24 NARR	24 WIDE	28 NARR	28 WIDE	32 NARR	32 WIDE	40 NARR	40 WIDE
A	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
B	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
C	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

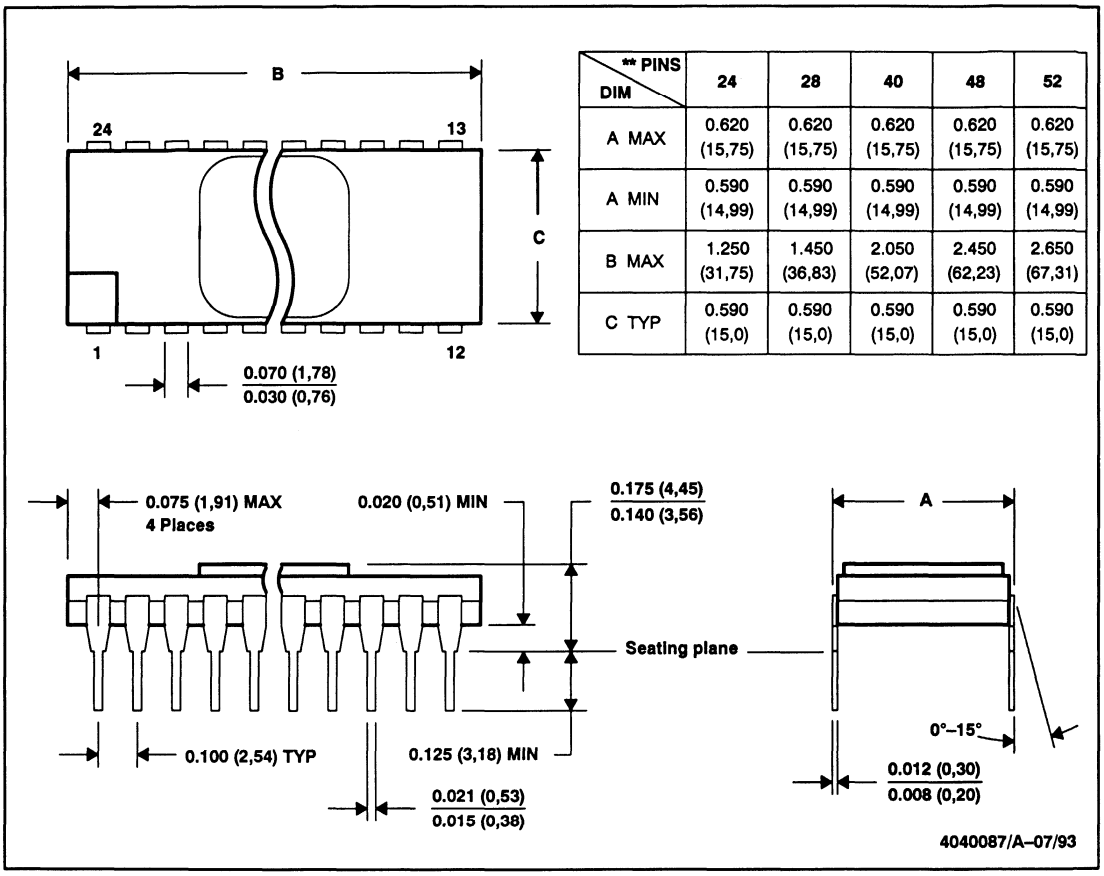
4040084/A–07/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

JD/R-CDIP-T**

600-MIL CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

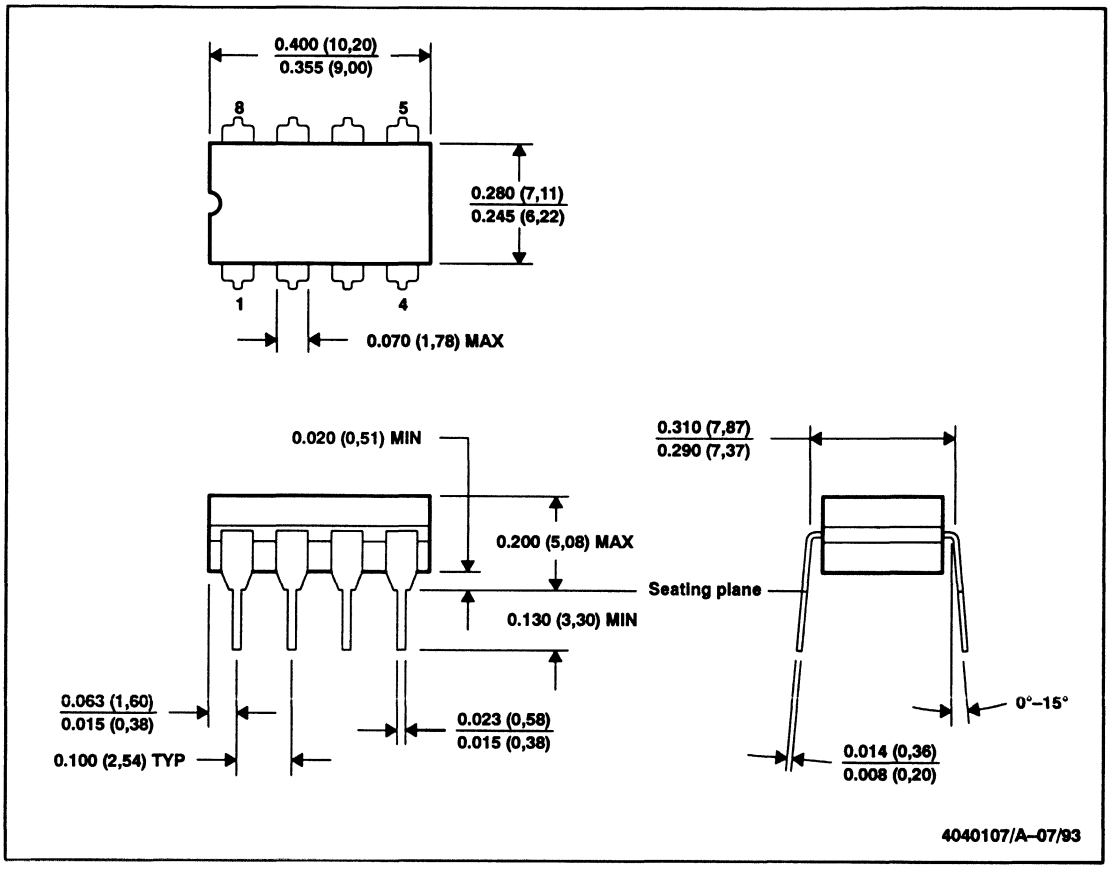
24-PIN SHOWN



DIM \ ** PINS	24	28	40	48	52
A MAX	0.620 (15,75)	0.620 (15,75)	0.620 (15,75)	0.620 (15,75)	0.620 (15,75)
A MIN	0.590 (14,99)	0.590 (14,99)	0.590 (14,99)	0.590 (14,99)	0.590 (14,99)
B MAX	1.250 (31,75)	1.450 (36,83)	2.050 (52,07)	2.450 (62,23)	2.650 (67,31)
C TYP	0.590 (15,0)	0.590 (15,0)	0.590 (15,0)	0.590 (15,0)	0.590 (15,0)

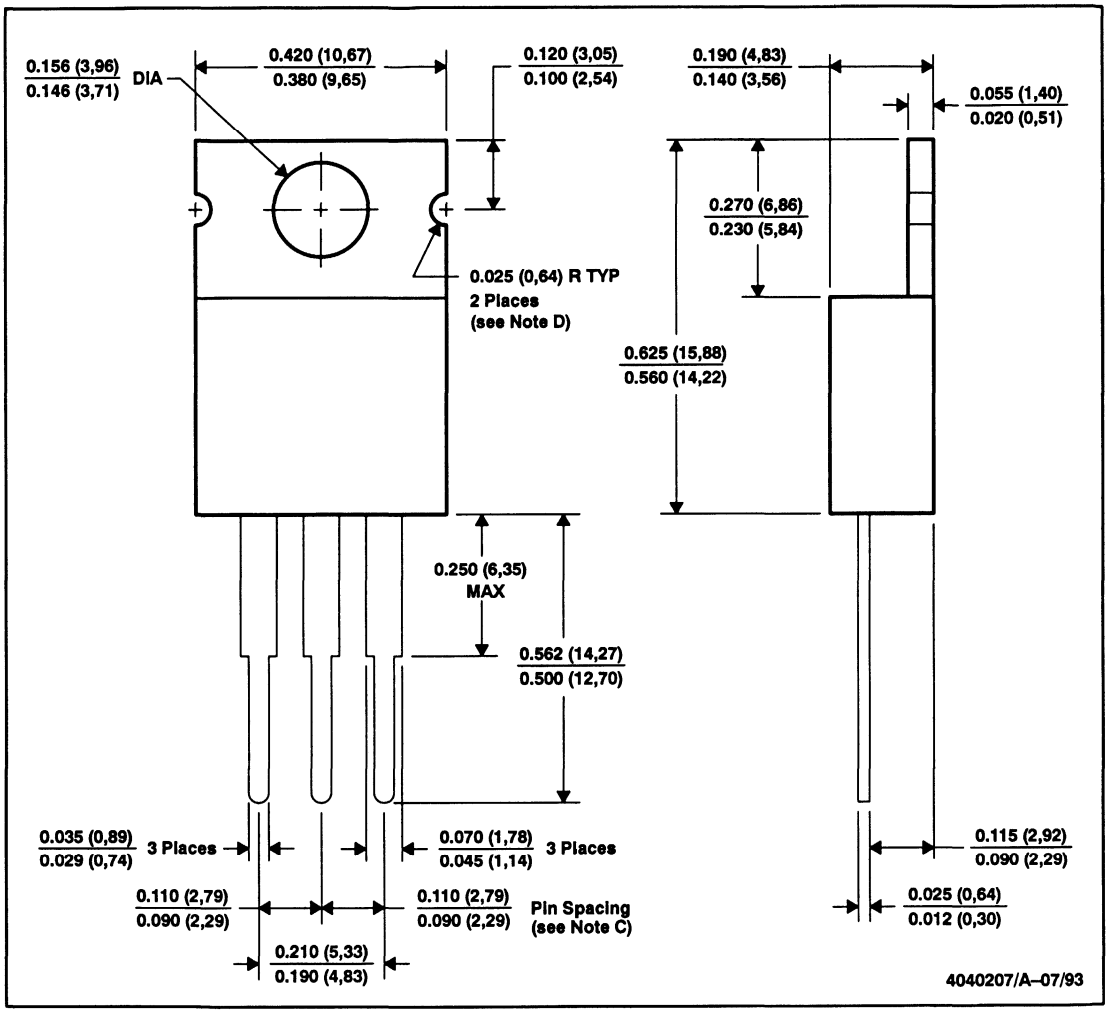
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

JG/R-GDIP-T8 **CERAMIC DUAL-IN-LINE PACKAGE**



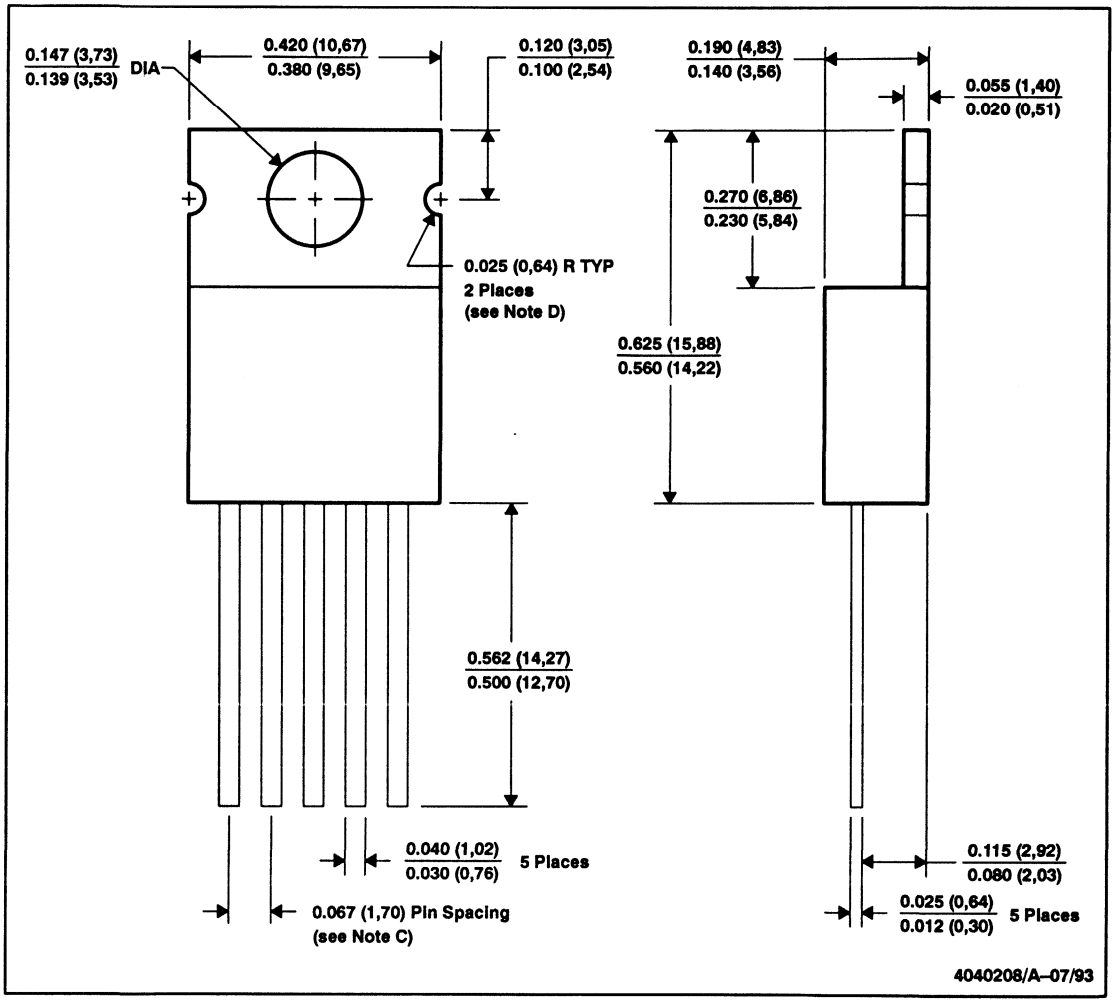
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is glass sealed.

KC/R-PSFM-T3 **PLASTIC FLANGE-MOUNT PACKAGE**



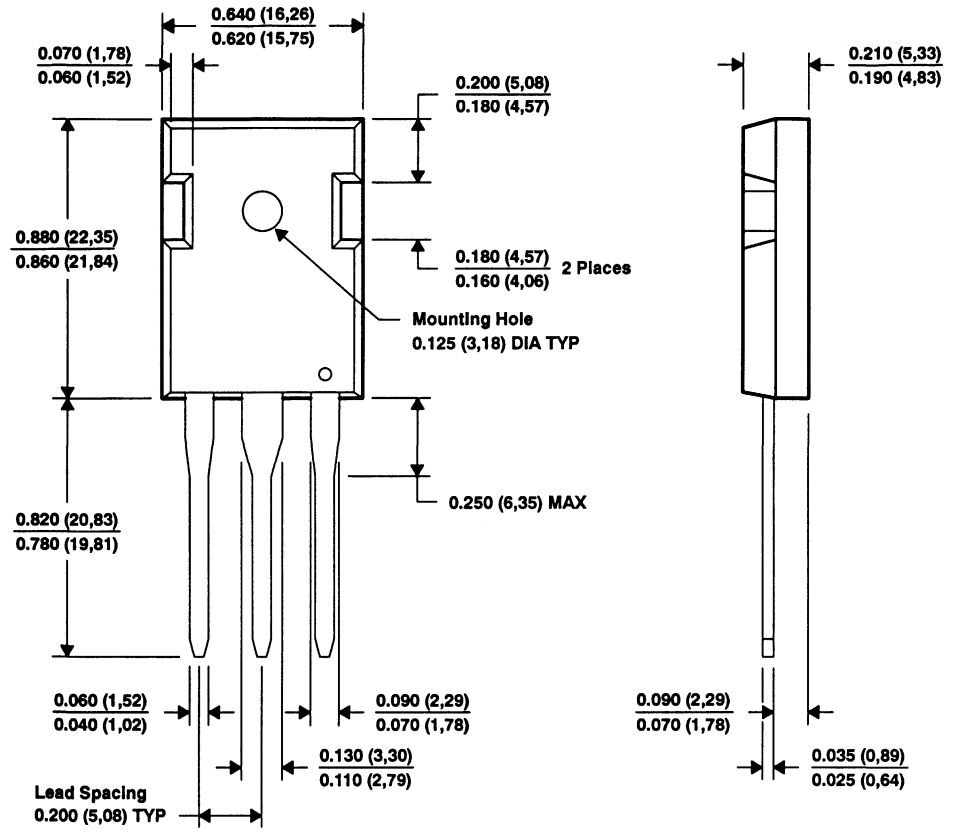
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are with 0.005 (0,13) radius to true position (T.P.) at maximum material conditions.
D. Notches may or may not be present.
E. The center terminal is in electrical contact with the mounting tab.
F. Falls within JEDEC TO-220AB dimensions

KC/R-PSFM-T5 **PLASTIC FLANGE-MOUNT PACKAGE**



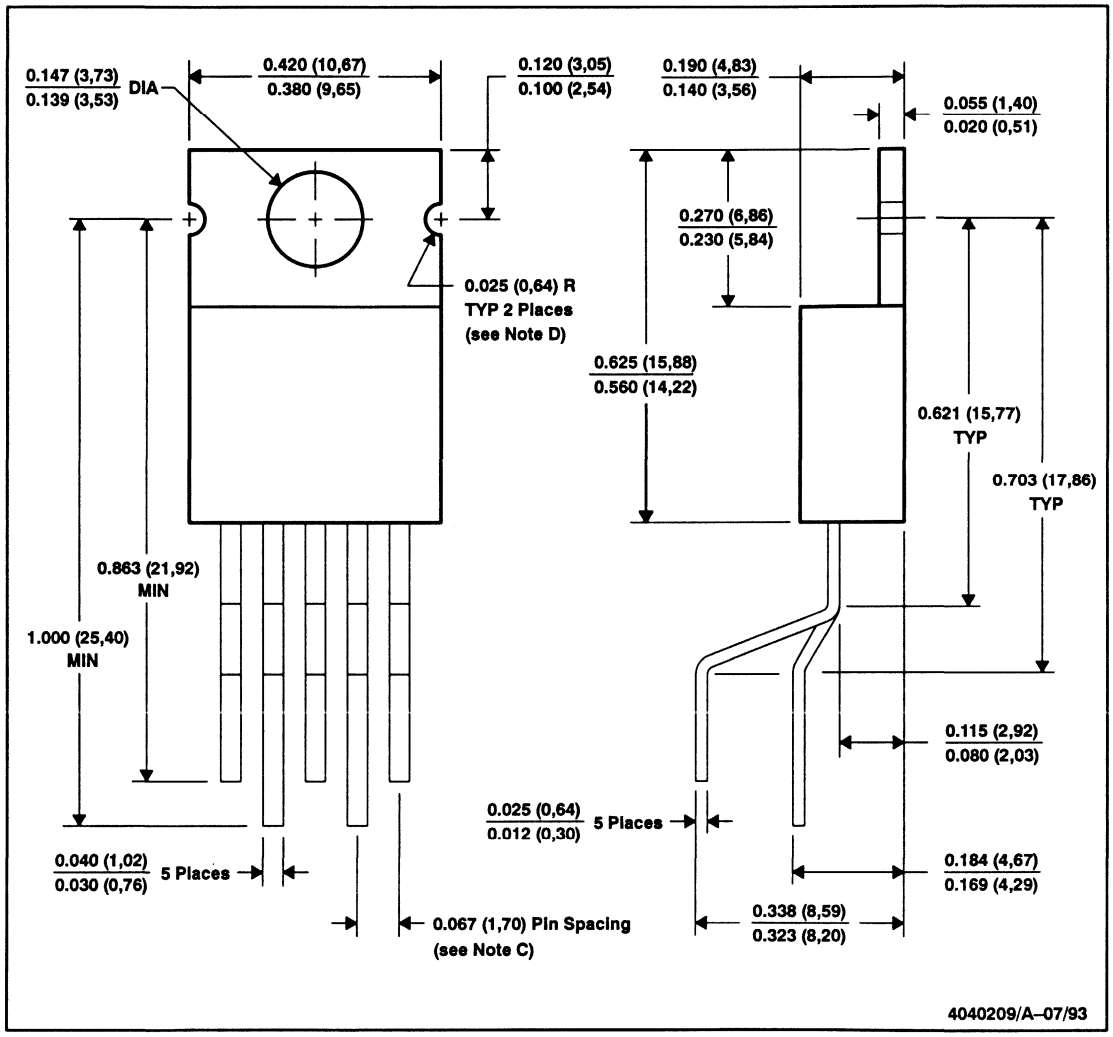
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are with 0.005 (0,13) radius to true position (T.P.) at maximum material conditions.
D. Notches may or may not be present.

KK/R-PSFM-T3 **PLASTIC FLANGE-MOUNT PACKAGE**



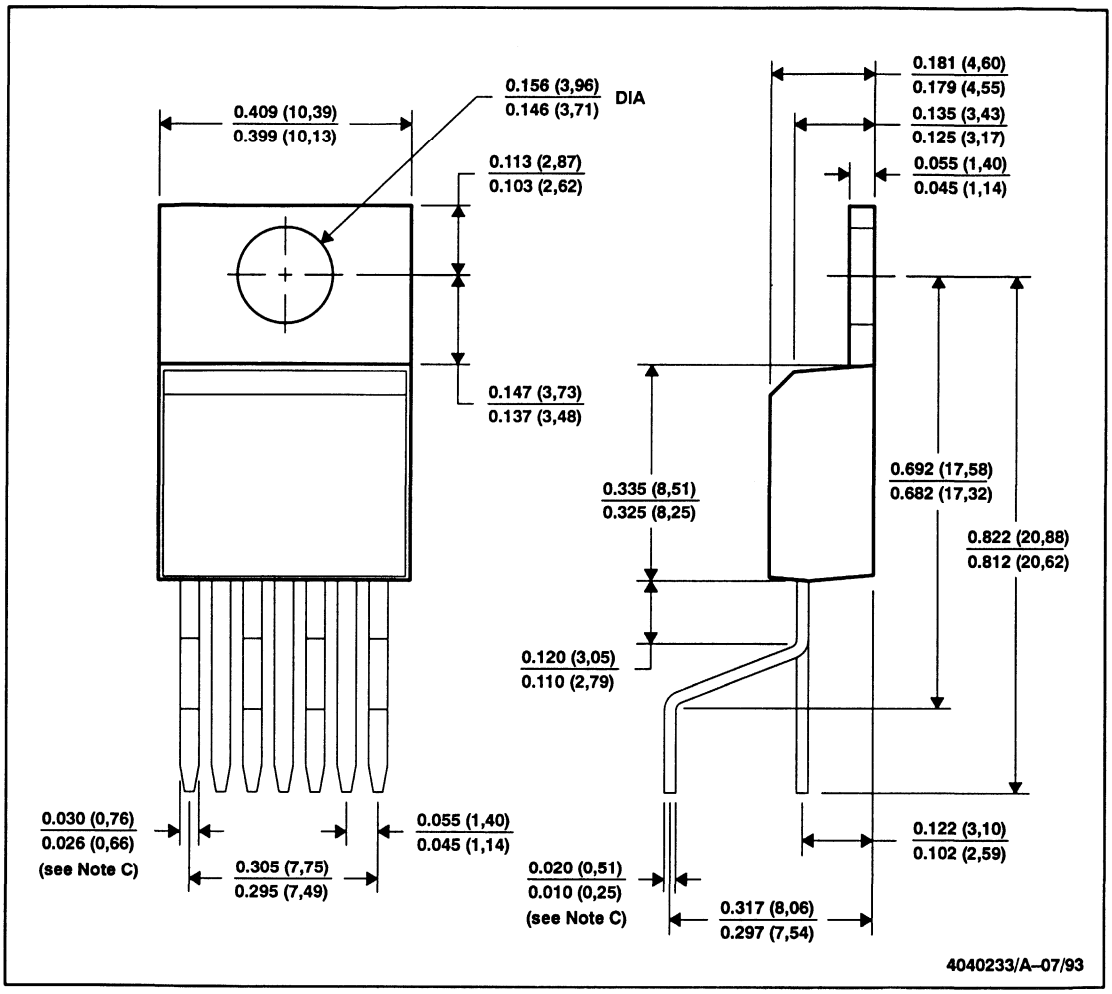
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

KV/R-PSFM-T5 **PLASTIC FLANGE-MOUNT PACKAGE**



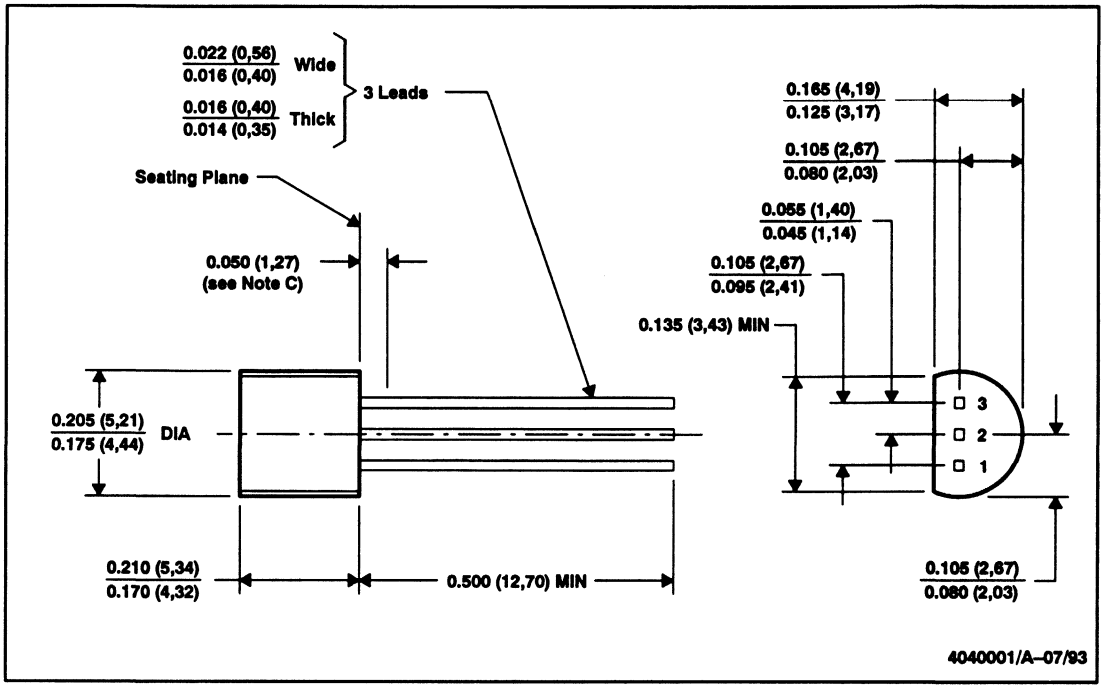
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are with 0.005 (0,13) radius to true position (T.P.) at maximum material conditions.
D. Notches may or may not be present.

KV/R-PZFM-T7 **PLASTIC FLANGE-MOUNT PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. All dimensions apply to solder dip.

LP/O-PBCY-W3 **PLASTIC CYLINDRICAL PACKAGE**

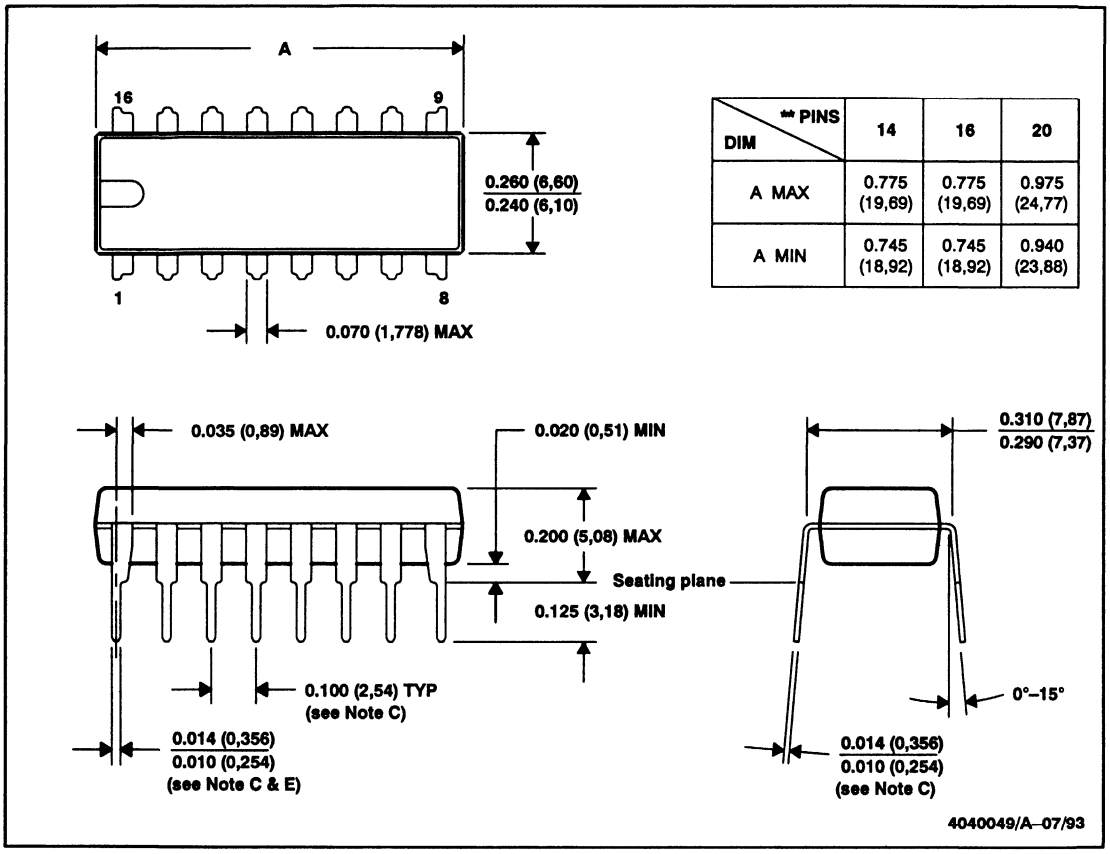


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. Falls within JEDEC TO-226AA dimensions (TO-226AA replaces TO-92).

N/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

16-PIN SHOWN



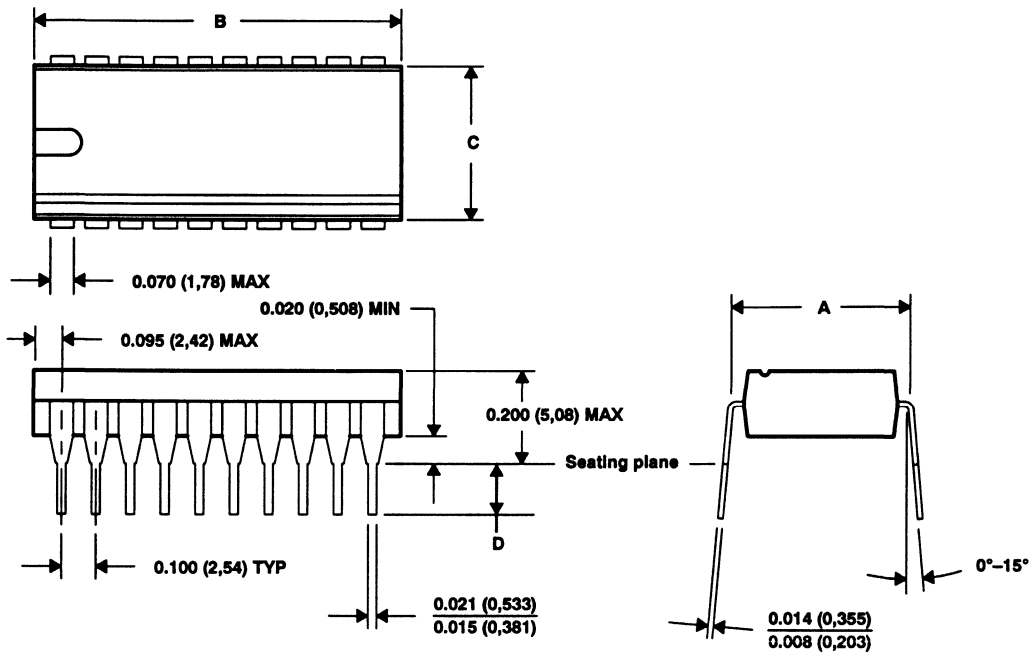
DIM \ ** PINS	14	16	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.940 (23,88)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each pin centerline is located within 0.010 (0,254) of its true longitudinal position.
D. This dimension does not apply for solder-dipped leads.
E. For solder-dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0.51) above seating plane.

N/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

20-PIN SHOWN



DIM \ PINS**	20	22	24	24	24	28	32	40
A MAX	0.325 (8,26)	0.425 (10,80)	0.300 (7,62)	0.425 (10,80)	0.625 (15,88)	0.625 (15,88)	0.625 (15,88)	0.610 (15,49)
B MAX	1.070 (27,18)	1.120 (28,45)	1.252 (31,75)	1.222 (31,04)	1.270 (32,26)	1.450 (36,83)	1.651 (41,94)	2.090 (53,09)
C MAX	0.270 (6,86)	0.355 (9,02)	0.260 (6,60)	0.360 (9,14)	0.550 (13,97)	0.550 (13,97)	0.550 (13,97)	0.550 (13,97)
D MIN	0.115 (2,92)	0.125 (3,18)	0.130 (3,30)	0.125 (3,18)	0.115 (2,92)	0.115 (2,92)	0.125 (3,18)	0.125 (3,18)

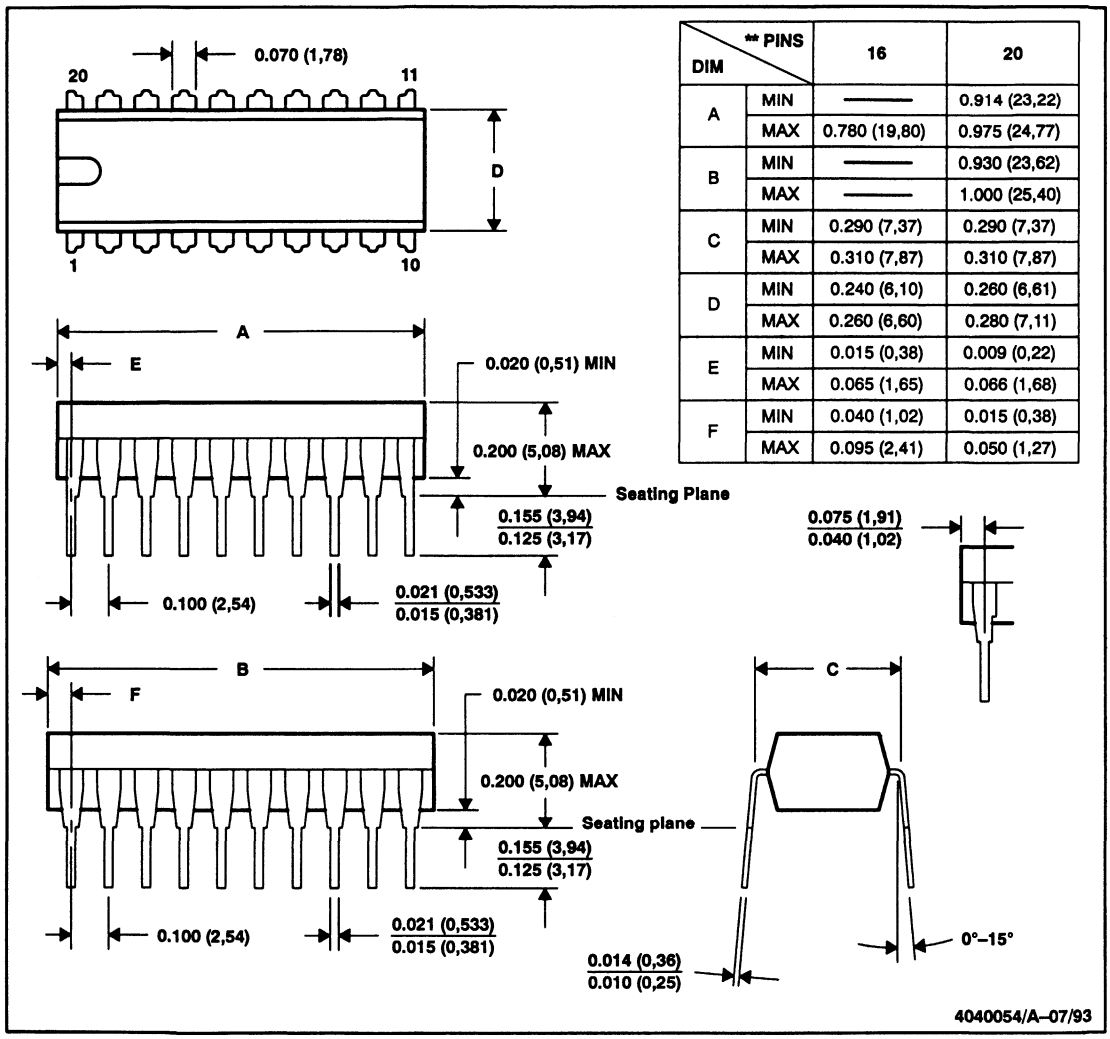
4040051/A–07/93

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

NE/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

20-PIN SHOWN



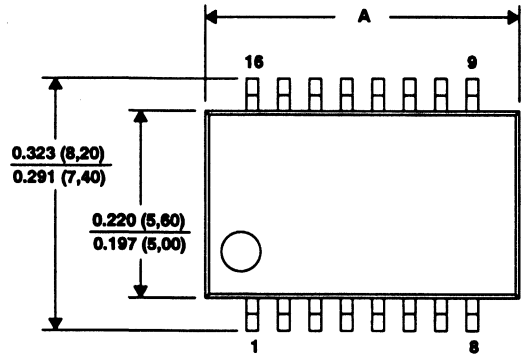
DIM \ ** PINS		16	20
A	MIN	—	0.914 (23,22)
	MAX	0.780 (19,80)	0.975 (24,77)
B	MIN	—	0.930 (23,62)
	MAX	—	1.000 (25,40)
C	MIN	0.290 (7,37)	0.290 (7,37)
	MAX	0.310 (7,87)	0.310 (7,87)
D	MIN	0.240 (6,10)	0.260 (6,61)
	MAX	0.260 (6,60)	0.280 (7,11)
E	MIN	0.015 (0,38)	0.009 (0,22)
	MAX	0.065 (1,65)	0.066 (1,68)
F	MIN	0.040 (1,02)	0.015 (0,38)
	MAX	0.095 (2,41)	0.050 (1,27)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 (0,51) above seating plane.

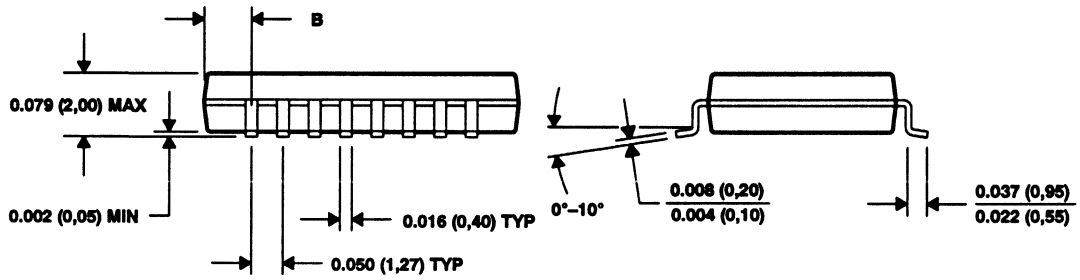
NS/R-PDSO-G**

PLASTIC SMALL-OUTLINE PACKAGE

16-PIN SHOWN



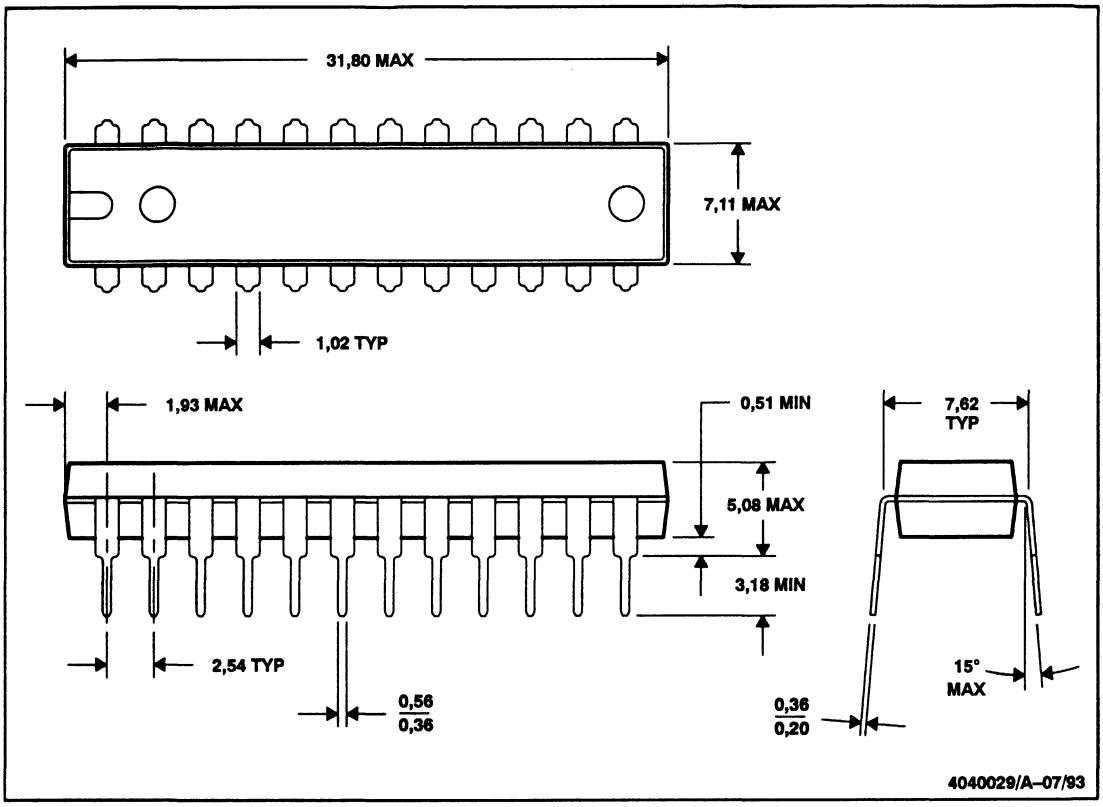
DIM \ ** PINS	14	16	20	24
A MAX	0.413 (10,50)	0.413 (10,50)	0.509 (12,90)	0.602 (15,30)
A MIN	0.390 (9,90)	0.390 (9,90)	0.484 (12,30)	0.579 (14,70)
B MAX	0.057 (1,44)	0.031 (0,81)	0.029 (0,74)	0.026 (0,67)



4040062/A–07/93

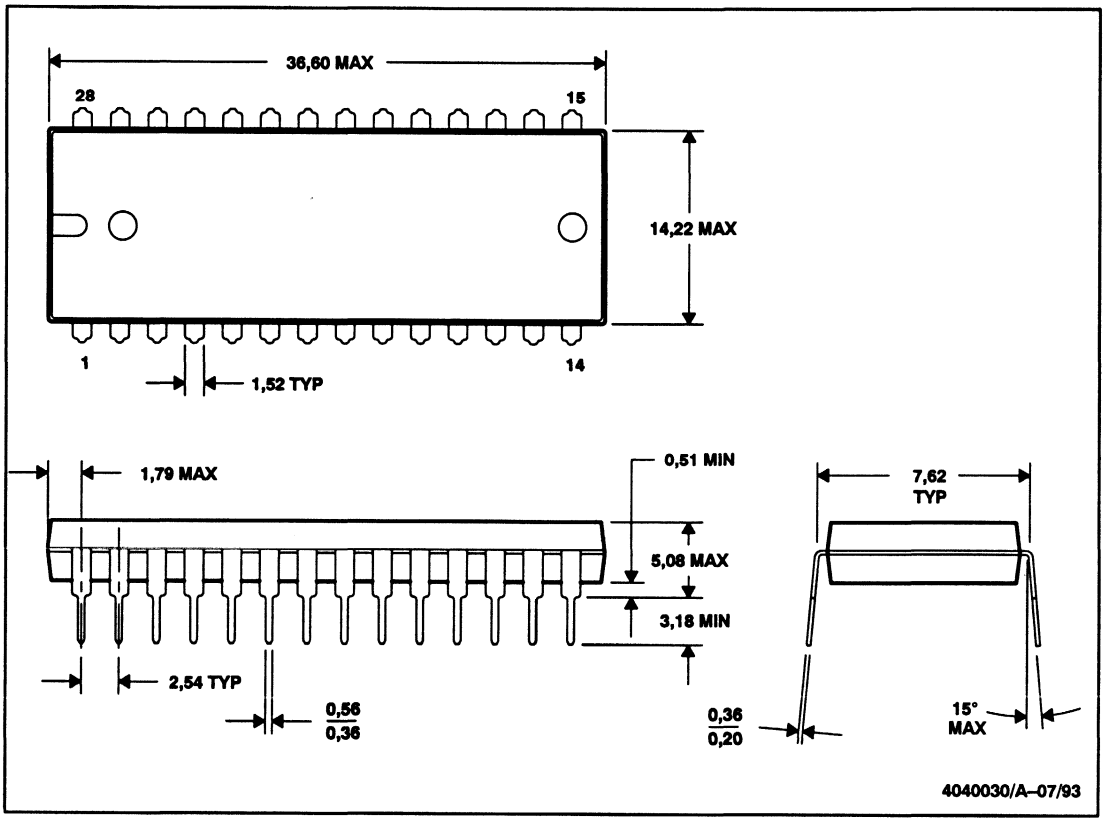
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

NT/R-PDIP-T24 **PLASTIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

NT/R-PDIP-T28 **PLASTIC DUAL-IN-LINE PACKAGE**

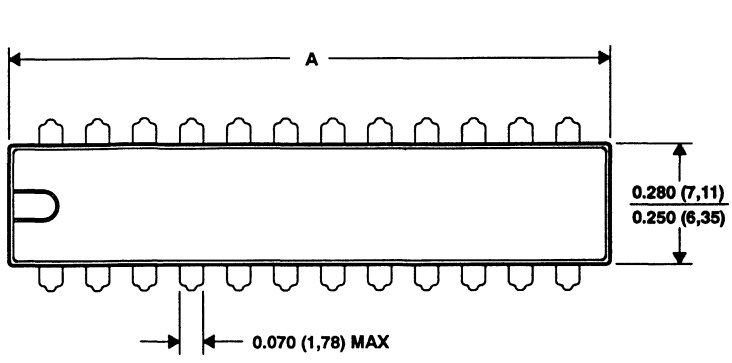


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

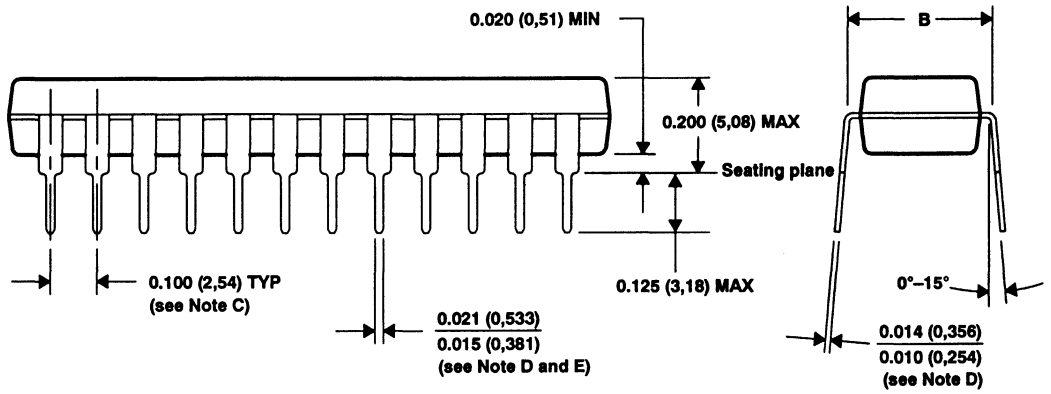
NT/R-PDIP-T**

PLASTIC DUAL-IN-LINE PACKAGE

24-PIN SHOWN



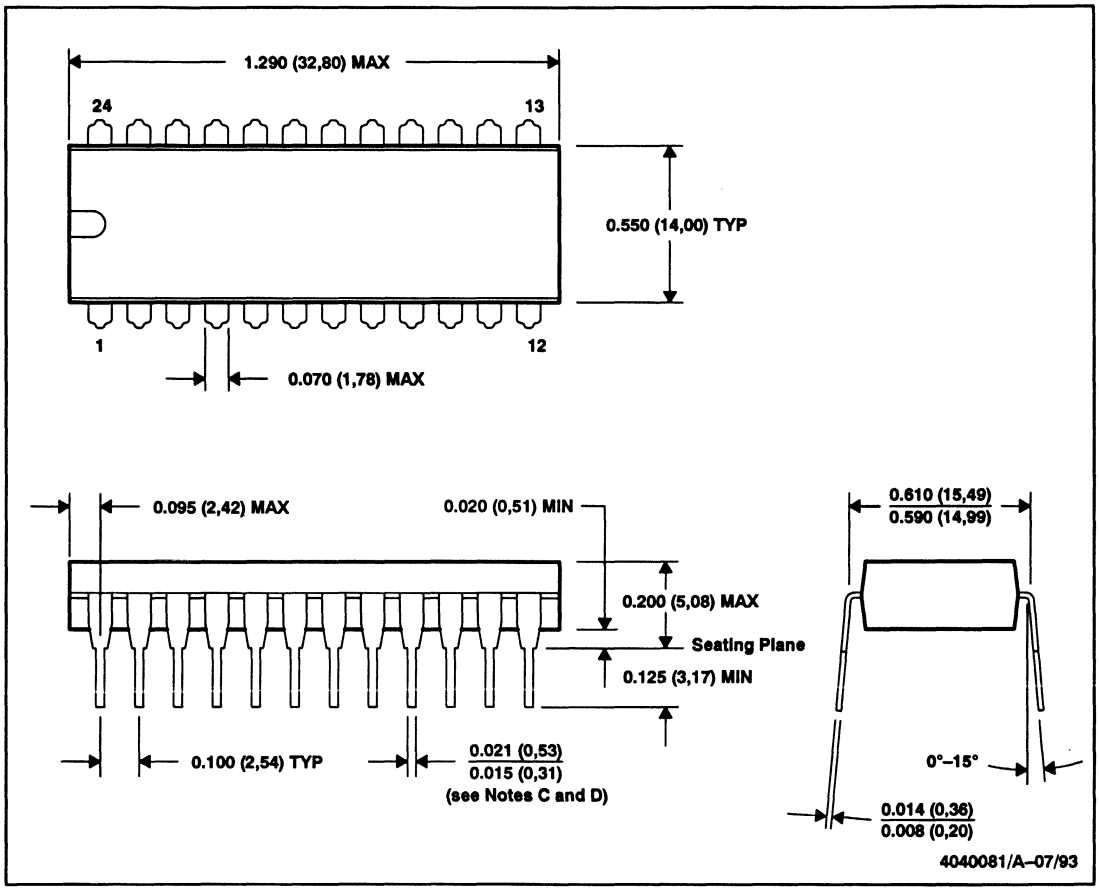
DIM \ PINS**	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)



4040050/A–07/93

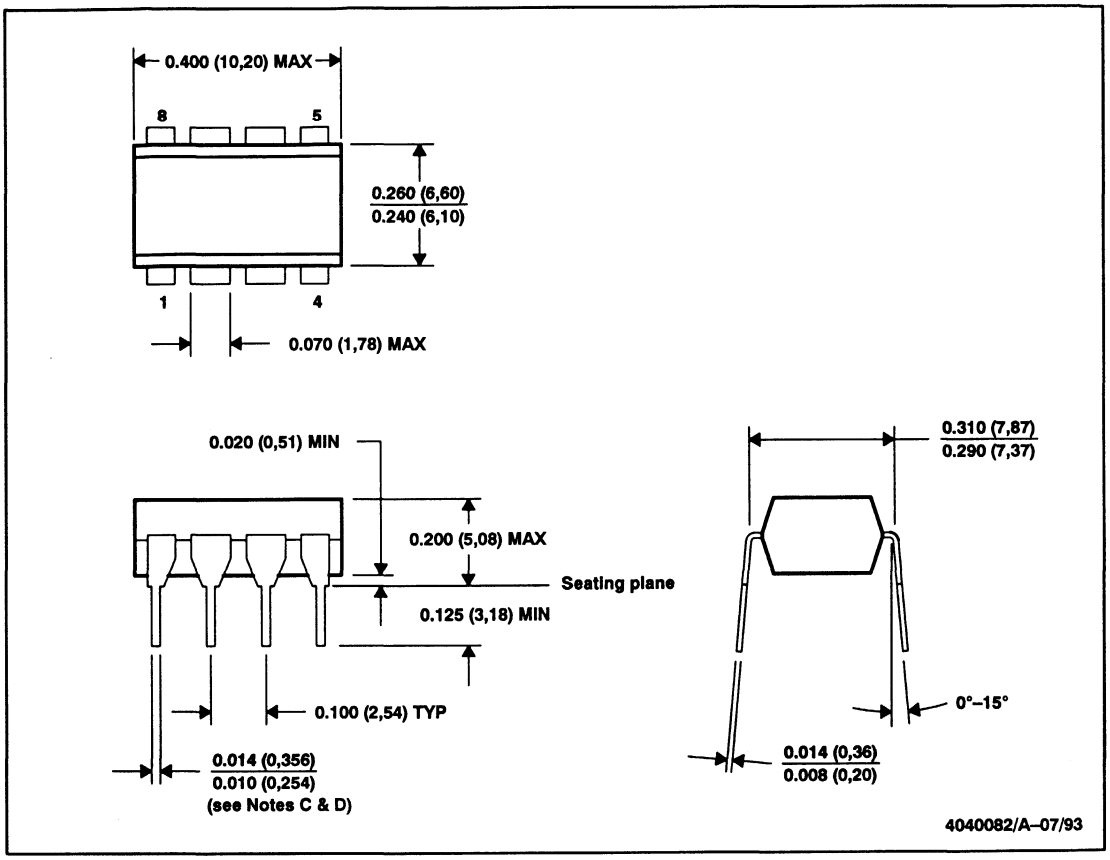
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each pin centerline is located within 0.010 (0,254) of its true longitudinal position.
D. This dimension does not apply for solder-dipped leads.
E. For solder-dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0.51) above seating plane.

NW/R-PDIP-T24 **PLASTIC DUAL-IN-LINE PACKAGE**



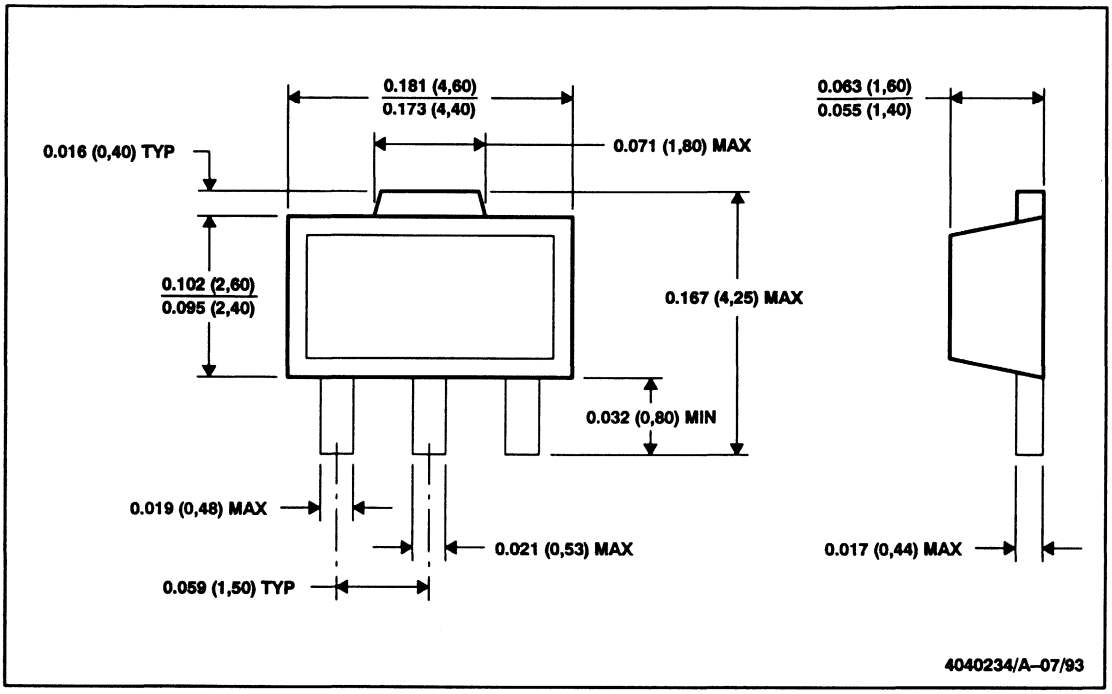
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This dimension does not apply for solder-dipped leads.
D. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 (0,51) above seating plane.

P/R-PDIP-T8 PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This dimension does not apply for solder-dipped leads.
D. For solder-dipped leads, dipping area of the leads extends from the lead tip to at least 0.020 (0.51) above seating plane.

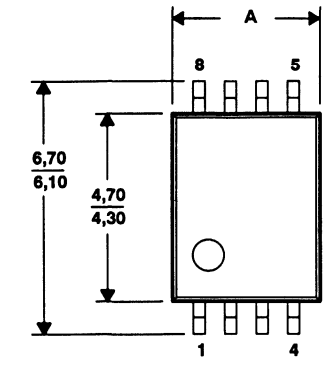
PK/R-PSSO-F3 **PLASTIC LEAD-MOUNT PACKAGE**



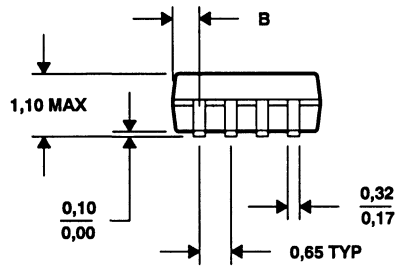
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the tab.

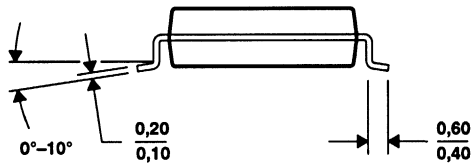
PW/R-PDSO-G** **PLASTIC SMALL-OUTLINE PACKAGE**

8-PIN SHOWN



DIM \ ** PINS	8	14	16	20	24	28
A MAX	3,30	5,30	5,30	6,80	8,10	10,00
A MIN	2,90	4,90	4,90	6,40	7,70	9,60
B MAX	0,65	0,70	0,38	0,48	0,48	0,78

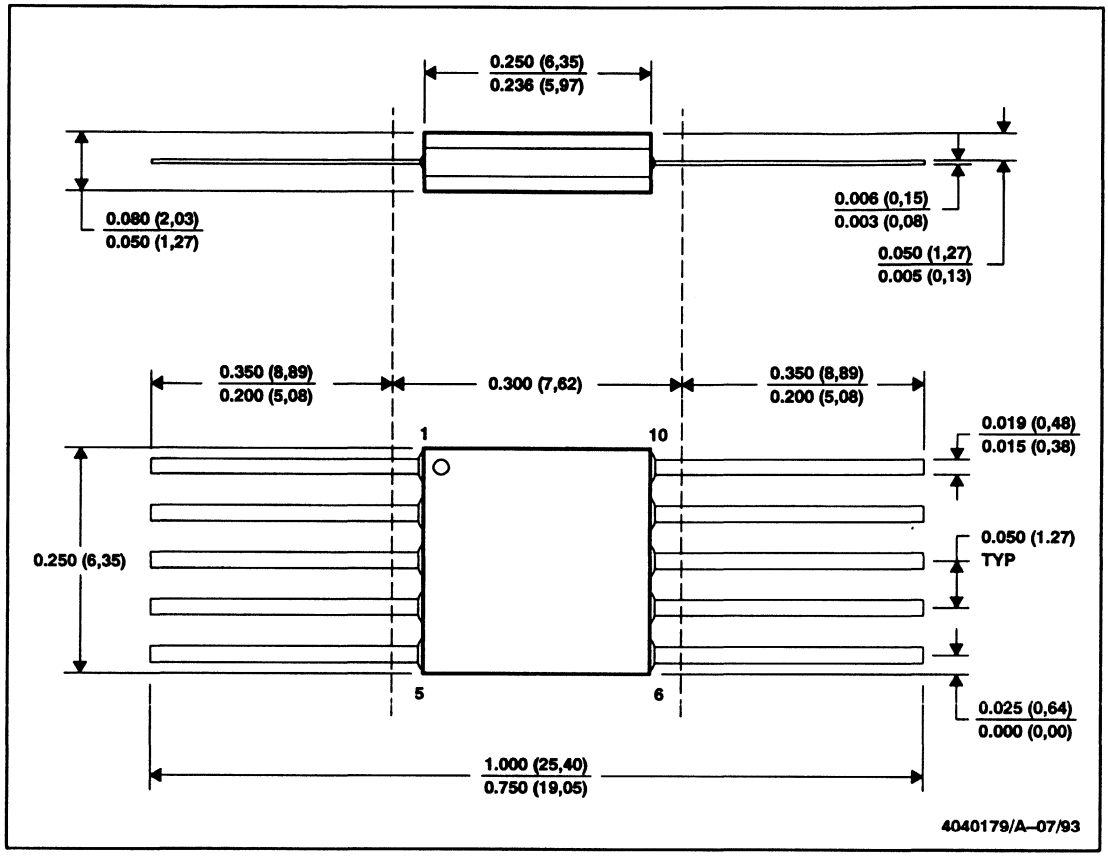




4040064/A–07/93

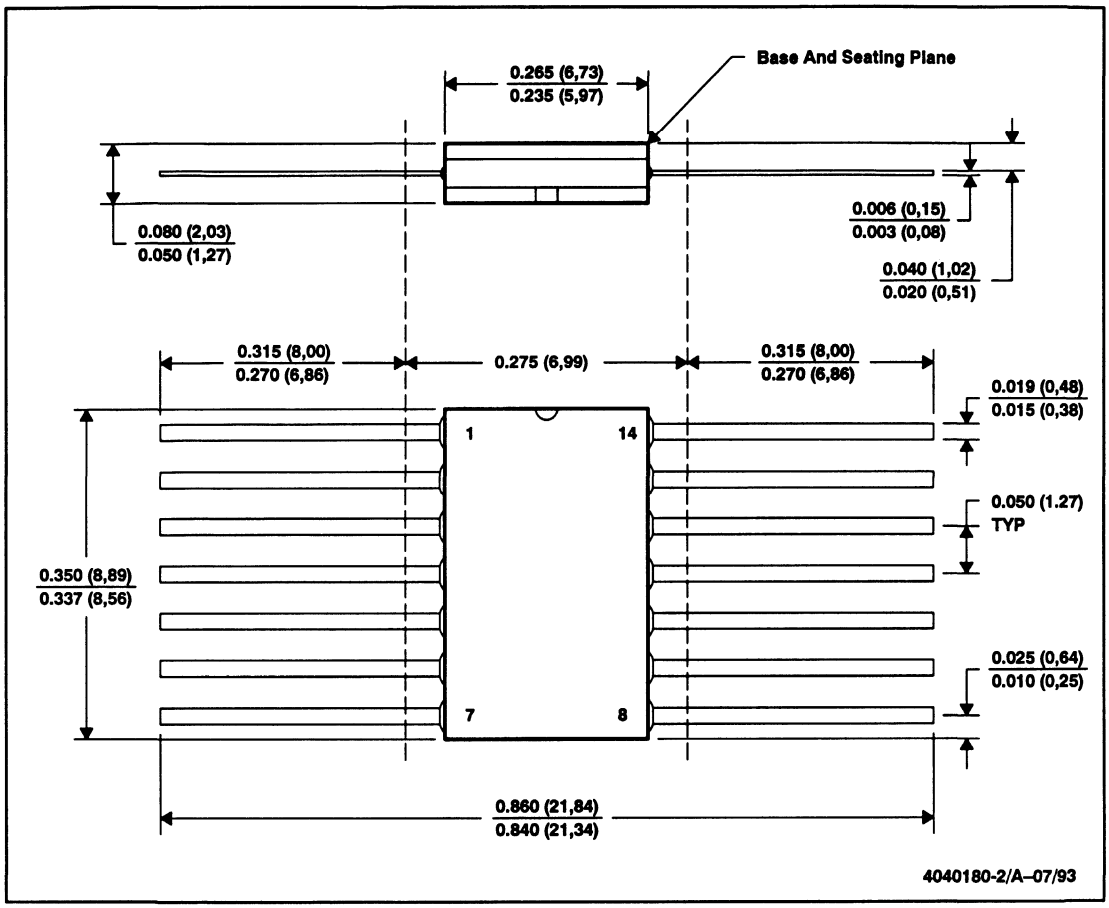
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Drawing source: SCJ Package handbook, 1990

U/S-GDFP-F10 CERAMIC FLAT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
D. Falls within JEDEC MO-004AE dimensions

W/R-GDFP-F14 CERAMIC FLAT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
D. Falls within JEDEC MO-004AA dimensions

NOTES

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